

**IBM Technical Reference Information
for the
Fixed Disk and Diskette
Drive Adapter**

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Fixed Disk and Diskette Drive Adapter

FIXED DISK AND DISKETTE DRIVE ADAPTER

Notes:

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Contents

Description	1
Fixed Disk Function	1
Task File	1
Task File Registers	2
Miscellaneous Information	10
Diskette Function	11
Diskette Controller	13
Controller Commands	15
Command Status Registers	28
Interfaces	32
Interface Lines	33
Logic Diagrams	36
Index	X-1

Notes:

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Description

The Fixed Disk and Diskette Drive Adapter connects to the system board I/O channel using one of the system expansion slots. The adapter controls the diskette drives and fixed disk drives. Connectors on the adapter supply all the signals necessary to operate up to two fixed disk drives and two diskette drives. The adapter will allow concurrent data operations on one diskette and one fixed disk drive.

Fixed Disk Function

The fixed disk function features 512-byte sectors; high-speed, programmed input/output (PIO) data transfers; error correction code (ECC) correction of up to five bits on data fields; multiple sector operations across track and cylinder boundaries; and on-board diagnostic tests. The adapter will support two fixed disks with up to 16 read/write heads and 1024 cylinders.

Task File

A task file, which contains eight registers, controls fixed-disk operations. The following figure shows the addresses and functions of these registers.

I/O Address		Read	Write
Primary	Secondary		
1F0	170	Data Register	Data Register
1F1	171	Error Register	Write Precomp
1F2	172	Sector Count	Sector Count
1F3	173	Sector Number	Sector Number
1F4	174	Cylinder Low	Cylinder Low
1F5	175	Cylinder High	Cylinder High
1F6	176	Drive/Head	Drive/Head
1F7	177	Status Register	Command Register

Task File

Task File Registers

Data Register

The data register provides access to the sector buffer for read and write operations in the PIO mode. This register must not be accessed unless a Read or Write command is being executed. The register provides a 16-bit path into the sector buffer for normal Read and Write commands. When a R/W Long command is issued, the 4 ECC bytes are transferred by byte with at least 2 microseconds between transfers. 'Data Request' (DRQ) must be active before the transferring of the ECC bytes.

Error Register

The error register is a read-only register that contains specific information related to the previous command. The data is valid only when the error bit in the status register is set, unless the adapter is in diagnostic mode. Diagnostic mode is the state immediately after power is switched on or after a Diagnose command. In these cases, the register must be checked regardless of the status register indicator. The following are bit values for the diagnostic mode.

Diagnostic Mode

- 01** No errors
- 02** Controller error
- 03** Sector buffer error
- 04** ECC device error
- 05** Control processor error

The following are bit definitions for the operational mode.

Operational Mode

- Bit 0** Data Address Mark (DAM) Not Found—This bit indicates that DAM could not be found within 16 bytes of the ID field.
- Bit 1** TR 000 Error—This bit will be set if, during a Restore command, the track 000 line from the fixed disk is not true within 1023 step pulses to the drive.
- Bit 2** Aborted Command—A command is aborted based on the drive status (Write Fault, Not Seek Complete, Drive Not Ready, or an invalid command). The status and error registers may be decoded to determine the cause.
- Bit 3** Not used.
- Bit 4** ID Not Found—The ID field with the specified cylinder, head, and sector number could not be found. If retries are enabled, the controller attempts to read the ID 16 times before indicating the error. If retries are disabled, the track is scanned a maximum of two times before setting this error bit.
- Bit 5** Not used
- Bit 6** Data ECC Error—This bit indicates that an uncorrectable ECC error occurred in the target's data field during a read command.
- Bit 7** Bad Block Detect—This bit indicates that the bad block mark was detected in the target's ID field. No Read or Write commands will be executed in any data fields marked bad.

Write Precompensation Register

The value in this register is the starting cylinder number divided by 4. The 'reduced write current' signal to the drive is activated and the adapter's write precompensation logic is turned on when the number is entered into the register.

Sector Count Register

The sector count register defines the number of sectors to be transferred during a Verify, Read, Write, or Format command. During a multi-sector operation, the sector count is decremented and the sector number is incremented. When the disk is being formatted, the number of sectors per track must be loaded into the register prior to each Format command. The adapter supports multi-sector transfers across track and cylinder boundaries. The drive characteristics must be set up by the Set Parameters command before initiating a multi-sector transfer. The sector count register must be loaded with the number of sectors to be transferred for any data-related command.

Note: A 0 in the sector count register specifies a 256-sector transfer.

Sector Number Register

The target's logical sector number for Read, Write, and Verify commands is loaded into this register. The starting sector number is loaded into this register for multi-sector operations.

Cylinder Number Registers

The target number for Read, Write, Seek, and Verify commands is loaded into these registers as shown in the following figure. The cylinder-number registers address up to 1024 cylinders.

	Cylinder High	Cylinder Low
Register Bits	76543210	76543210
Cylinder Bits	_____98	76543210

Cylinder Number Registers

Drive/Head Register

- Bit 7** Set to 1
- Bit 6** Set to 0
- Bit 5** Set to 1
- Bit 4** Drive Select—This bit selects the drive. A 0 indicates the first fixed disk drive, and a 1 indicates the second.
- Bit 3–Bit 0** Head Select Bits—Bits 3 through 0 specify the desired read/write head. Bit 0 is the least-significant (0101 selects head 5). The adapter supports up to 16 read/write heads. For access to heads 8 through 15, bit 3 of the fixed disk register (address hex 3F6) must be set to 1.

Note: This register must be loaded with the maximum number of heads for each drive before a Set Parameters command is issued.

Status Register

The controller sets up the status register with the command status after execution. The program must look at this register to determine the result of any operation. If the busy bit is set, no other bits are valid. A read of the status register clears interrupt request 14. If '-write fault' or 'error' is active, or if '-seek complete' or '-ready' is inactive, a multi-sector operation is aborted.

The following defines the bits of the status register.

- Bit 7** Busy—This bit indicates the controller's status. A 1 indicates the controller is executing a command. If this bit is set, no other status register bit is valid, and the other registers reflect the status register's contents; therefore, the busy bit must be examined before any fixed disk register is read.

- Bit 6** Drive Ready—A 1 on this bit together with a 1 on seek complete bit (bit 4) indicates that the fixed disk drive is ready to read, write, or seek. A 0 indicates that read, write, and seek are inhibited.
- Bit 5** Write Fault—A 1 on this bit indicates improper operation of the drive; read, write, or seek is inhibited.
- Bit 4** Seek Complete—A 1 on this bit indicates that the read/write heads have completed a seek operation.
- Bit 3** Data Request—This bit indicates that the sector buffer requires servicing during a Read or Write command. If either bit 7 (busy) or this bit is active, a command is being executed. Upon receipt of any command, this bit is reset.
- Bit 2** Corrected Data—A 1 on this bit indicates that the data read from the disk was successfully corrected by the ECC algorithm. Soft errors will not end multi-sector operations.
- Bit 1** Index—This bit is set to 1 each revolution of the disk.
- Bit 0** Error—A 1 on this bit indicates that the previous command ended in an error, and that one or more bits are set in the error register. The next command from the controller resets the error bit. This bit, when set, halts multi-sector operations.

Command Register

The command register accepts eight commands to perform fixed disk operations. Commands are executed by loading the task file and writing in the command register while the controller status is not busy. If '-write fault' is active or if '-drive ready' or '-seek complete' are inactive, the controller will not execute any command. Any code not defined in the following causes an Aborted Command error. Interrupt request 14 is reset when any command is written. The following are acceptable commands to the command register.

Command	Bits							
	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read Sector	0	0	1	0	0	0	L	T
Write Sector	0	0	1	1	0	0	L	T
Format Track	0	1	0	1	0	0	0	0
Read Verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set Parameters	1	0	0	1	0	0	0	1

Valid Command-Register Commands

Stepping rate values for R3 through R0 and bit definitions for L and T are shown in the following figures.

R3	R2	R1	R0	Stepping Rate
0	0	0	0	35 us
0	0	0	1	0.5 ms
0	0	1	0	1.0 ms
0	0	1	1	1.5 ms
0	1	0	0	2.0 ms
0	1	0	1	2.5 ms
0	1	1	0	3.0 ms
0	1	1	1	3.5 ms
1	0	0	0	4.0 ms
1	0	0	1	4.5 ms
1	0	1	0	5.0 ms
1	0	1	1	5.5 ms
1	1	0	0	6.0 ms
1	1	0	1	6.5 ms
1	1	1	0	7.0 ms
1	1	1	1	7.5 ms

Stepping Rate

Note: After a Diagnose or Reset Command, the stepping rate is set to 7.5 milliseconds.

Bit	Definition	0	1
L	Data Mode	Data Only	Data Plus 4 Byte ECC
T	Retry Mode	Retries Enabled	Retries Disabled

L and T Bit Definitions

Note: When retries are disabled, ECC and ID field retries are limited to less than two complete revolutions.

Following are descriptions of the valid command-register commands.

Restore: The controller issues step pulses to the drive until the Track 000 indicator from the drive is active. If Track 000 is not active within 1023 steps, the error bit in the status register is set, and a Track 000 error is posted in the error register. The implied seek step rate is set up using the stepping rate figure. The restore step rate is established by the seek complete signal from the drive (each step pulse is issued after seek complete is asserted by the drive from the previous step).

Seek: The Seek command moves the R/W heads to the cylinder specified in the task files. The adapter supports overlapped seeking on two drives or setup of the buffered seek stepping rate for the implied seek during a Read/Write command. An interrupt is generated at the completion of the command.

Read Sector: A number of sectors (1–256) may be read from the fixed disk with or without the ECC field appended in the Programmed I/O (PIO) mode. If the heads are not over the target track, the controller issues step pulses to the drive and checks for the proper ID field before reading any data. The stepping rate used during the implied seek is the value specified during the previous Seek or Restore command. Data errors, up to 5 bits in length, are automatically corrected on Read Short commands. If an uncorrectable error occurs, the data transfer still takes place; however, a multi-sector read ends after the system reads the sector in error. Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command, after the last sector is read by the system.

Write Sector: A number of sectors (1–256) may be written to the fixed disk with or without the ECC field appended in the PIO mode. The Write Sector command also supports implied seeks. Interrupts for the Write command occur before each sector is transferred to the buffer (except the first) and at the end of the command. The first sector may be written to the buffer immediately after the command has been sent, and '-data request' is active.

Format Track: The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table is composed of two bytes per sector as follows: 00, Physical Sector 1; 00, Physical Sector 2; ... 00, Physical Sector 17. The table for 2-to-1 interleave is: 00, 01, 00, 0A, 00, 02, 00, 0B, 00, 03, 00, 0C, 00, 04, 00, 0D, 00, 05, 00, 0E, 00, 06, 00, 0F, 00, 07, 00, 10, 00, 08, 00, 11, 00, 09. The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each Format Track command. An interrupt is generated at the completion of the command; the Format Track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with an 80.

When switching between drives, a restore command must be executed prior to attempting a format.

Perform the following when formatting a drive with more than 8 read/write heads:

1. Restore
2. Format all cylinders, heads 0 - 7 only
3. Restore
4. Format all cylinders, heads 8 and above.

Read Verify: This command is similar to a Read command except that no data is sent to the host. This allows the system to verify the integrity of the fixed disk drive. A single interrupt is generated upon completion of the command or in the event of an error.

Diagnose: This command causes the adapter to execute its self-test code and return the results to the error register. An interrupt is generated at the completion of this command.

Set Parameters: This command sets up the drive parameters (maximum number of heads and sectors per track). The drive/head register specifies the drive affected. The sector count and drive/head registers must be set up before this command is issued. The adapter uses the values specified for track and cylinder crossing during multi-sector operations. An interrupt is generated at the completion of this command. This command must be issued before any multi-sector operations are attempted. The adapter supports two fixed disk drives with different characteristics, as defined by this command.

Miscellaneous Information

The following is miscellaneous information about the fixed disk drive function.

- The adapter performs normal read/write operations on a data field only after a successful match of that sector's ID with the targeted ID.
- ID fields are checked for errors when read from the disk.
- The adapter supports only ECC on data fields and only CRC on ID fields. The CRC polynomial is $X^{16} + X^{12} + X^5 + 1$; the ECC polynomial is $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$. All shift registers are preset to hex F before calculating the checksums, which begin with the respective address marks.

Diskette Function

The 5-1/4 inch diskette drive function is an integral part of the Fixed Disk and Diskette Drive Adapter. Up to two diskette drives may be attached to the adapter through an internal, daisy-chained, flat cable. The attachments support diskette data transfer at 500, 300, 250, and 125 kilobits per second.

The Address assignments for diskette function are shown in the following figure

I/O Address		Read	Write
Primary	Secondary		
3F2	372	Unused	Digital Output Register
3F4	374	Main Status Register	Main Status Register
3F5	375	Diskette Data Register	Diskette Data Register
3F6	376	Unused	Fixed Disk Register
3F7	377	Digital Input Register	Diskette Control Register

Diskette Function

The adapter is designed for a double-density, MFM-coded, diskette drive and uses write precompensation with an analog circuit for clock and data recovery. The diskette-drive parameters are programmable, and the diskette drive's write-protect feature is supported. The adapter is buffered on the I/O bus and uses the system board's direct memory access (DMA) for record data transfers. An interrupt level also is used to indicate when an operation is complete and that a status condition requires microprocessor attention.

Digital Output Register (Hex 3F2)

The digital output register (DOR) is an output-only register used to control drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions follow.

Bit 7 Reserved

Bit 6 Reserved

Bit 5	Drive B Motor Enable
Bit 4	Drive A Motor Enable
Bit 3	Enable Diskette Interrupts and DMA
Bit 2	Diskette Function Reset
Bit 1	Set to a logical 0
Bit 0	Drive Select—A 0 on this bit indicates that drive A is selected.

Note: A channel reset clears all bits.

Digital Input Register

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register.

Bit 7	Diskette Change
Bit 6	Write Gate
Bit 5	Head Select 3/Reduced Write Current
Bit 4	Head Select 2
Bit 3	Head Select 1
Bit 2	Head Select 0
Bit 1	Drive Select 1
Bit 0	Drive Select 0

Note: Bits 0 through 6 apply to the currently selected fixed disk drive. These bits are valid for 50 microseconds after a write to the Drive Head Register.

Diskette Controller

The diskette controller has two registers to which the system unit's microprocessor has access: a status register and a data register. The status register may only be read and is used to facilitate the transfer of data between the processor and diskette controller. The 8-bit status register has the status information about the diskette and may be accessed at any time. The 8-bit data register (hex 3F5), which actually consists of several registers in a stack with only one register presented to the data bus at a time, stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are read from or written to the data register in order to program or obtain results after a particular command.

The bits in the status register (hex 34F) are defined as follows:

- Bit 7** Request for Master (RQM)— The data register is ready to send or receive data to or from the processor.
- Bit 6** Data Input/Output (DIO)—The direction of data transfer between the diskette controller and the processor. If this bit is a 1, transfer is from the diskette controller's data register to the processor; if it is a 0, the opposite is true.
- Bit 5** Non-DMA Mode (NDM)—The diskette controller is in the non-DMA mode.
- Bit 4** Diskette Controller Busy (CB)— A Read or Write command is being executed.
- Bit 3** Reserved
- Bit 2** Reserved
- Bit 1** Diskette Drive B Busy (DBB)— Diskette drive B is in the seek mode.
- Bit 0** Diskette Drive A Busy (DAB)— Diskette drive A is in the seek mode.

Diskette Control Register (hex 3F7)

This register is assigned two addresses, hex 3F7 (primary) and hex 377 (secondary). This is a four bit write only register. The bits are defined as follows:

Bits 3 - 2 Reserved

Bits 1 - 0 Diskette Data Rate— These bits select the diskette data rate as shown in the following figure:

Bit 0	Bit 1	Diskette Data Rate
0	0	500,000 bps
0	1	300,000 bps
1	0	250,000 bps
1	1	125,000 bps

Diskette Data Rate

Fixed Disk Register (hex 3F6)

This register is assigned two addresses, 3F6 (primary) and 376 (secondary). This is a four bit write only register. The bits are defined as follows:

Bit 3 A logical 0 enables reduced write current. A logical 1 enables head select 3.

Bit 2 A logical 1 enables reset fixed disk function.

Bit 1 A logical 0 enables fixed disk interrupts.

Bit 0 Reserved

Note: Bit 3 defines the function of the fixed disk control interface connector (pin 2).

Controller Commands

The diskette controller can perform 16 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the diskette controller and the processor, each command can be considered to consist of three phases:

Command Phase: The processor issues a sequence of Write commands to the diskette controller that direct the controller to perform a specific operation.

Execution Phase: The diskette controller performs the specified operation

Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor through a sequence of Read commands to the processor.

The following is a list of commands that may be issued to the diskette controller:

- Read Data
- Read Deleted Data
- Write Data
- Write Deleted Data
- Read a Track
- Read ID
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek
- Invalid

Symbol Descriptions

The following are descriptions of the symbols used in the "Command Definitions" later in this section.

- A0** Address Line 0—A logical 0 selects the main status register, and a 1 selects the data register.
- C** Cylinder Number—Contains the current or selected cylinder number in binary notation.
- D** Data—Contains the data pattern to be written to a sector.
- D7-D0** Data Bus—An 8-bit data bus in which D7 is the most-significant bit and D0 is the least-significant.
- DTL** Data Length—When N is 00, DTL is the data length to be read from or written to a sector.
- EOT** End of Track—The final sector number on a cylinder.
- GPL** Gap Length—The length of gap 3 (spacing between sectors excluding the VCO synchronous field).
- H** Head Address—The head number, either 0 or 1, as specified in the ID field.
- HD** Head—The selected head number, 0 or 1. (H = HD in all command words.)
- HLT** Head Load Time—The head load time in the selected drive (2 to 256 milliseconds in 2-millisecond increments for the 1.2M-byte drive and 4 to 512 milliseconds in 4-millisecond increments for the 320K-byte drive).
- HUT** Head Unload Time—The head unload time after a read or write operation (0 to 240 milliseconds in 16-millisecond increments for the 1.2M-byte drive and 0 to 480 milliseconds in 32-millisecond increments for the 320K-byte drive).

- MF** FM or MFM Mode—A 0 selects FM mode and a 1 selects MFM (MFM is selected only if it is implemented.)
- MT** Multitrack—A 1 selects multitrack operation. (Both HD0 and HD1 will be read or written.)
- N** Number—The number of data bytes written in a sector.
- NCN** New Cylinder—The new cylinder number for a seek operation
- ND** Non-Data Mode— This indicates an operation in the non-data mode.
- PCN** Present Cylinder Number—The cylinder number at the completion of a Sense interrupt status command (present position of the head).
- R** Record—The sector number to be read or written.
- R/W** Read/Write—This stands for either a 'read' or 'write' signal.
- SC** Sector—The number of sectors per cylinder.
- SK** Skip—This stands for skip deleted-data address mark.
- SRT** This 4 bit byte indicates the stepping rate for the diskette drive as follows:
- 1.2M-Byte Diskette Drive**
 1111 1 millisecond
 1110 2 milliseconds
 1101 3 milliseconds
- 320K-Byte Diskette Drive**
 1111 2 milliseconds
 1110 4 milliseconds
 1101 6 milliseconds
- ST 0—ST 3** Status 0—Status 3—One of the four registers that stores status information after a command is executed.

STP Scan Test—If STP is 1, the data in contiguous sectors is compared with the data sent by the processor during a scan operation. If STP is 2, then alternate sections are read and compared.

US0–US1 Unit Select—The selected driver number encoded the same as bits 0 and 1 of the digital output register (DOR).

Command Definitions

The following are commands that may be issued to the controller.

Note: An X is used to indicate a don't-care condition.
Commands not shown in binary format are shown as bytes.

Read Data

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	SK	0	0	1	1	0
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
DTL

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
C
H
R
N

Read Deleted Data

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	SK	0	1	1	0	0
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
DTL

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
C
H
R
N

Write Data

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	0	0	0	1	0	1
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
DTL

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Write Deleted Data

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	0	0	1	0	0	1
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
DTL

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Read a Track

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	MF	SK	0	0	0	1	0
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
DTL

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Read ID

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	MF	0	0	1	0	1	0
X	X	X	X	X	HD	US1	US0

Result Phase: The following bytes are issued by the processor in the command phase:

ST0
ST1
ST2
C
H
R
N

Format a Track

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	MF	0	0	1	1	0	0
X	X	X	X	X	HD	US1	US0

N
SC
GPL
D

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Scan Equal

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	SK	1	0	0	0	1
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
STP

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Scan Low or Equal

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	SK	1	1	0	0	1
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
STP

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Scan High or Equal

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
MT	MF	SK	1	1	1	0	1
X	X	X	X	X	HD	US1	US0

C
H
R
N
EOT
GPL
STP

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
ST1
ST2
C
H
R
N

Recalibrate

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1
X	X	X	X	X	0	US1	US0

Result Phase: This command has no result phase.

Sense Interrupt Status

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0

Result Phase: The following bytes are issued by the controller in the result phase:

ST0
PCN

Specify

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	1	
(SRT)	(HUT)	(ND)
	HLT							

Result Phase: This command has no result phase.

Sense Driver Status

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0
X	X	X	X	X	HD	US1	US0

Result Phase: The following bytes are issued by the controller in the result phase:

ST3

Seek

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1
X	X	X	X	X	HD	US1	US0

NCN

Result Phase: This command has no result phase.

Invalid

Command Phase: The following bytes are issued by the processor in the command phase:

D7	D6	D5	D4	D3	D2	D1	D0
			Invalid Codes				
X	X	X	X	X	HD	US1	US0

Result Phase: The following byte is issued by the controller in the result phase:

ST0

Command Status Registers

The following is information about the command status registers ST0 through ST3.

Command Status Register 0 (ST0)

The following are bit definitions for command status register 0.

- Bit 7–Bit 6** Interrupt Code (IC)
- 00** Normal Termination of Command (NT)—The command was completed and properly executed.
 - 01** Abrupt Termination of Command (AT)—The execution of the command was started but not successfully completed.
 - 10** Invalid Command Issue (IC)—The issued command was never started.
 - 11** Abnormal termination because, during the execution of a command, the 'ready' signal from the diskette drive changed state.
- Bit 5** Seek End (SE)—Set to 1 when the controller completes the Seek command.
- Bit 4** Equipment Check (EC)—Set if a 'fault' signal is received from the diskette drive, or if the 'track-0' signal fails to occur after 77 step pulses (Recalibrate Command).
- Bit 3** Not Ready (NR)—This flag is set when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.

Bit 2 **Head Address (HD)**—Indicates the state of the head at interrupt.

Bit 1–Bit 0 **Unit select 0 and 1 (US 0 and 1)**—Indicate a drive's unit number at interrupt. The following figure shows the binary values to select each drive.

Bit 1	Bit 0	Drive Selected
0	0	A
0	1	B
1	0	Unused
1	1	Unused

Unit Selection

Command Status Register 1 (ST1)

The following are bit definitions for command status register 1.

Bit 7 **End of Cylinder (EC)**—Set when the controller tries to gain access to a sector beyond the final sector of a cylinder.

Bit 6 **Not Used**—Always 0.

Bit 5 **Data Error (DE)**—Set when the controller detects a CRC error in either the ID field or the data field.

Bit 4 **Overrun (OR)**—Set if the controller is not serviced by the main system within a certain time limit during data transfers.

Bit 3 **Not Used**—This bit is always set to 0.

Bit 2 **No Data (ND)**—Set if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan Command. This flag is also set if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read Cylinder command.

- Bit 1** Not Writable (NW)—Set if the controller detects a 'write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.
- Bit 0** Missing Address Mark (MA)—Set if the controller cannot detect the ID address mark. At the same time, the MD of status register 2 is set.

Command Status Register 2 (ST2)

- Bit 7** Not Used—Always 0.
- Bit 6** Control Mark (CM)—This flag is set if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.
- Bit 5** Data Error in Data Field (DD)—Set if the controller detects an error in the data.
- Bit 4** Wrong Cylinder (WC)—This flag is related to ND (no data) and when the contents of C on the medium are different from that stored in the ID register, this flag is set.
- Bit 3** Scan Equal Hit (SH)—Set if the contiguous sector data equals the processor data during the execution of a Scan command.
- Bit 2** Scan Not Satisfied (SN)—Set if the controller cannot find a sector on the cylinder that meets the condition during a Scan command.
- Bit 1** Bad Cylinder (BC)—Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set.
- Bit 0** Missing Address Mark in Data Field (MD)— Set if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Command Status Register 3 (ST3)

The following are bit definitions for command status register 3.

- Bit 7** **Fault (FT)**—Status of the 'fault' signal from the diskette drive.
- Bit 6** **Write Protect (WP)**—Status of the 'write-protect' signal from the diskette drive.
- Bit 5** **Ready (RY)**—Status of the 'ready' signal from the diskette drive.
- Bit 4** **Track 0 (T0)**—Status of the 'track 0' signal from the diskette drive.
- Bit 3** **Two Side (TS)**—Status of the 'two side' signal from the diskette drive.
- Bit 2** **Head Address (HD)**—Status of the 'side select' signal from the diskette drive.
- Bit 1** **Unit Select 1 (US 1)**—Status of the 'unit select 1' signal from the diskette drive.
- Bit 0** **Unit Select 0 (US 0)**—Status of the 'unit select 0' signal from the diskette drive.

Interfaces

The system interface is through the I/O channel. The address, DMA, and interrupt assignments are shown in the following figures.

I/O Address		Read	Write
Primary	Secondary		
3F2	372	Unused	Digital Output Register
3F4	374	Main Status Register	Main Status Register
3F5	375	Diskette Data Register	Diskette Data Register
3F6	376	Unused	Fixed Disk Register
3F7	377	Digital Input Register	Diskette Control Register

Diskette Function

Note: DMA request is level 2 and interrupt request is level 6.

I/O Address		Read	Write
Primary	Secondary		
1F0	170	Data Register	Data Register
1F1	171	Error Register	Write Precomp
1F2	172	Sector Count	Sector Count
1F3	173	Sector Number	Sector Number
1F4	174	Cylinder Low	Cylinder Low
1F5	175	Cylinder High	Cylinder High
1F6	176	Drive/Head	Drive/Head
1F7	177	Status Register	Command Register

Fixed Disk Function

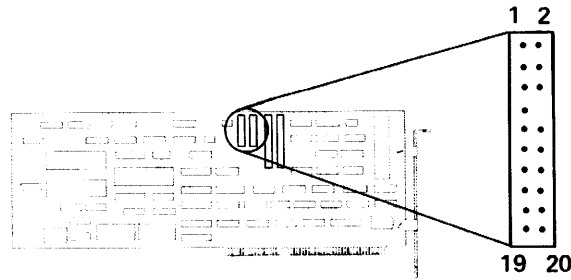
Note: Interrupt request is level 14.

The following operations are supported by this adapter:

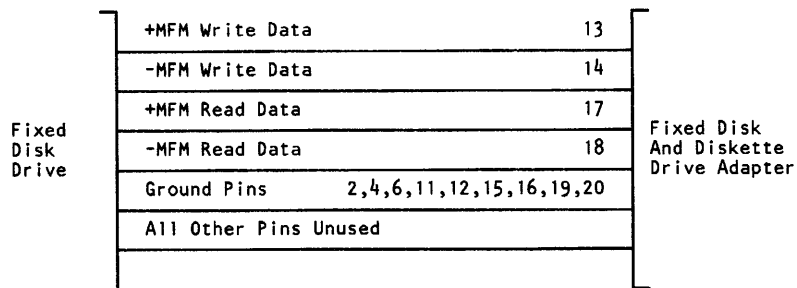
- 16 bit programmed I/O (PIO), data transfers to the fixed disk. All other transfers are 8 bits wide.
- The I/O addresses, recognized by the adapter for either the fixed disk or the diskette function, are independently selected by jumpers.

Interface Lines

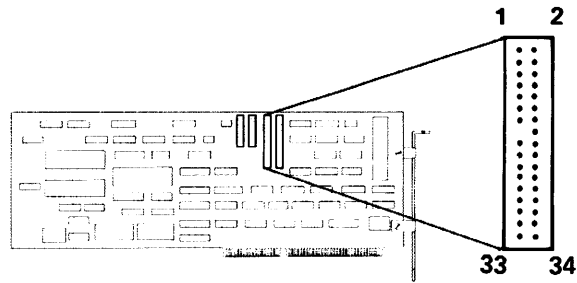
The interface to the fixed disk drive consists of the Control cable and the Data cable. The following figures show signals and pin assignments for these cables.



Fixed Disk Control Cable Connector



Note: Connection is through a 2-by-10 Berg connector. Pin 8 is reserved to polarize the connector.

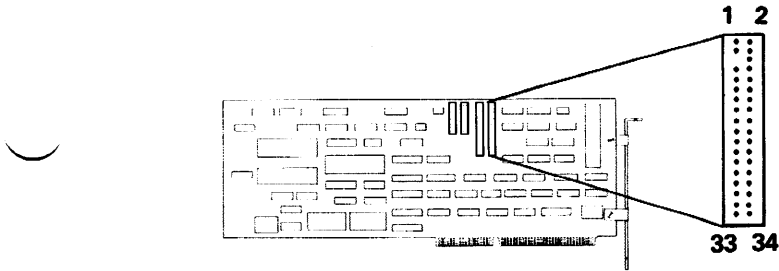


Fixed Disk Data Cable Connector

Fixed Disk Drive	Ground (All Odd Numbers)	1 through 33	Fixed Disk And Diskette Drive Adapter
	-Reduced Write Current/-Head Select 3	2	
	-Head Select 2	4	
	-Write Gate	6	
	-Seek Complete	8	
	-Track 000	10	
	-Write Fault	12	
	-Head Select 0	14	
	Reserved	16	
	-Head Select 1	18	
	-Index	20	
	-Ready	22	
	-Step	24	
	-Drive Select 1	26	
	-Drive Select 2	28	
	Reserved	30	
	Reserved	32	
-Direction In	34		

Note: Connection is through a 2-by-17 Berg connector. Pin 15 is reserved to polarize the connector.

The interface to the diskette drives is a single cable that carries both data and control signals. The following figures show signal and pin assignments for this cable.

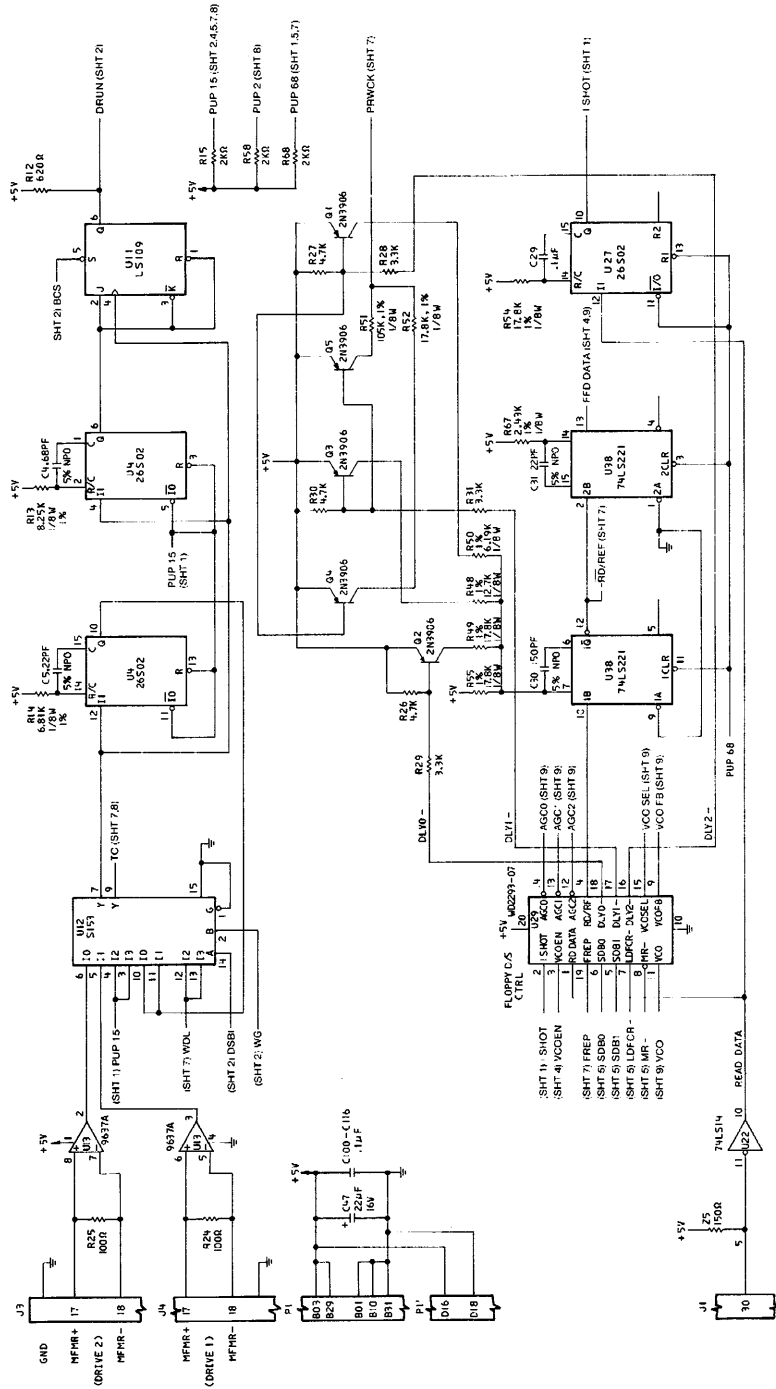


Diskette Data and Control Connector

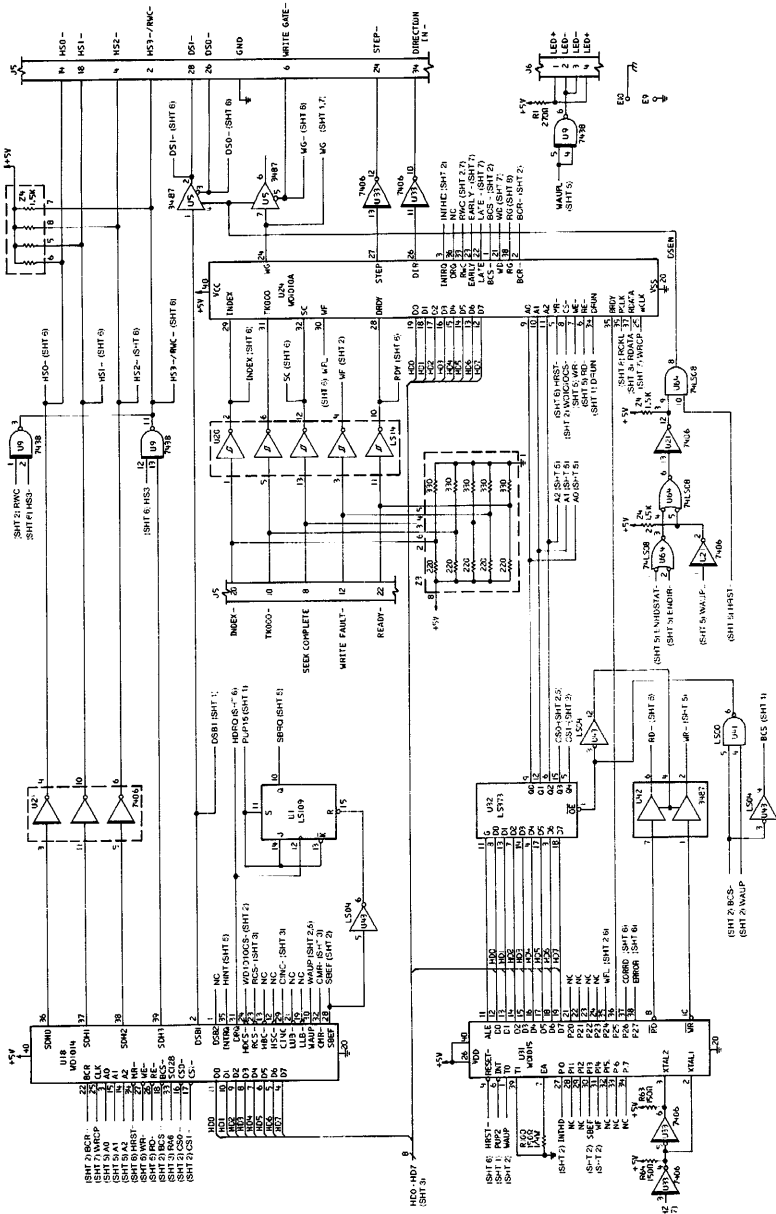
	Ground (All Odd Numbers)	1 through 33	
	-Reduced Write	2	
	Reserved	4	
	-Drive Select 3	6	
	-Index	8	
	-Drive Select 0	10	
	-Drive Select 1	12	
	-Drive Select 2	14	
	-Motor On	16	
Diskette Drive	-Direction Select	18	Fixed Disk And Diskette Drive Adapter
	-Step	20	
	-Write Data	22	
	-Write Gate	24	
	-Track 00	26	
	-Write Protect	28	
	-Read Data	30	
	-Side 1 Select	32	
	-Diskette Change	34	

Note: Connection is through a 2-by-17 Berg connector. Pin 5 is reserved to polarize the connector.

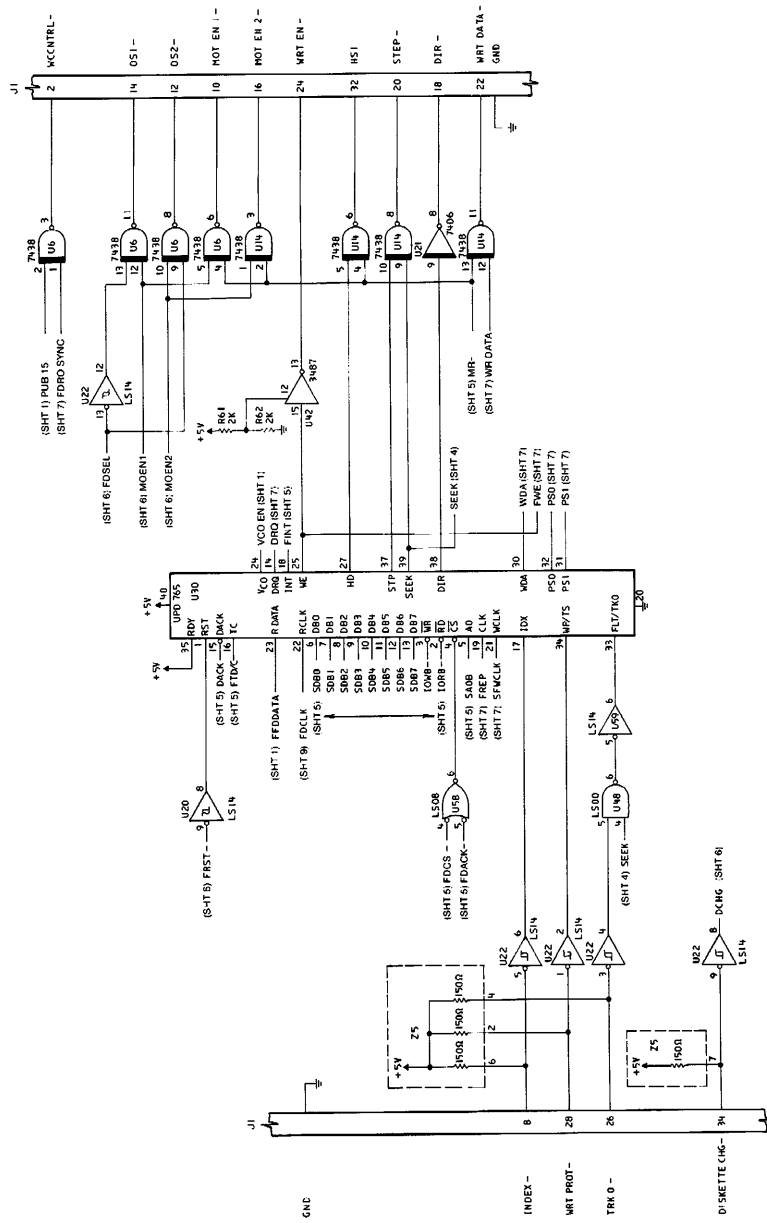
Logic Diagrams



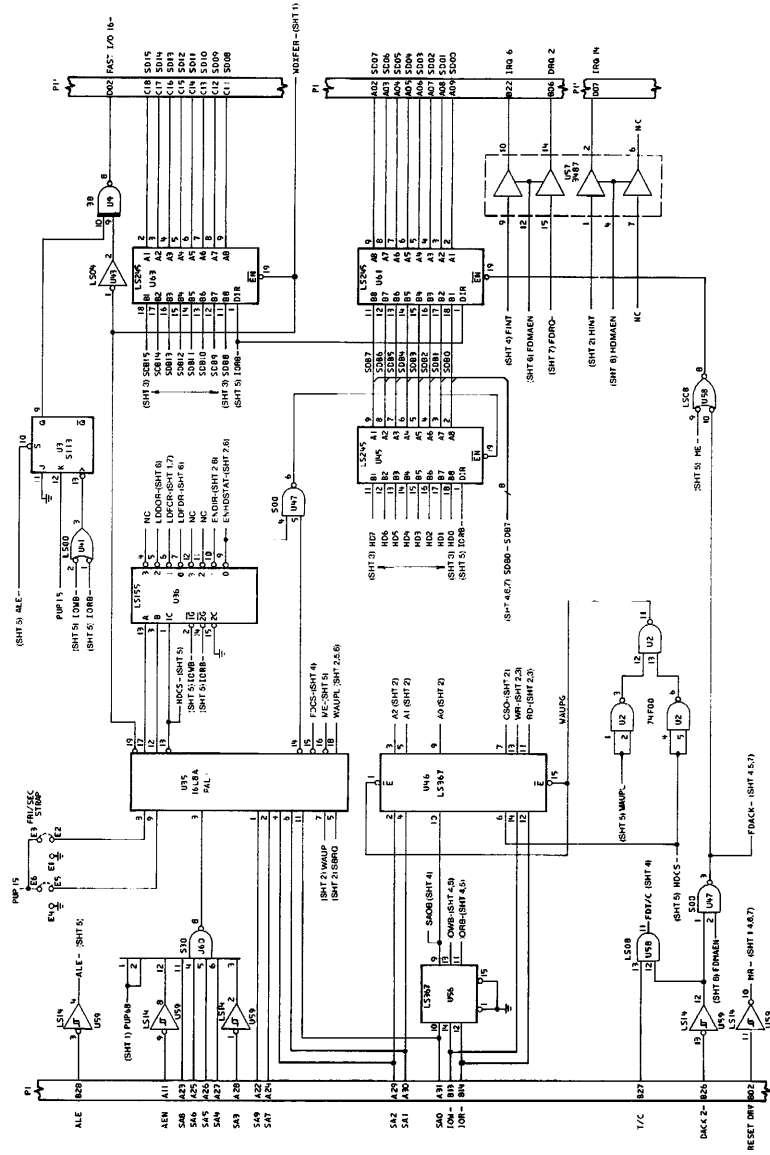
Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 1 of 9)



Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 2 of 9)

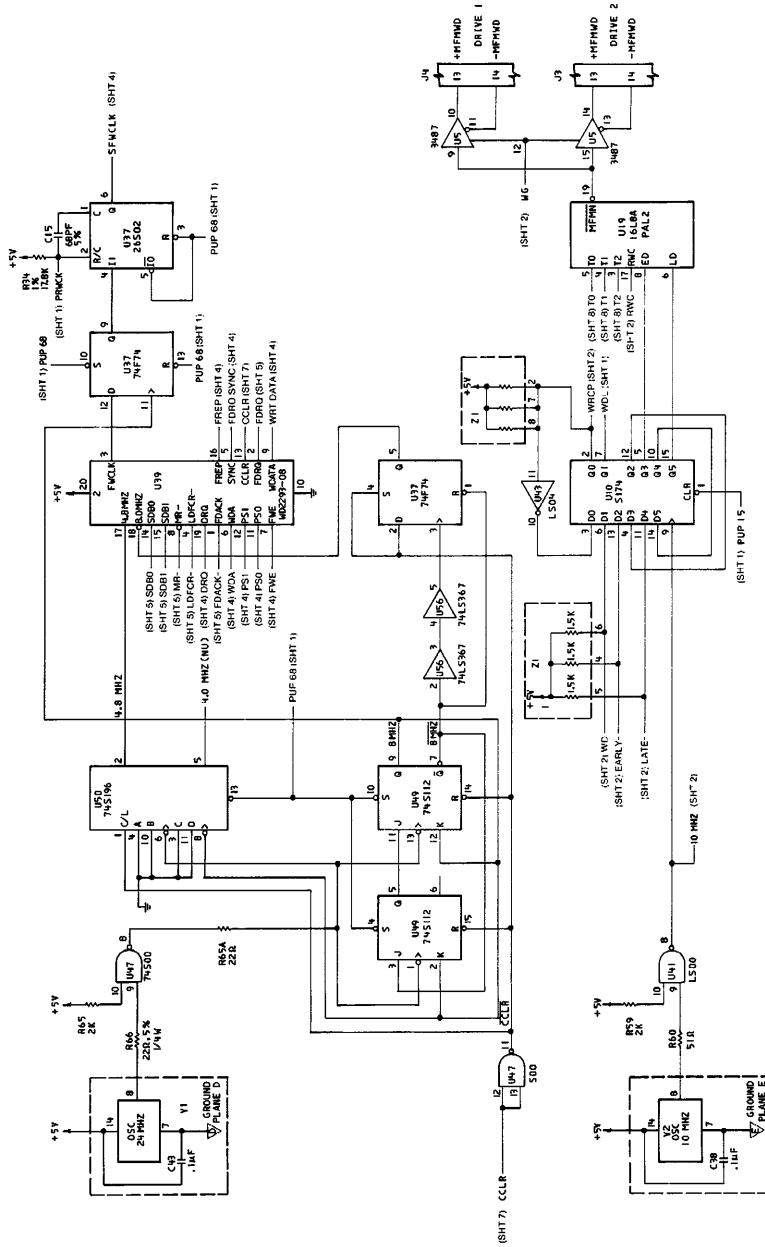


Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 4 of 9)

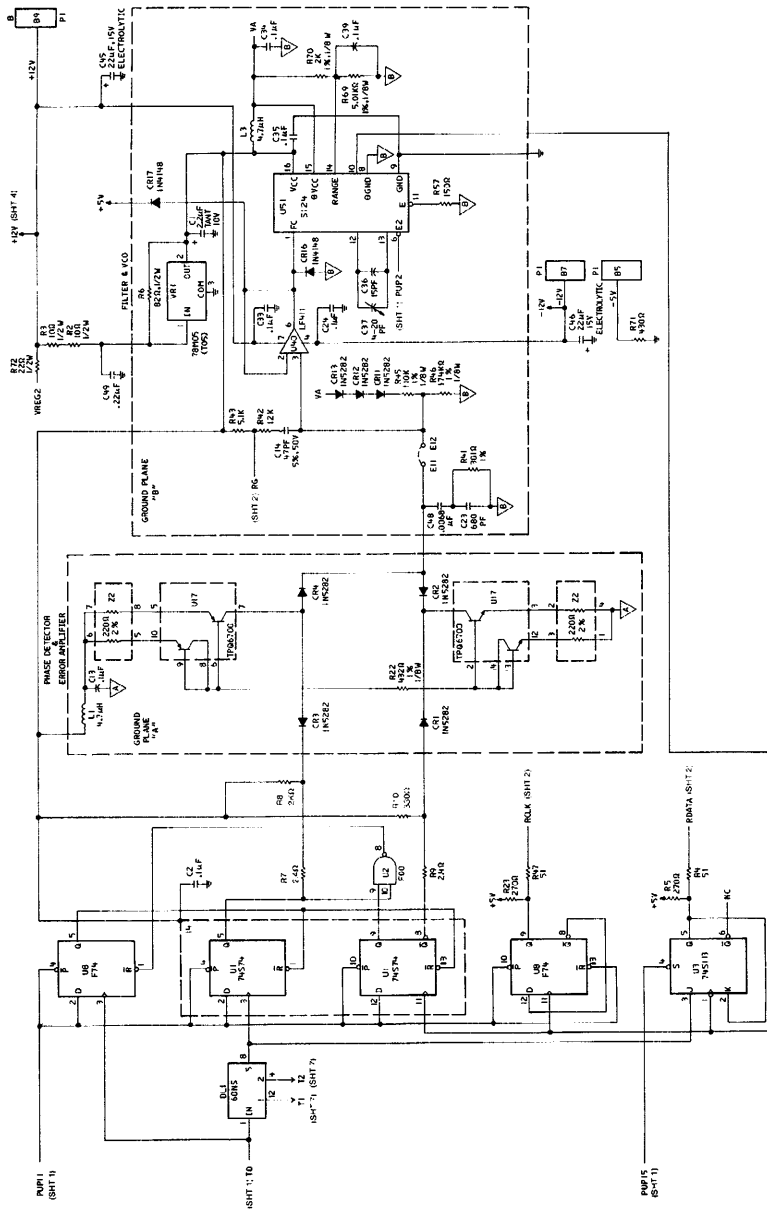


Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 5 of 9)

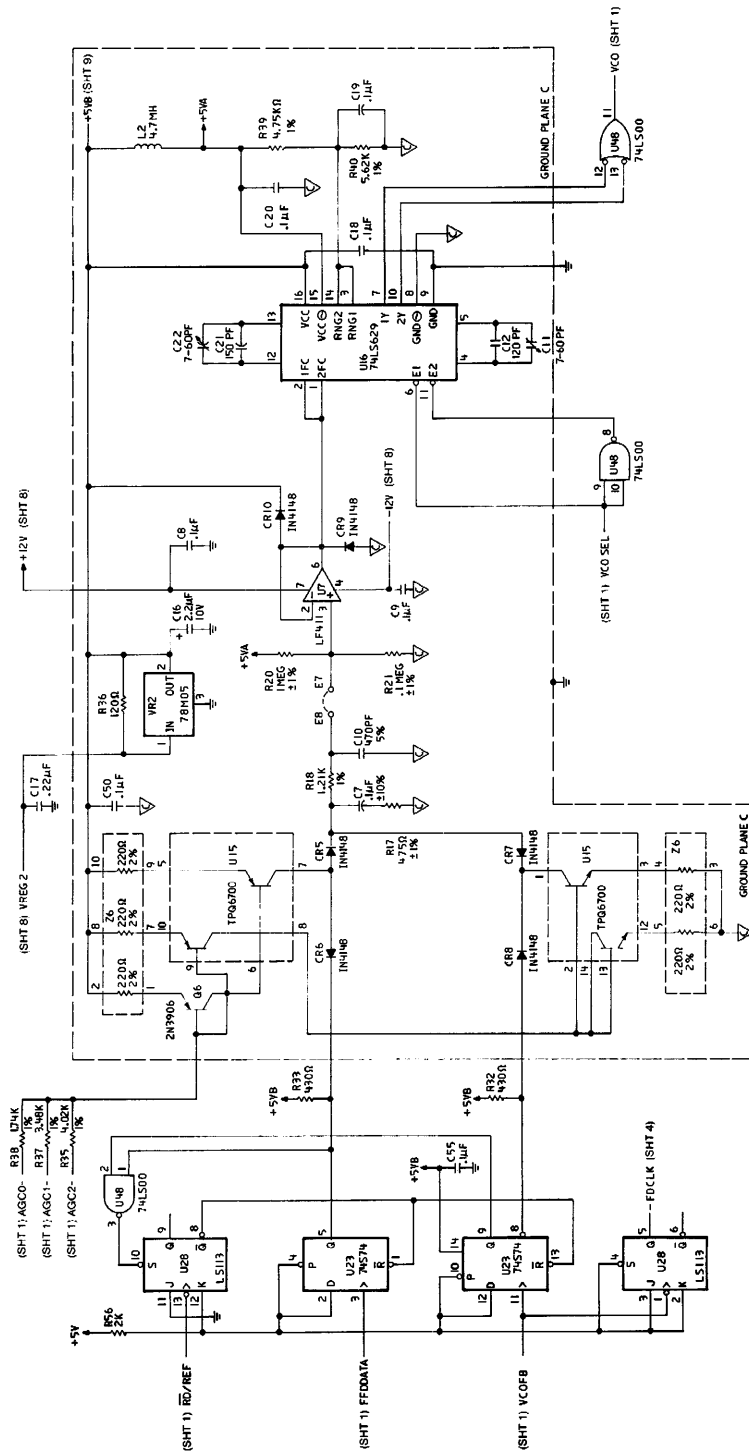
Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 5 of 9)



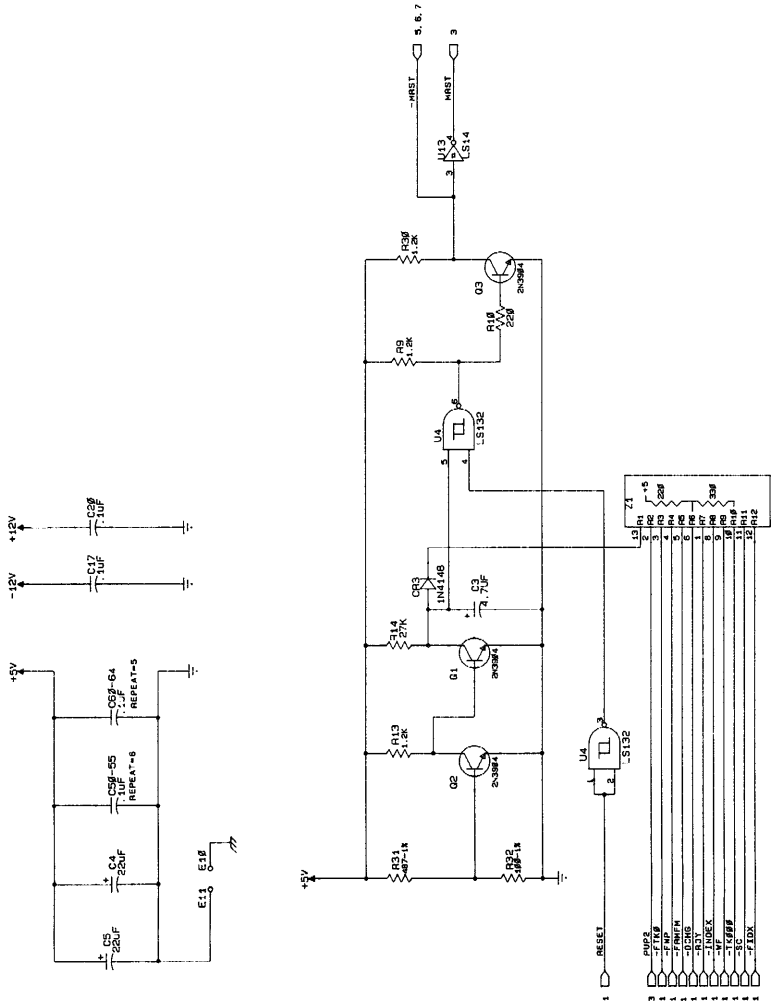
Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 7 of 9)



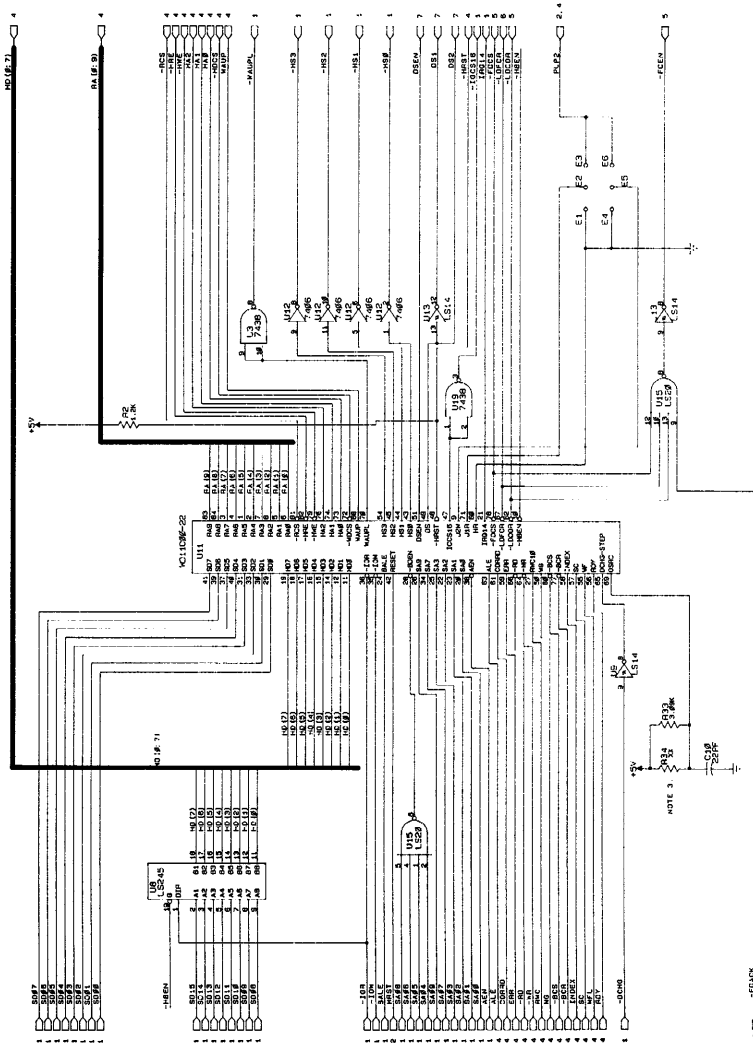
Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 8 of 9)



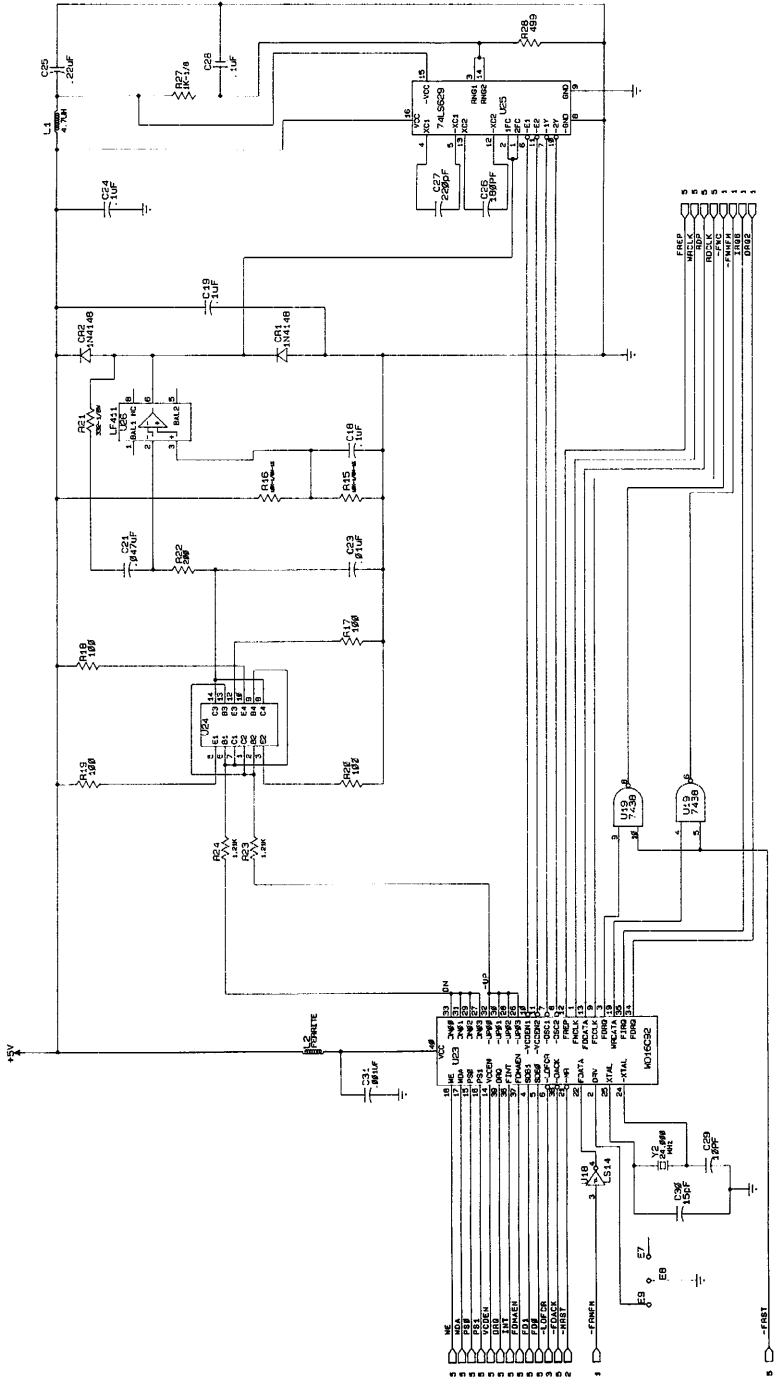
Fixed Disk and Diskette Drive Adapter - Level 1 (Sheet 9 of 9)



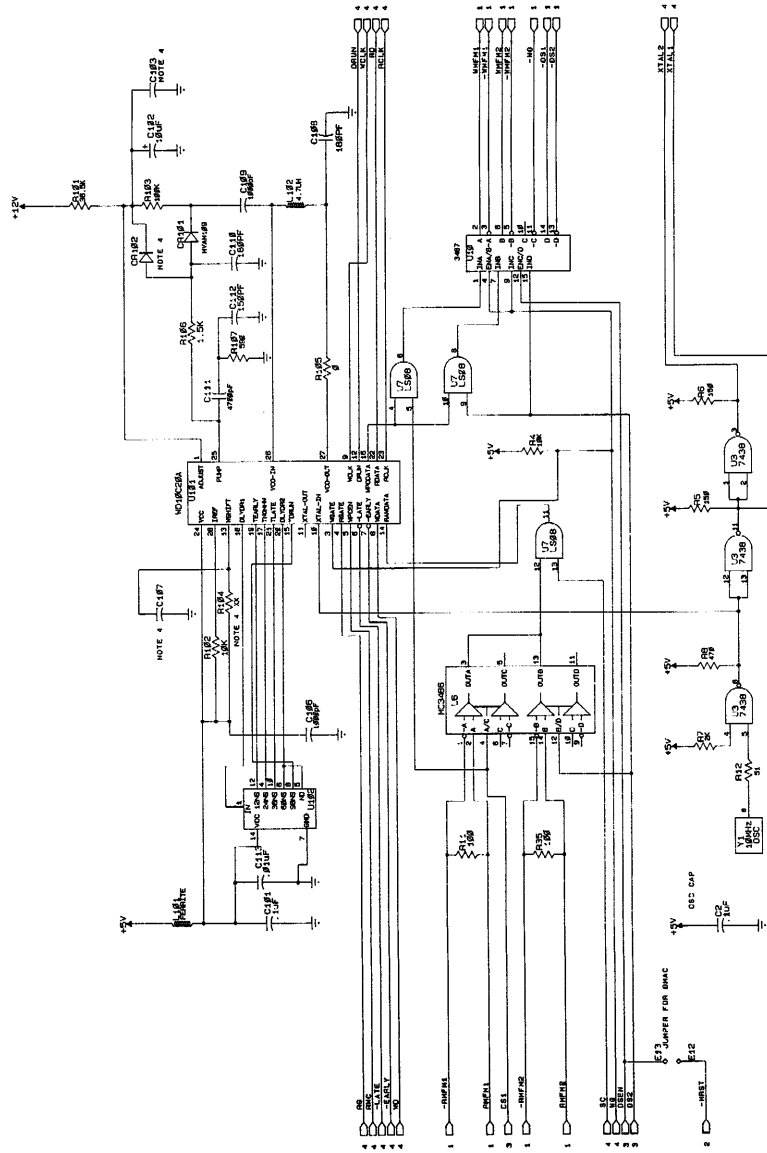
Fixed Disk and Diskette Drive Adapter-Level 2 (Sheet 2 of 7)



Fixed Disk and Diskette Drive Adapter-Level 2 (Sheet 3 of 7)



Fixed Disk and Diskette Drive Adapter-Level 2 (Sheet 6 of 7)



Fixed Disk and Diskette Drive Adapter-Level 2 (Sheet 7 of 7)

Notes:

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Index

C

command definitions,
diskette 19
 Format a Track 23
 Invalid 27
 Read a Track 22
 Read Data 19
 Read Deleted Data 20
 Read ID 22
 Recalibrate 25
 Scan Equal 23
 Scan High or Equal 25
 Scan Low or Equal 24
 Seek 27
 Sense Driver Status 26
 Sense Interrupt Status 26
 Specify 26
 Write Data 20
 Write Deleted Data 21
command register 6
command status register 0
 (ST0) 28
command status register 1
 (ST1) 29
command status register 2
 (ST2) 30
command status register 3
 (ST3) 31
command status registers 28
 Register 0 (ST0) 28
 Register 1 (ST1) 29
 Register 2 (ST2) 30
 Register 3 (ST3) 31
commands, diskette
 controller 15

symbol descriptions 16
controller, diskette 13
 diskette control
 register 14
 fixed disk register 14
cylinder number registers 4

D

data register 2
description 1
diagnostic mode 2
digital input register 12
digital output register 11
diskette command
 definitions 19
 Format a Track 23
 Invalid 27
 Read a Track 22
 Read Data 19
 Read Deleted Data 20
 Read ID 22
 Recalibrate 25
 Scan Equal 23
 Scan High or Equal 25
 Scan Low or Equal 24
 Seek 27
 Sense Driver Status 26
 Sense Interrupt Status 26
 Specify 26
 Write Data 20
 Write Deleted Data 21
diskette control register 14
diskette controller 13

- diskette control
 - register 14
- fixed disk register 14
- diskette controller
 - commands 15
 - controller command definitions 19
 - symbol descriptions 16
- diskette function 11
 - command status registers 28
 - controller commands 15
 - digital input register 12
 - digital output register 11
 - diskette controller 13
- drive/head register 5

E

- error register 2

F

- fixed disk function 1
 - fixed disk function 10
 - task file 1
 - task file registers 2
- fixed disk register 14
- Format a Track 23
- function, diskette 11
 - command status registers 28
 - controller commands 15
 - digital input register 12
 - digital output register 11
 - diskette controller 13
- function, fixed disk 1

- function, fixed disk 10
- task file 1
- task file registers 2
- functions 1
 - diskette 11

I

- interface lines 33
- Interfaces 32
 - interface lines 33
- Invalid 27

L

- Logic Diagrams 36

O

- operational mode 2

R

- Read a Track 22
- Read Data 19
- Read Deleted Data 20
- Read ID 22
- Recalibrate 25
- register, digital input 12
- register, digital output 11
- register, diskette control 14
- register, fixed disk 14

S

Scan Equal 23
Scan High or Equal 25
Scan Low or Equal 24
sector count register 4
sector number register 4
Seek 27
Sense Driver Status 26
Sense Interrupt Status 26
Specify 26
status register 5
status registers 28
 Register 0 (ST0) 28
 Register 1 (ST1) 29
 Register 2 (ST2) 30
 Register 3 (ST3) 31

T

task file 1
task file registers 2
 cylinder number
 registers 4
 data register 2
 drive/head register 5
 error register 2
 operational mode 2
 sector count register 4
 sector number register 4
 status register 5, 6
write precompensation
 register 3

W

Write Data 20
Write Deleted Data 21
write precompensation
 register 3

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August 5, 1986