F4164
65,536 x 1
Dynamic RAM

MOS Memory Products

Description

The F4164 is a dynamic Random Access Memory (RAM) circuit organized as 65,536 single-bit words. This memory uses the Fairchild advanced double poly NMOS, Isoplanar-H™ process which allows volume manufacture of reliable, high density memory products.

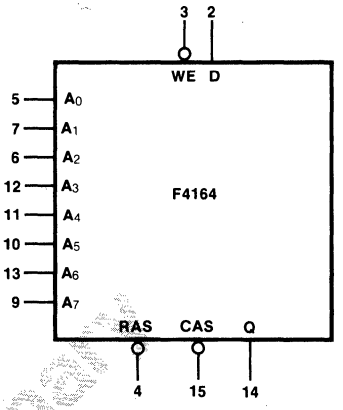
Innovative architecture and circuit design provide significant user benefits including wide operating margins, low power dissipation and excellent noise characteristics. Double cruciform architecture minimizes signal path lengths to improve noise margin and reduce propagation delays. A multiplexed sense amplifier scheme halves the number of sense amplifiers and the bit-line to cell capacitance ratio; this simultaneously reduces power consumption and improves signal sensing margins. Full-sized reference cells provide good margins and control. Low capacitance TTL-compatible inputs with overshoot and anti-static protection insure data and address input integrity.

- **INDUSTRY STANDARD 16-PIN DIP WITH PIN 1 NOT CONNECTED (NC)**
- **LOW CAPACITANCE TTL-COMPATIBLE INPUTS WITH OVERSHOOT AND ANTI-STATIC PROTECTION**
- **COMMON I/O CAPABILITY**
- **STANDARD 5 V ±10% SINGLE POWER SUPPLY REQUIREMENT**
- **LOW POWER**
  209 mW ACTIVE (MAX)
  19.3 mW STANDBY (MAX)
- **FAST ACCESS TIME — 120 ns, 150 ns or 200 ns**
- **READ-MODIFY-WRITE, RAS-ONLY REFRESH AND PAGE MODE CAPABILITY**
- **OUTPUT UNLATCHED AT CYCLE END ALLOWS FOR PAGE BOUNDARY EXTENSION AND TWO-DIMENSIONAL CHIP SELECTION**

Pin Names

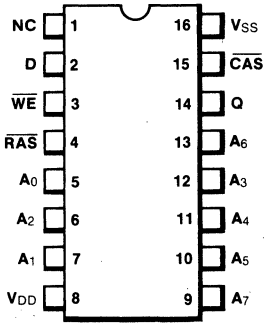
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D	Data Input
Q	Data Output

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8

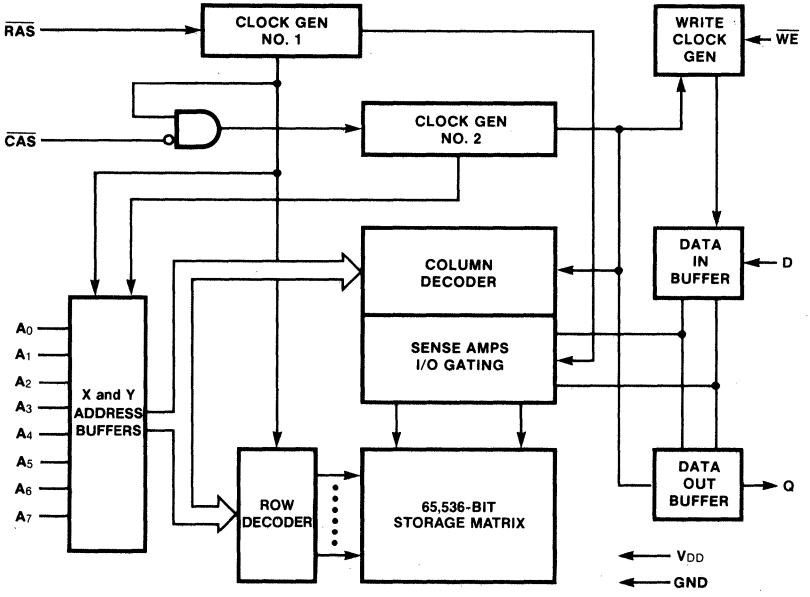
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	WC	D

Block Diagram



Functional Description

Memory Cycles

The F4164 operates in several modes which reflect various application considerations, some examples of which follow.

Random Read or Write Cycle

This mode implements standard Read or Write operation. Addresses are entered in two consecutive 8-bit bytes synchronized with $\overline{RAS}$ and $\overline{CAS}$. In the Read case, $\overline{WE}$ should be HIGH before the falling edge of $\overline{CAS}$. During Early-Write operations, $\overline{WE}$ falls before $\overline{CAS}$, causing the output to remain in the high impedance state. This output mode is useful if the RAM Data input (D) and Data output (Q) pins are to be wired in common as a bidirectional data bus.

Read-Write Cycle

The Read-Write mode is used when new data is to be written into the same cell location from which the content is currently being read. Since no address change is required, this mode provides a much faster Read-Write cycle by allowing the overhead associated with the address decoder and precharge to be amortized over two operations. In general, t_{RWC} is significantly less than twice t_{RC}. In this mode the new input data is not a function of the currently stored data. For that reason the cycle time is not limited by access time (t_{RAC}), but by Write considerations such as t_{RWD} and t_{RWL}.

Read-Modify-Write Cycle

The Read-Modify-Write cycle is used when the data from the cell at the current address is used to derive new data for writing back into that cell, such as in error correction schemes. In this mode, cycle time is dependent upon both read access time and write-related parameters.

Addressing

The 16 address bits required to decode one-of-65,536 storage cell locations in the F4164 are entered using a two-phase multiplexing operation. First, the 8-bit row address is applied to the eight Address inputs of the F4164 and latched into the chip by Row Address Strobe ($\overline{RAS}$). Next, the 8-bit column address is presented to the Address inputs and latched by the Column Address Strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ or $\overline{CAS}$.

$\overline{CAS}$ is internally inhibited by a signal derived from $\overline{RAS}$. This feature prevents column addresses from being strobed onto the chip before row address dependent operations have been completed.

The gated-$\overline{CAS}$ feature allows $\overline{CAS}$ to occur any time before $t_{RCD(max)}$ with no effect on the worst-case access time (t_{RAC}). No errors will result if $\overline{CAS}$ is applied to the F4164 after the $t_{RCD(max)}$ limit, but access time will then be determined from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}).

Page Mode Operation
Higher speed and lower power operations can be performed in Page Mode on bits sharing a Row Address. In this mode $\overline{RAS}$ strobes in the common Row Address and is then kept LOW (active) while successive $\overline{CAS}$ cycles allow the required Column Addresses to be strobed in for subsequent Read or Write operations. Data from the first bit addressed is accessed within t_{RAC} (or $t_{RCD} + t_{CAC}$ if $t_{RCD} > t_{RCD(max)}$) and subsequent Column Addresses are accessed within t_{CAC} only.

Both the delays and the dynamic power dissipation associated with row selection and sensing occur only once with the initial $\overline{RAS}$ transition. Thereafter, delays and dynamic power dissipation are incurred only in the column select and data path. The delay and power in the row and sensing circuitry are amortized over 256 different Column Addresses offering improved speed and lower power per bit.

Page Mode address boundaries may be extended by multiplexing $\overline{CAS}$ to several devices which share a common Data output (Q) bus.

Data Input
In a Write operation, the data to be written is latched into the chip while $\overline{RAS}$ is LOW by a combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$). The strobe is enabled by the last of these two signals to go LOW. This allows several types of write cycles to be performed. In an Early-Write cycle ($\overline{WE}$ LOW before $\overline{CAS}$ goes LOW), the Data input (D) is strobed by $\overline{CAS}$. Here data set-up and hold times are referenced to $\overline{CAS}$. If D is not yet valid at the time $\overline{CAS}$ becomes active, or if a Read-Write or Read-Modify-Write cycle is desired, then $\overline{WE}$ must be delayed. In this "late-write" mode, the data set-up and hold times are referenced to $\overline{WE}$ rather than $\overline{CAS}$.

Data Output
The Data output (Q) buffer assumes a high impedance state whenever $\overline{CAS}$ is HIGH (inactive) subject to $t_{OFF(max)}$. If the cycle being performed is a Read, Read-Modify-Write, or a "late-write" cycle, then the Q latch and buffer will remain high impedance until the access time, after which Q will assume the value of the data read from the selected cell. This output data is of the same polarity as the input data and will remain valid as long as $\overline{CAS}$ is kept LOW (active). However, if the operation is an Early-Write, or if the chip does not receive both $\overline{RAS}$ and $\overline{CAS}$, then Q will remain high impedance throughout the cycle. This feature allows systems which write exclusively in the Early-Write mode to connect D and Q directly together.

Since both $\overline{RAS}$ and $\overline{CAS}$ must be supplied for a device to be "active", a reduction in external decoding logic can be realized by using $\overline{RAS}$ and $\overline{CAS}$ in a 2-dimensional decoding/selection scheme. An analogous method can be used to extend the page boundary to beyond 256 locations by decoding which device receives a $\overline{CAS}$ in addition to the $\overline{RAS}$ already latched into the chips. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ will respond with a valid memory cycle (see Table 1).

Table 1 $\overline{RAS}$ and $\overline{CAS}$ Clock Conditions

$\overline{RAS}$ and $\overline{CAS}$ cycle	Device active
$\overline{RAS}$-only cycle	Device deselected, refresh
$\overline{CAS}$-only cycle	Device deselected
Neither $\overline{RAS}$ nor $\overline{CAS}$	Device deselected, standby

Refresh
Refresh of the data stored in the dynamic cell matrix of the F4164 is accomplished by performing a memory cycle at each of the 256 row addresses at least every 4 ms. Performing a $\overline{RAS}$-only Refresh with $\overline{CAS}$ held HIGH causes the output buffer to remain in the high-impendence state throughout the cycle.

The F4164 256-cycle, 4 ms refresh timing requirement is compatible with distributed refresh techniques currently utilized for 128-cycle, 2 ms refresh 16K dynamic RAMs.

Absolute Maximum Ratings

Voltage on Any Pin with Respect to V_{SS}	−1.0 V to +7.0 V
V_{DD} Supply with Respect to V_{SS}	−1.0 V to +7.0 V
Storage Temperature	−65°C to +150°C
Power Dissipation	1.0 W
Short-Circuit Output Current	50 mA
Operating Temperature	0°C to +70°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (Note)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	4.5		5.5	V
V_{SS}		0		0	V
V_{IH}	Input HIGH Voltage	2.4		6.5	V
V_{IL}	Input LOW Voltage, All Inputs	−1.0		0.8	V

DC Characteristics Recommended operating conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −5.0 mA
I_{DD1}	Operating Current Average Power Supply Current		27	38	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min; Q = no connection
I_{DD2}	Standby Current Power Supply Current			3.5	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
I_{DD3}	Refresh Current Average Power Supply Current		21	32	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min, Q = no connection
I_{DD4}	Page Mode Current Average Power Supply Current		15	30	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{CP} = Min, Q = no connection
I_{IL}	Input Leakage Current	−10		10	μA	Any Input, 0 V ≤ V_{IN} ≤ 6.5 V; all other pins not under test = 0 V
I_{OL}	Output Leakage Current	−10		10	μA	Data Out is disabled, 0 V ≤ V_{OUT} ≤ 6.5 V

Capacitance T_A = +25°C

Symbol	Characteristic	Min	Typ	Max	Unit
C_{IN1}	Input Capacitance A_0-A_7, D			5.0	pF
C_{IN2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			10	pF
C_{OUT}	Output Capacitance Q			7.0	pF

Note

All Voltages are referenced to V_{SS}. Conditions apply over the entire operating temperature range.

AC Characteristics Recommended operating conditions unless otherwise noted (Notes 1, 2, and 3)

IEEE Symbol[9]	Symbol	Characteristic	F4164-1		F4164-2		F4164-3		Unit	Note
			Min	Max	Min	Max	Min	Max		
TRVRV	t_{REF}	Time between Refresh		4.0		4.0		4.0	ms	
TRELREL	t_{RC}	Random Read/Write Cycle Time	300		320		330		ns	
TRELREL	t_{RWC}	Read-Write Cycle Time	315		335		375		ns	
TCELCEL	t_{PC}	Page Mode Cycle Time	160		170		225		ns	
TRELQV	t_{RAC}	Access Time from $\overline{RAS}$		120		150		200	ns	4, 6
TCEHQV	t_{CAC}	Access Time from $\overline{CAS}$		80		100		135	ns	5, 6
TCEHQZ	t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	0	50	ns	
TT	t_T	Transition Time	3.0	35	3.0	35	3.0	50	ns	
TREHREL	t_{RP}	$\overline{RAS}$ Precharge Time	80		100		120		ns	
TRELREH	t_{RAS}	$\overline{RAS}$ Pulse Width	120	10K	150	10K	200	10K	ns	
TCELREH	t_{RSH}	$\overline{RAS}$ Hold Time	80		100		135		ns	
TCEHCEL	t_{CP}	$\overline{CAS}$ Precharge Time	60		60		80		ns	
TCELCEH	t_{CAS}	$\overline{CAS}$ Pulse Width	80	10K	100	10K	135	10K	ns	
TRELCEH	t_{CSH}	$\overline{CAS}$ Hold Time	120		150		200		ns	
TRELCEL	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	40	30	50	35	65	ns	7
TCEHREL	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
TARVREL	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
TRELARX	t_{RAH}	Row Address Hold Time	15		20		25		ns	
TACVCEL	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
TCELACX	t_{CAH}	Column Address Hold Time	40		45		55		ns	
TRELACX	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	80		95		120		ns	
TWHCEL	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
TCEHWL	t_{RCH}	Read Command Hold Time	0		0		0		ns	
TWLCEL	t_{WCS}	Write Command Set-up Time	0		−10		−10		ns	8
TCELWH	t_{WCH}	Write Command Hold Time	40		45		55		ns	
TRELWH	t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	80		95		120		ns	
TWLWH	t_{WP}	Write Command Pulse Width	40		45		55		ns	
TWLREH	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		70		80		ns	
TWLCEH	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		70		80		ns	

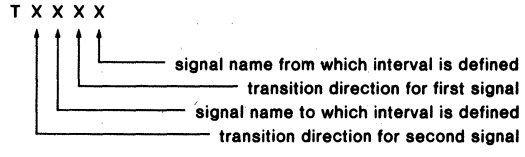
Notes on following page.

AC Characteristics (Continued)

IEEE Symbol[9]	Symbol	Characteristic	F4164-1		F4164-2		F4164-3		Unit	Note
			Min	Max	Min	Max	Min	Max		
TDVREL	t_{DS}	Data In Set-up Time	0		0		0		ns	
TCELDX	t_{DH}	Data In Hold Time	40		45		55		ns	
TRELDX	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	80		95		120		ns	
TCELWL	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		70		95		ns	8
TRELWL	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		160		ns	8

Notes

1. Several cycles are required after power up before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.
2. Dynamic measurements assume $t_T = 5$ ns.
3. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. Refer to test conditions.
7. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating characteristics due to the following. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data output pin will be open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$, the cycle is a read-write cycle and Data output will contain data read from the selected cell. If neither of the conditions is satisfied the condition of the Data output is indeterminate.
9. **Timing Parameter Abbreviations**
   All timing abbreviations in this format use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a 'from-to' sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



The signal definitions used in this data sheet are:

RE = $\overline{RAS}$, CE = $\overline{CAS}$
AR = Row Address
AC = Column Address

A = Address
D = Data In
Q = Data Out
W = Write Enable

The transition definitions used in this data sheet are:

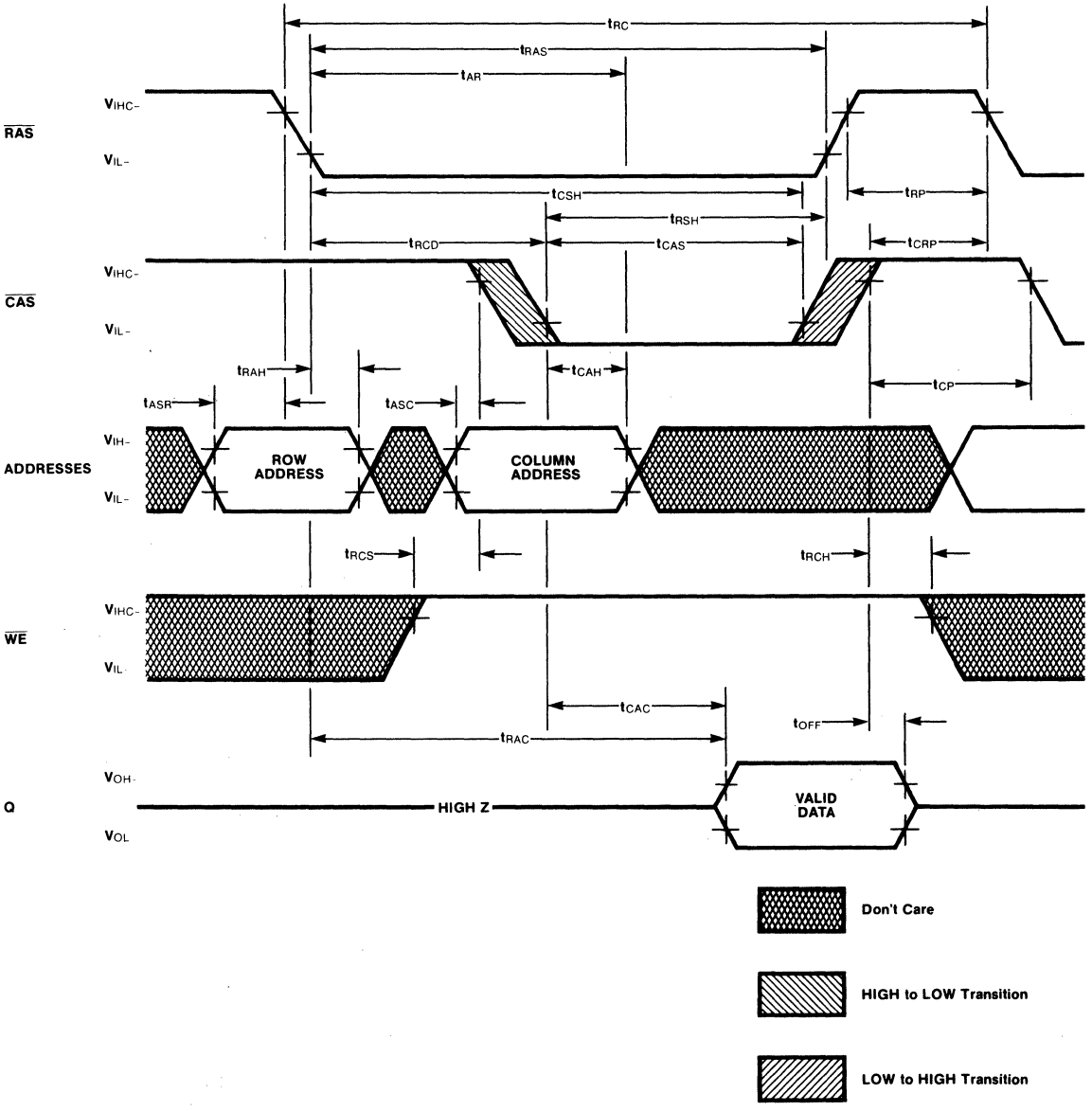
H = transition to HIGH
L = transition to LOW
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

Timing Limits

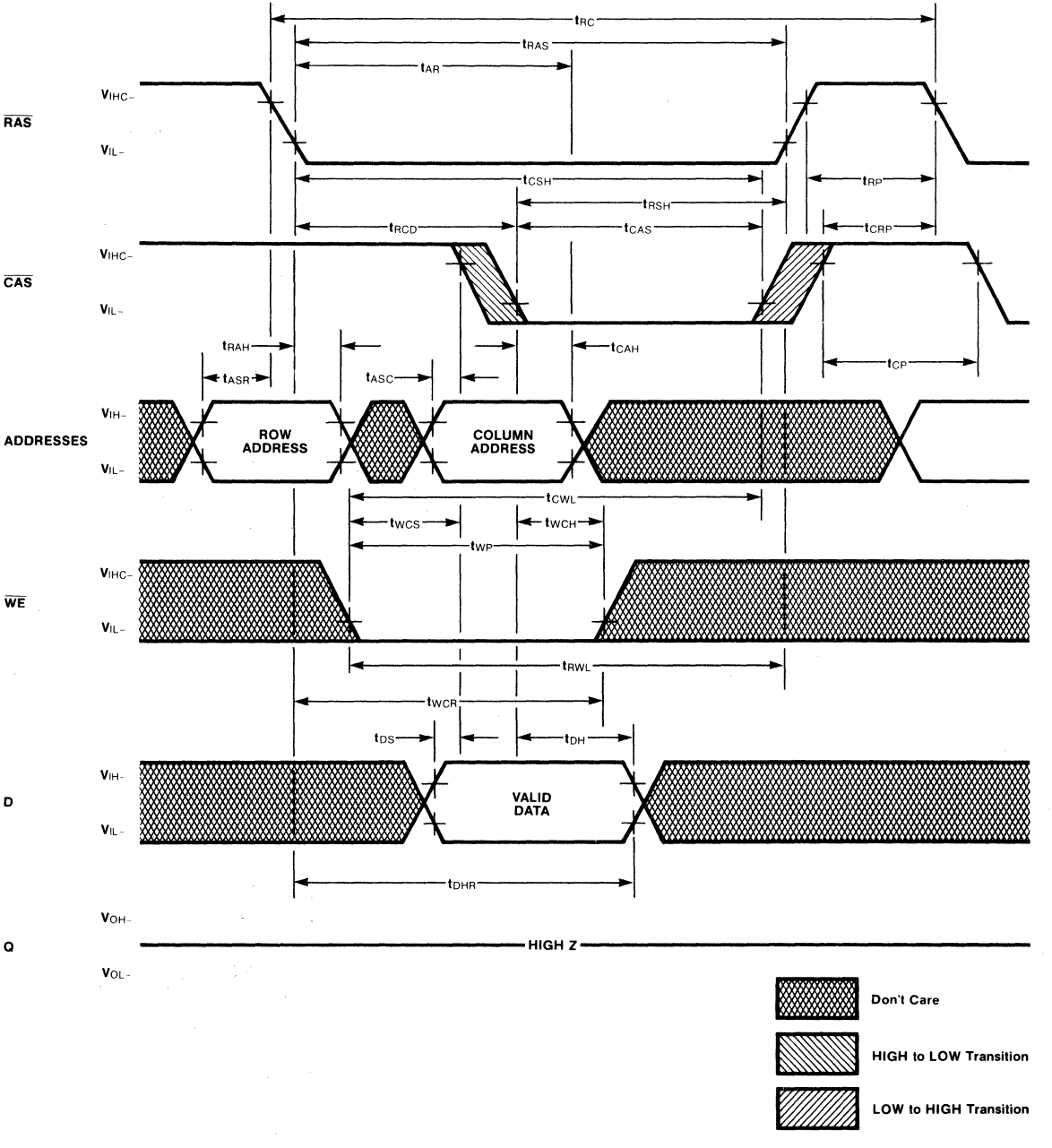
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Timing Diagrams

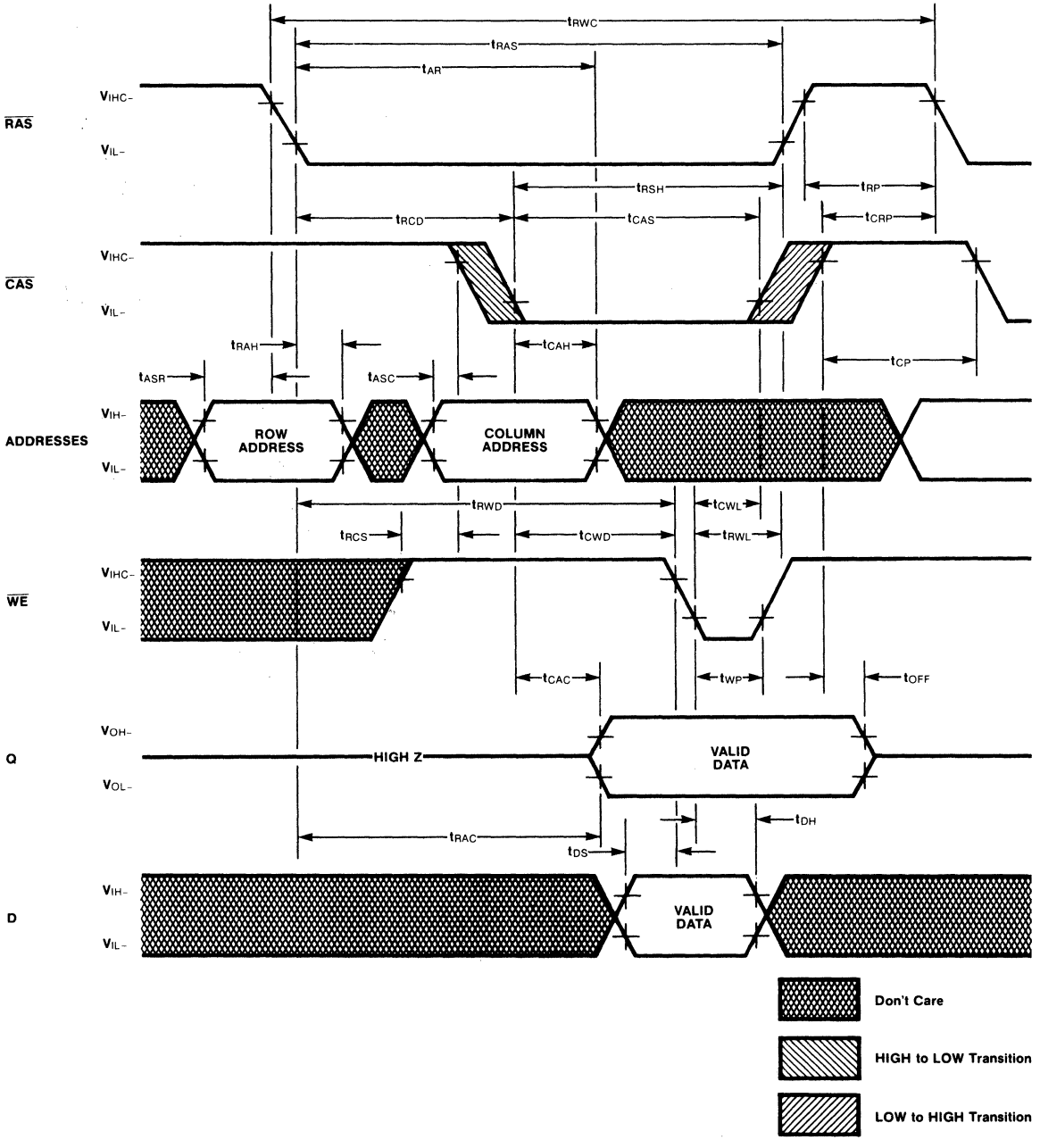
Read Cycle Timing Diagram



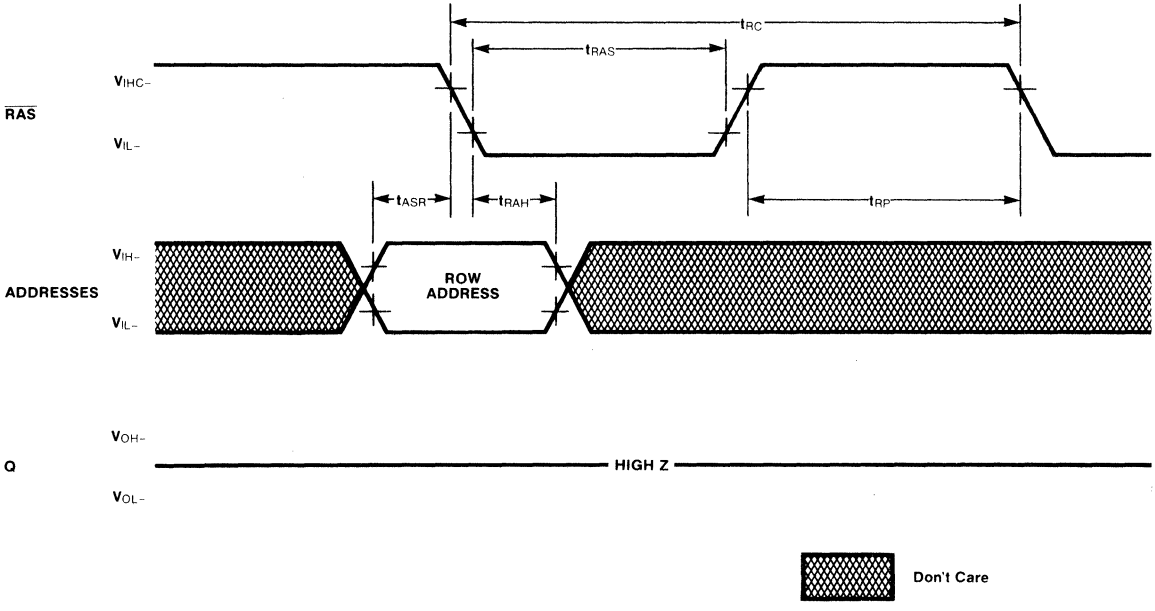
Write Cycle (Early Write)



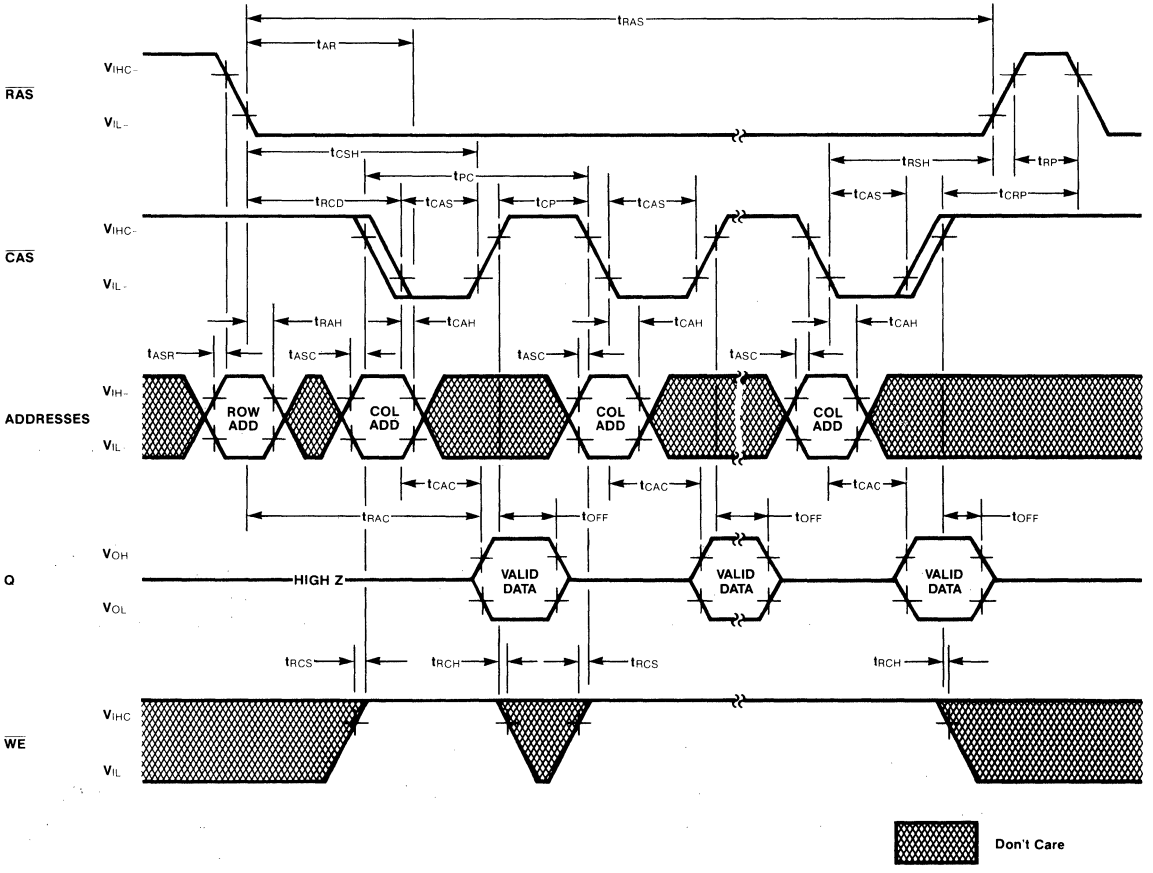
Read-Write/Read-Modify-Write Cycle



"$\overline{\text{RAS}}$-only" Refresh Cycle



Page Mode Read Cycle



Page Mode Write Cycle