GM71C256A

262,144 WORDS × 1 BIT
CMOS DYNAMIC RAM

Description

The GM71C256A is the new generation dynamic RAM organized 262,144 × 1 Bit. GM71C256A has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C256A offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C256A to be packaged in a standard 16 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

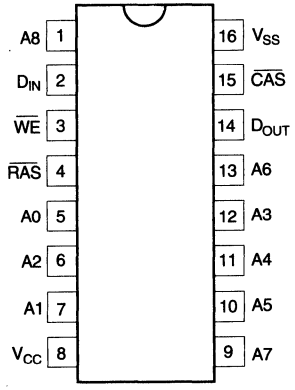
Features

- 262,144 × 1 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C256A-70	70	15	130	50
GM71C256A-80	80	20	145	55
GM71C256A-10	100	25	175	60

- Low Power
  Active: 385/330/275 mW (MAX)
  Standby: 16.5 mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and output TTL Compatible
- 256 Refresh Cycles/4 ms

Pin Configuration
16 DIP



Pin Description

Pin	Function	Pin	Function
A0 ~ A8	Address Inputs	D_{IN}	Data Input
$\overline{RAS}$	Row Address Strobe	D_{OUT}	Data Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable	V_{SS}	Ground

Ordering Information

Type No.	Access Time	Package
GM71C256A-70	70ns	300 Mil
GM71C256A-80	80ns	16 Pin
GM71C256A-10	100ns	Plastic DIP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	70ns	—	70	mA	1,2
		80ns	—	60		
		100ns	—	50		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		—	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	70ns	—	70	mA	2
		80ns	—	60		
		100ns	—	50		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	70ns	—	45	mA	1,3
		80ns	—	40		
		100ns	—	35		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V, D_{OUT} = High-Z)		—	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	70ns	—	70	mA	
		80ns	—	60		
		100ns	—	50		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	4	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 6.5V$)		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 6.5V$)		−10	10	μA	

Note 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address, D_{IN})	—	4	pF	1
C_{I2}	Input Capacitance (Clocks)	—	5	pF	1
C_O	Data Capacitance (D_{OUT})	—	6	pF	1,2

Note 1. Capacitance is sampled and not 100% tested.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C, Note 1,14)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	145	—	175	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	55	—	65	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	75,000	80	75,000	100	75,000	ns	
$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75,000	20	75,000	25	75,000	ns	
$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	20	—	25	—	30	—	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	60	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	ns	9
$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15	—	20	—	25	—	ns	
$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	25	—	25	—	30	—	ns	
t_{AR}	Column Address Hold Time from $\overline{RAS}$	55	—	60	—	70	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	15	—	ns	
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	7
t_{REF}	Refresh Period	—	4	—	4	—	4	ms	

Read Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	35	—	40	—	45	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	5	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	0	15	0	20	0	25	ns	6

Write Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	—	60	—	70	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	20	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	30	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11
t_{DHR}	Data-in Hold Time Referenced to $\overline{RAS}$	55	—	60	—	70	—	ns	

Read-Modify-Write Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	155	—	175	—	210	—	ns	
t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	95	—	110	—	135	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	—	80	—	100	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	—	20	—	25	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	35	—	40	—	45	—	ns	10

Refresh Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	20	—	25	—	30	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	50	—	55	—	60	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	15	—	15	—	20	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	75,000	—	75,000	—	75,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	45	—	50	—	55	ns	13

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	75	—	85	—	95	—	ns	

Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{CWD} and t_{RWD}, t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, the cycle is a read-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or Read-modify-Write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

TIMING WAVEFORMS

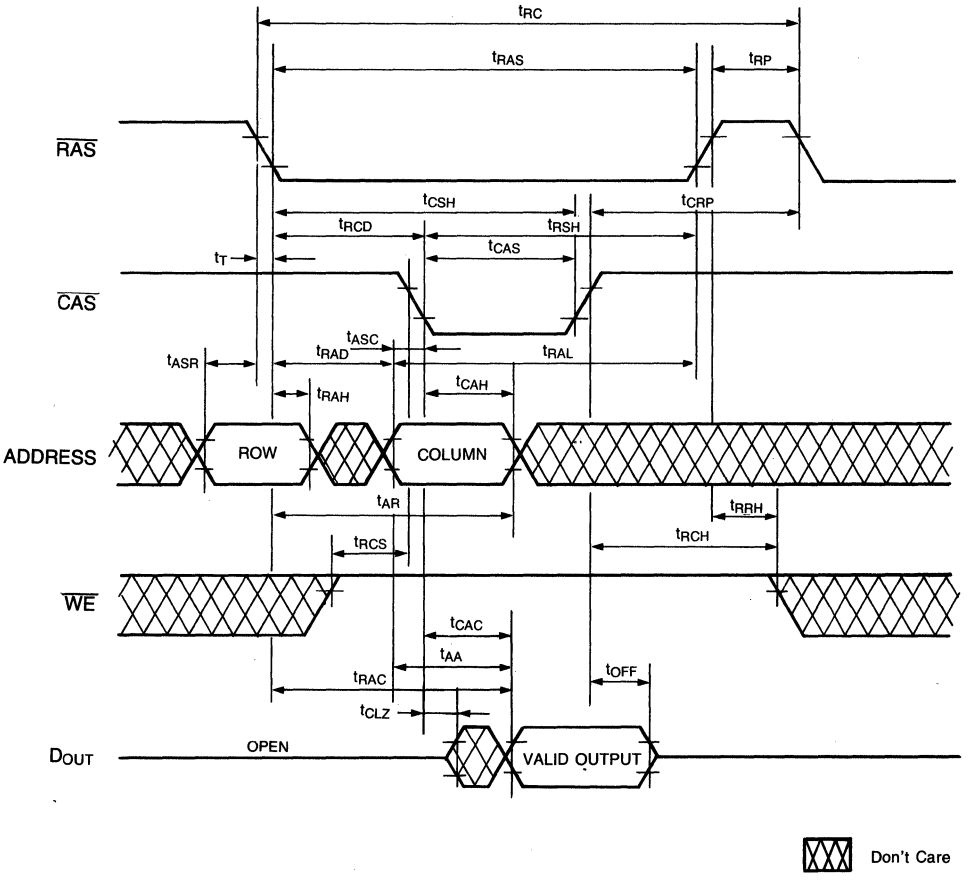


FIGURE 1. READ CYCLE

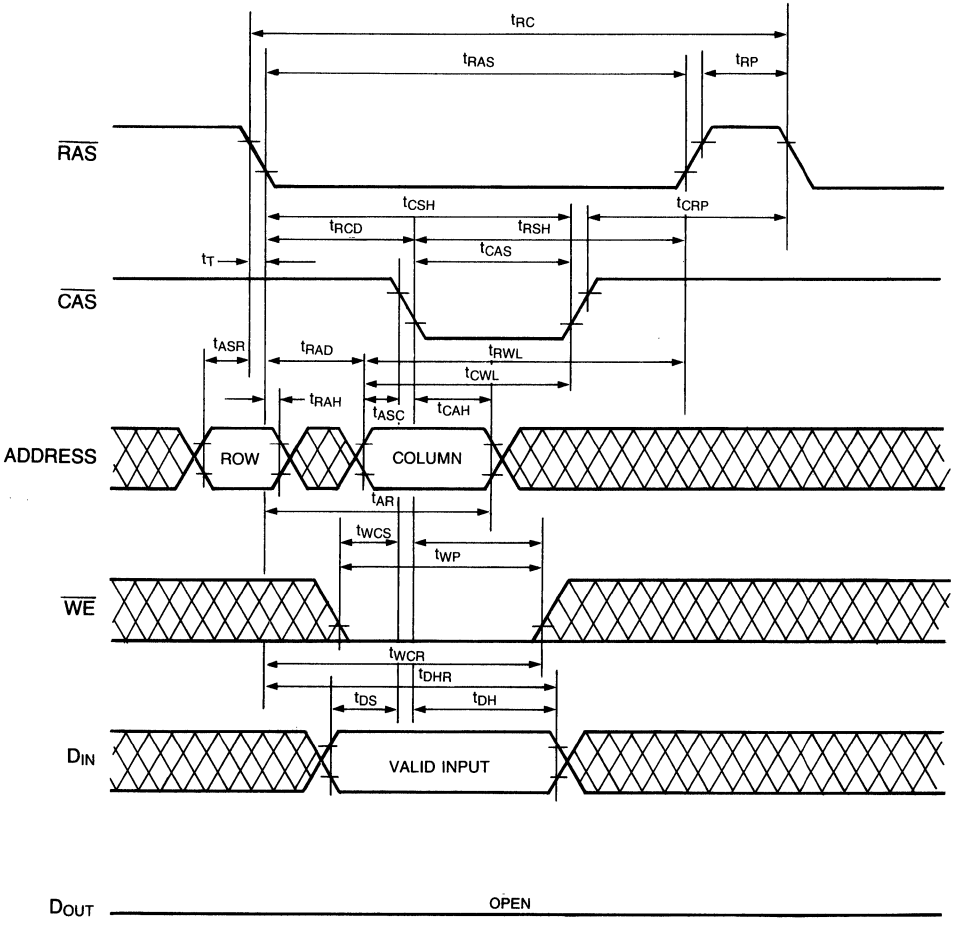


FIGURE 2. EARLY WRITE CYCLE

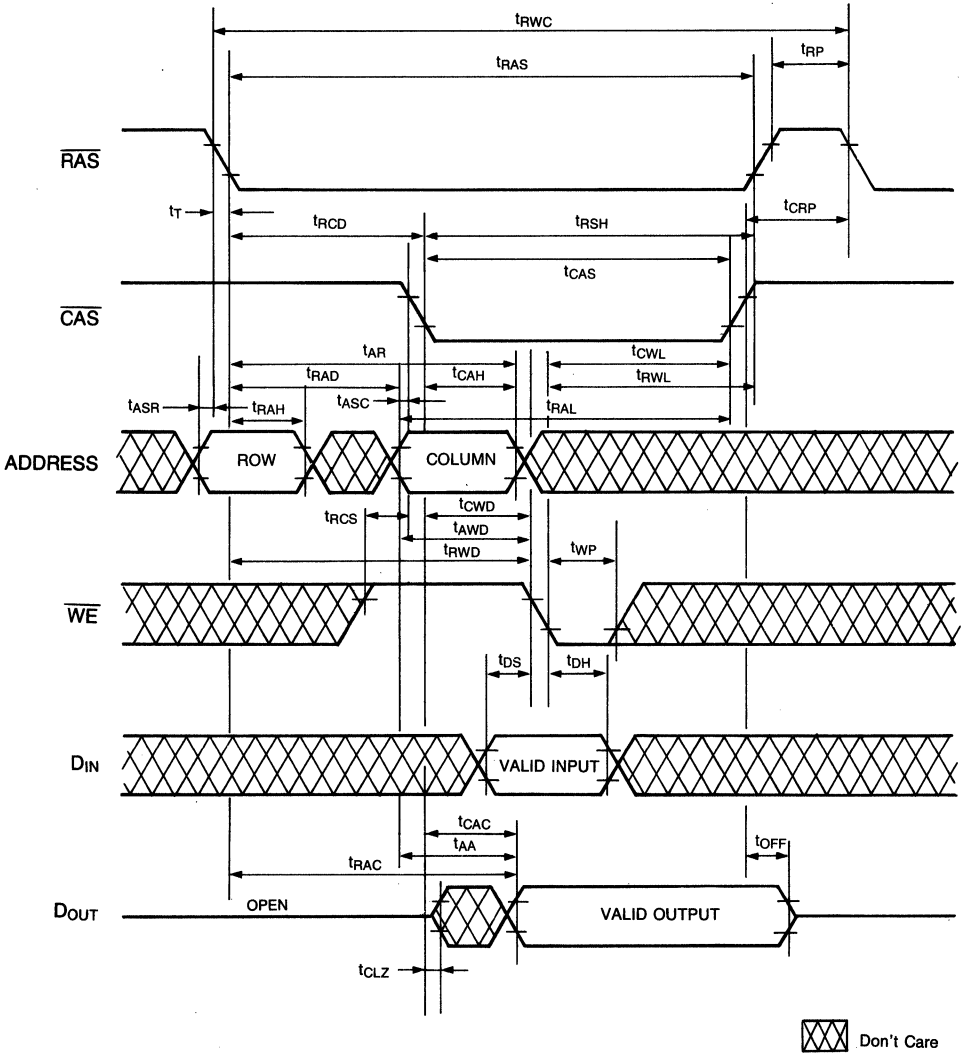


FIGURE 3. READ-MODIFY-WRITE CYCLE

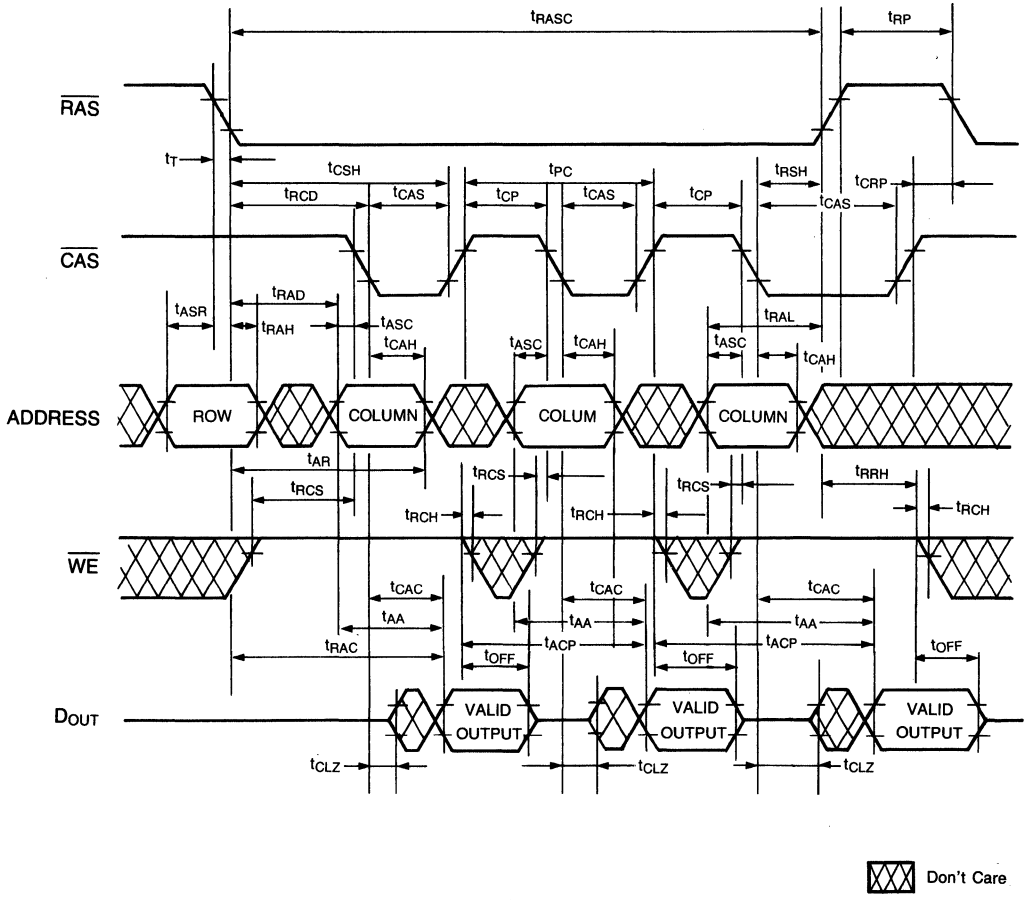


FIGURE 4. FAST PAGE MODE READ CYCLE

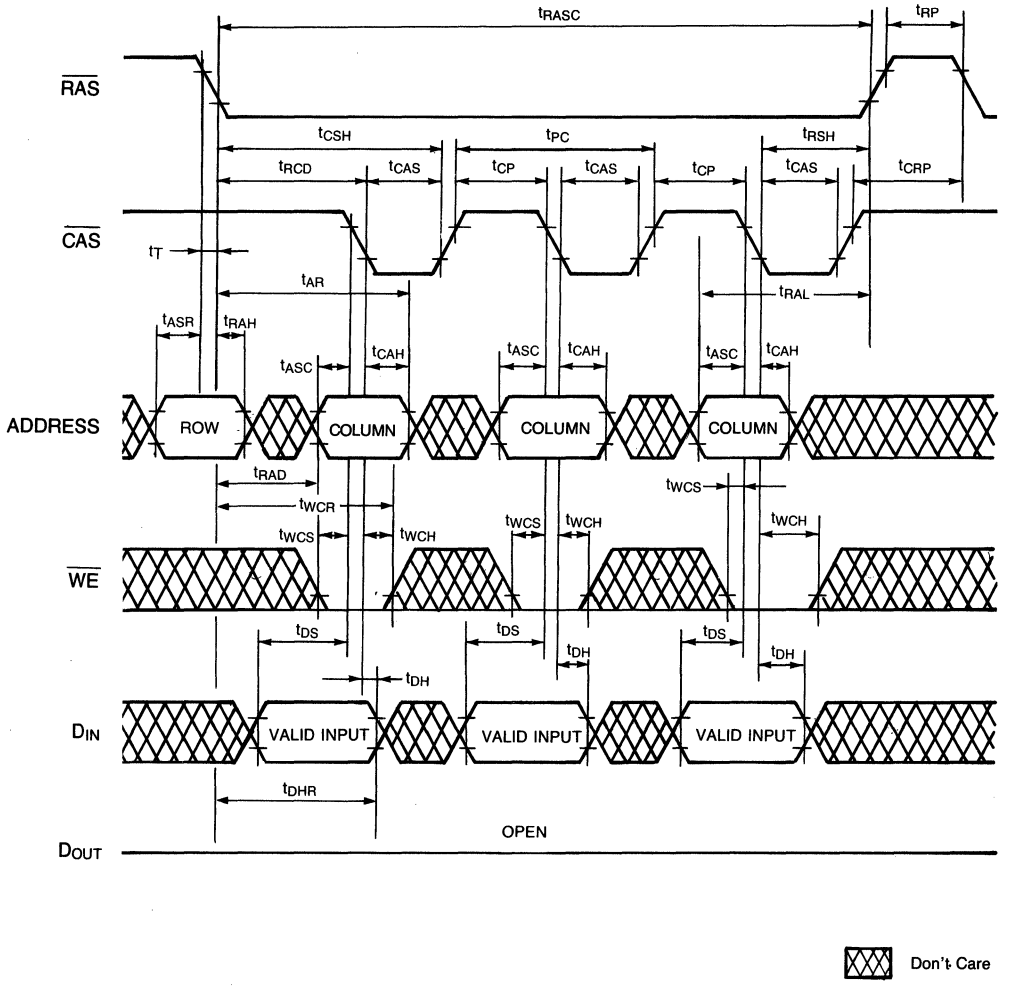


FIGURE FAST PAGE MODE WRITE CYCLE

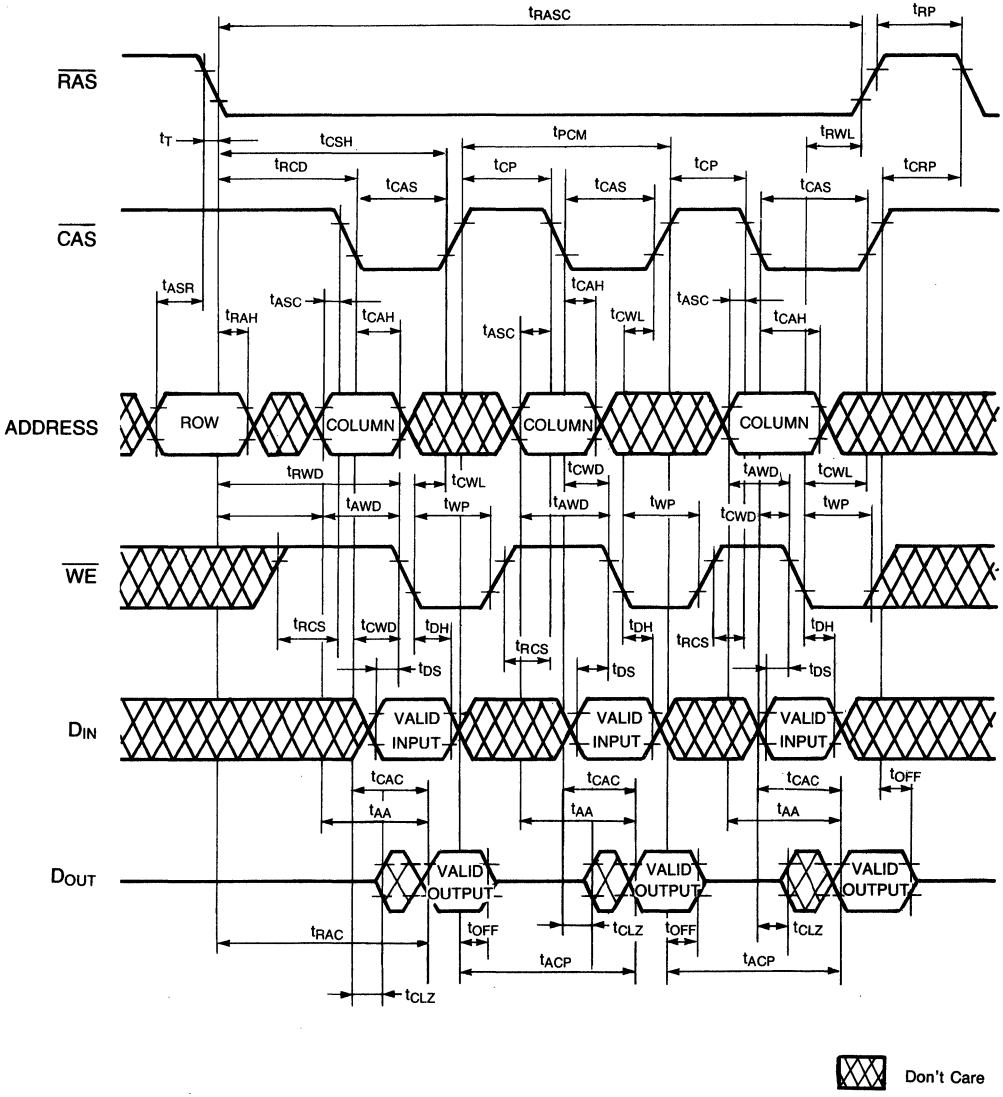


FIGURE FAST PAGE MODE READ-MODIFY-WRITE CYCLE

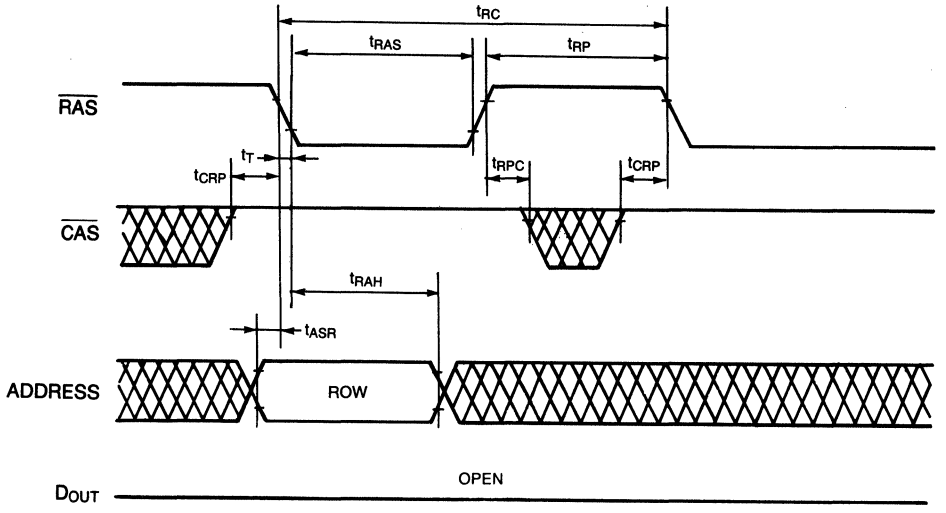


FIGURE 7. RAS-ONLY-REFRESH CYCLE

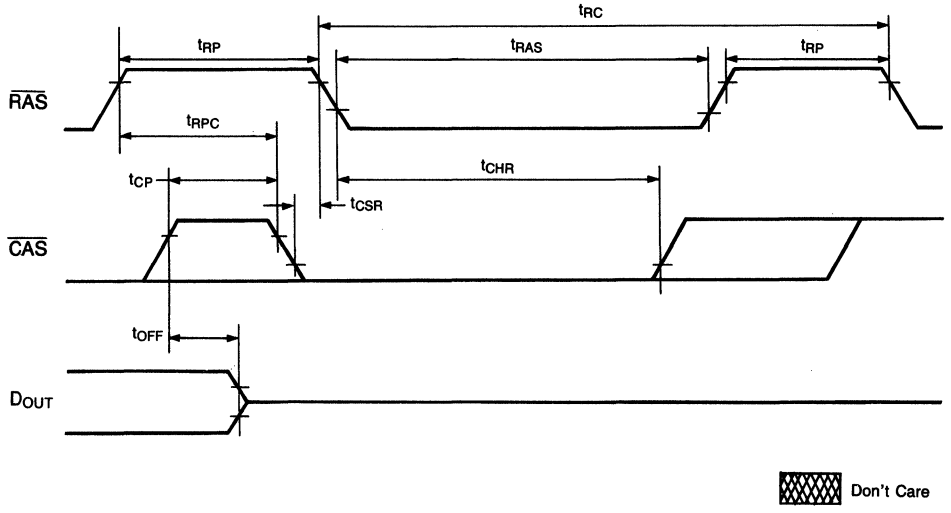


FIGURE 8. CAS BEFORE RAS REFRESH CYCLE

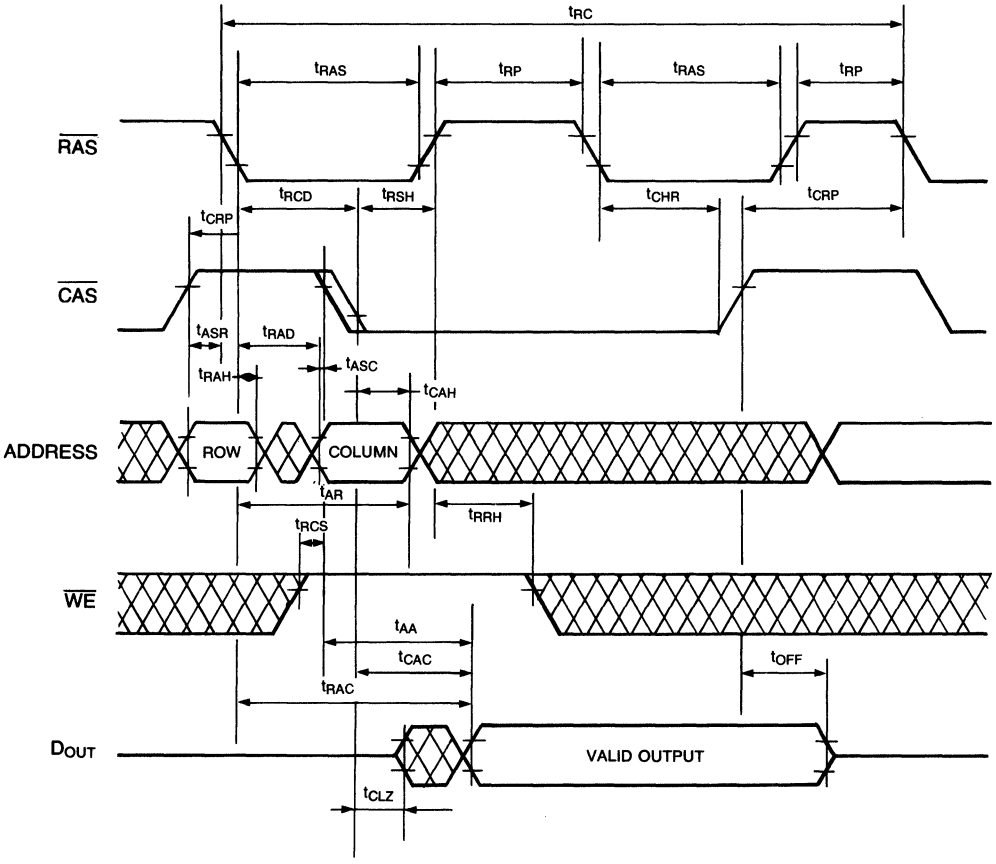


FIGURE 9. HIDDEN REFRESH CYCLE (READ)

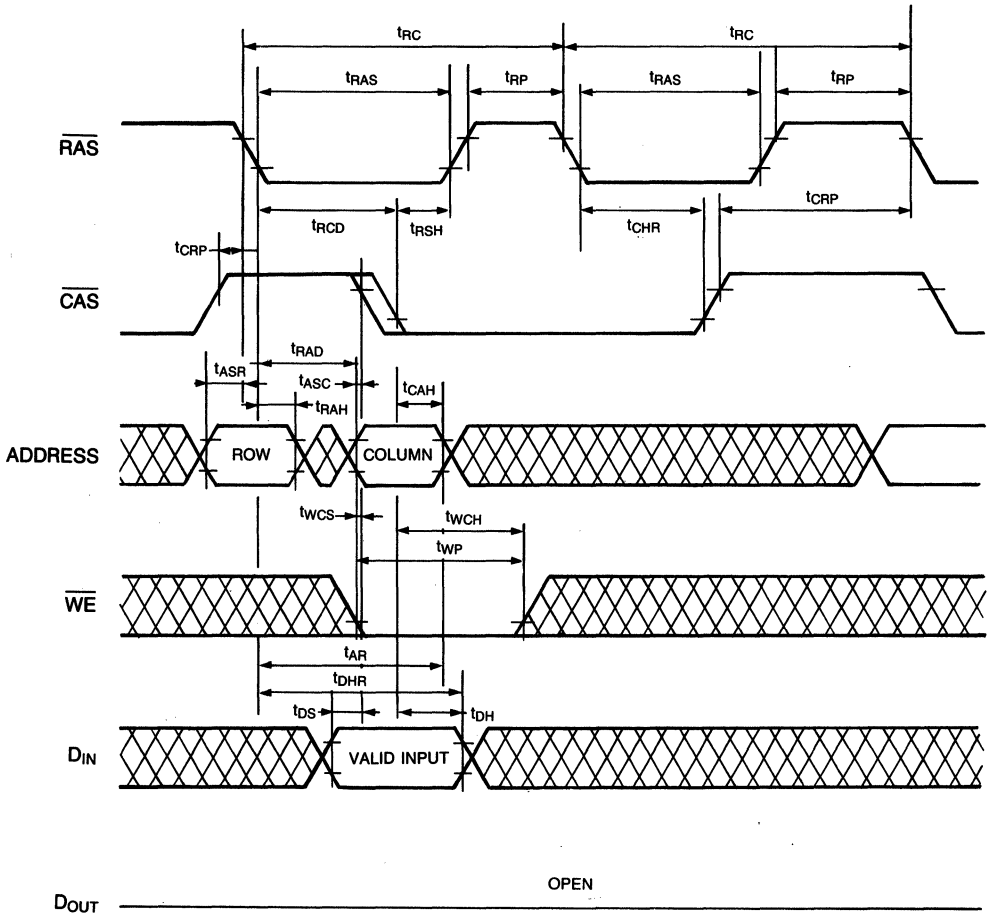


FIGURE 10. HIDDEN REFRESH CYCLE (WRITE)

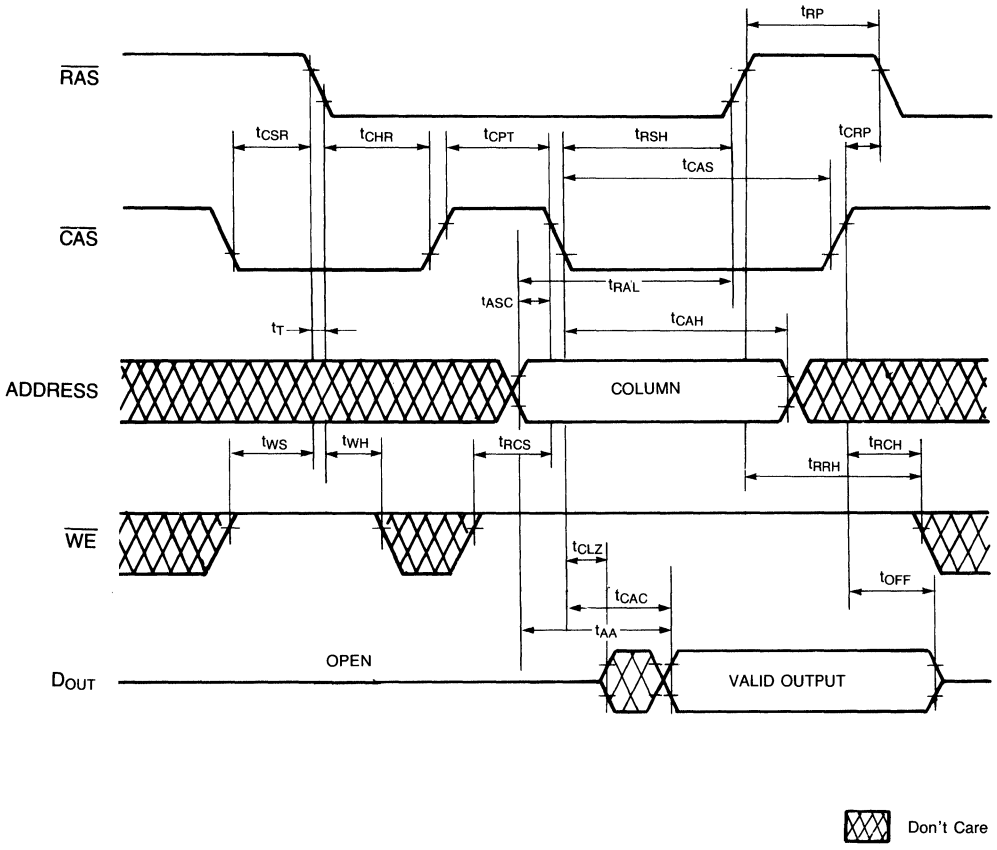


FIGURE 11. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

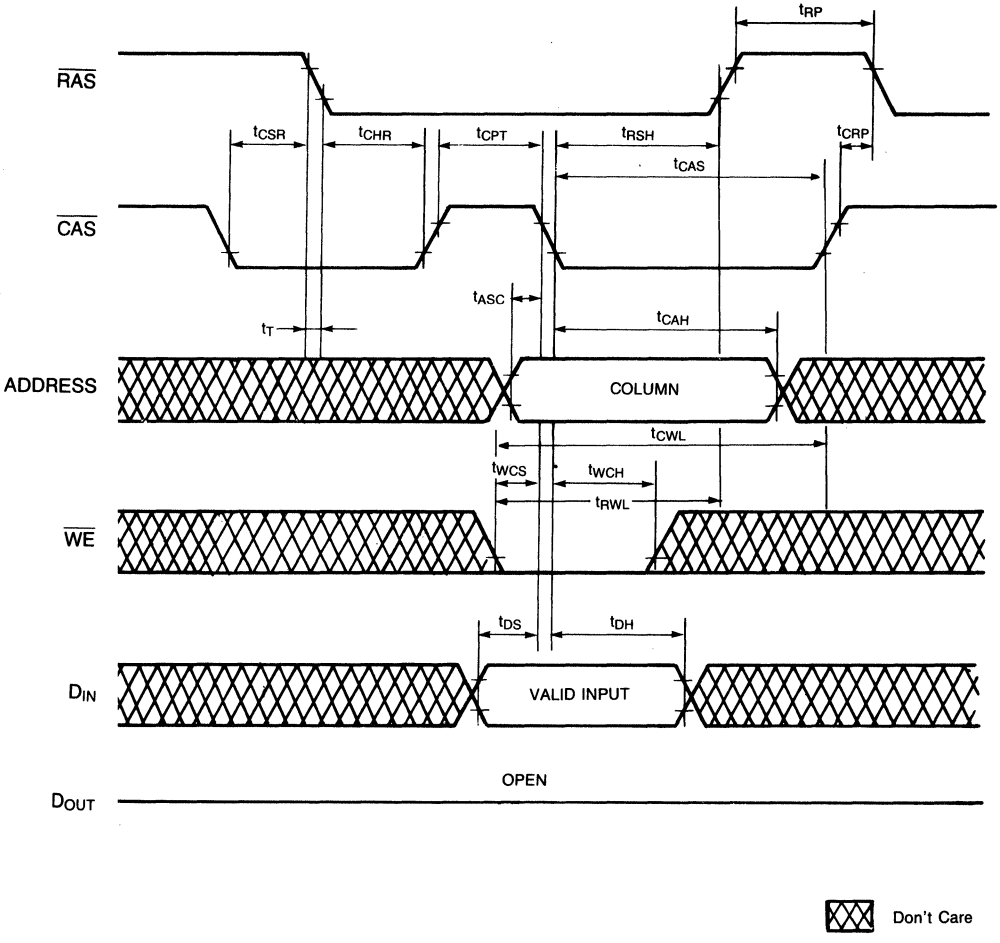


FIGURE 12. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER CHECK CYCLE (WRITE)

Package Dimensions

16 DIP

Unit: inches (mm)