SHARP SERVICE MANUAL

CODE: 00ZPC4741SM-E

PERSONAL COMPUTER

PC-4741
PC-4721
MODEL PC-4702

CONTENTS

SHARP CORPORATION

CHAPTER 1. OVERVIEW

1. Scope

This manual is covered for PC4702, PC4721, PC4741 CPU and hard disk drive.

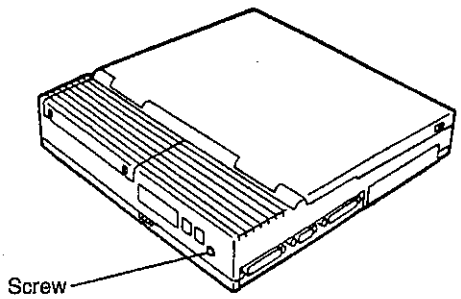
For detailed information on other auxiliary equipment and options (list following), please refer to the separate service manuals provided for each devices.

- CRT adaptor (CE-471A)
- MFD unit (CE-452F)
- EMS card (CE-471B)
- SIO card (CE-451B)

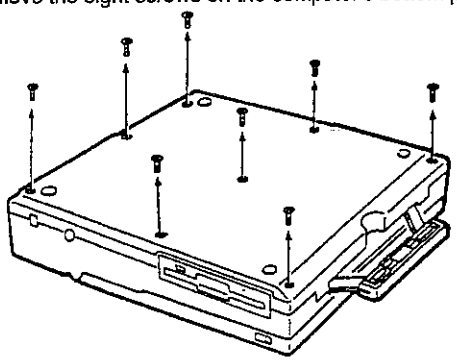
2. Service method

1) Cabinet Top Removal

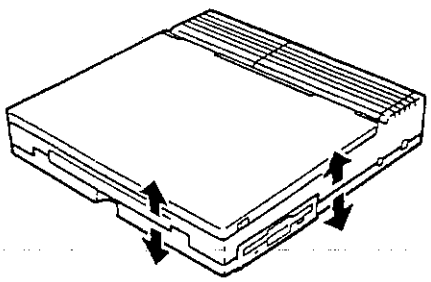
1. Before disassembly, remove the AC adaptor and the built-in lead battery.
   If the CRT board, the modem board, or the SIO board is installed, locate the face plate screw fastened to the computer and remove.



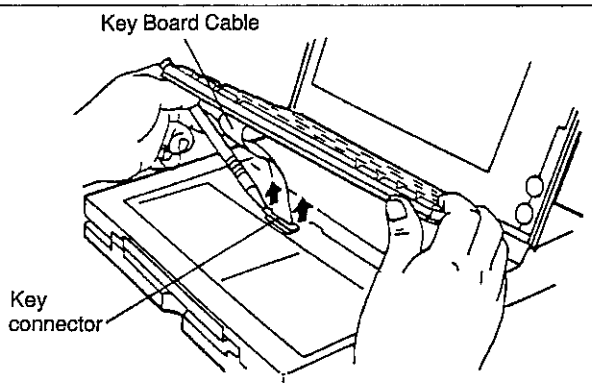
2. Remove the eight screws on the computer's bottom panel.



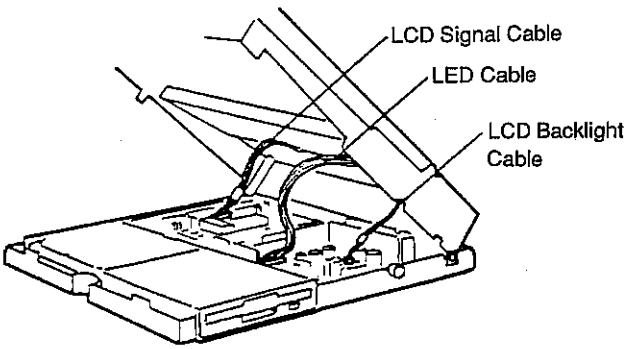
3. Lift up the cabinet top. This reveals the system board of the computer.



4. Lift up the keyboard and unfasten the connector as illustration shows. The disconnect the cable.

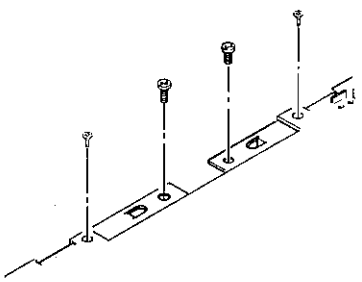


5. First incline the cabinet top backward slowly about 30 degrees. Then disconnect three cables. (the LCD signal cable, the LCD backlight cable, and the LED cable.)

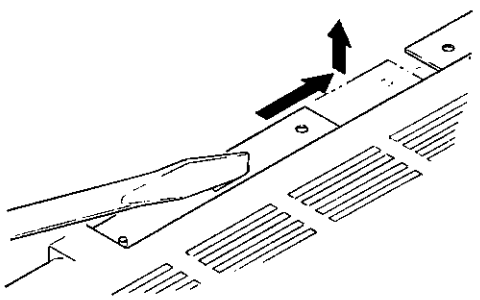


2) LCD unit removal

1. Remove the four screws which are fixing the tilt mechanism.



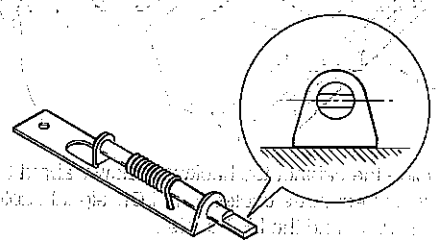
2. Move a tilt mechanism to the center with a screwdriver, and remove it upwards.
   Then remove the other tilt mechanism in the same manner.



3. Operate the LCD release lever, unfix the upper cabinet and the LCD section, and separate the upper cabinet from the LCD section.
   In this case, be careful not to damage two LCD cables.

Installation

1. Install the upper cabinet and the LCD section by reversing the disassembly procedure.
   When installing the tilt mechanism, set the shaft horizontally in parallel to the angle bottom and insert into the LCD section.



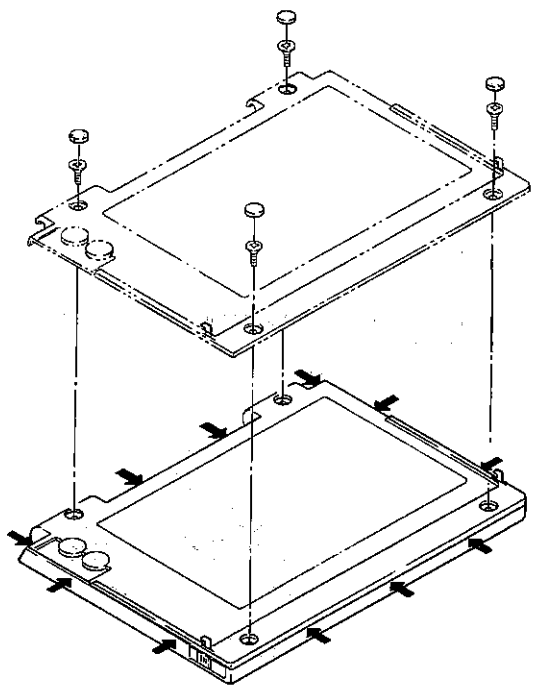
2. Attach the upper and lower cabinets to the set.

3) LCD section

Disassembly

<Caution>
For disassembly of the LCD unit, be sure to follow the procedure below. If not, the cabinet may be damaged.

1. Remove the keyboard.
2. Separate the upper cabinet from the lower cabinet.
3. Remove the upper cabinet.
4. Remove the four rubber cushions fixed with duplex tape on the LCD section, and remove the four screws which were covered by the four rubber cushions.



5. Remove the front and rear cabinets of the LCD section.
6. Remove the fixture which fixes the LCD section and the body.
7. Remove the reflection plate of the backlight.
8. Remove the fixing screws and the connectors of the illumination control PWB and the backlight convertor PWB, and remove the PWB's.

Assembly

1. Assemble the LCD unit by reversing the disassembly procedure.
   Carefully check that there is no fingerprint on the LCD section. If there is, clean with a cloth and alcohol. The cloth must be fine and smooth, such as glass wiper cloth.
2. Attach the upper cabinet to the set.
3. Attach the lower cabinet to the set.
4. Attach the keyboard to the set.
5. HD INTERFACE AND HD DRIVE
   The HD drive unit can be replaced only in whole unit, but not in part. When they are diagnosed to be defective by the diagnostic program, replace the whole unit of them.

4) Cautions

1. Although the CE-471A CRT adaptor board is an option for the PC-4700, it comes standard for the US version PC-4700. For more information about the wiring schematics and parts layout, refer to the CE-471A Service Manual.
2. Cosmetic sheet
   Do not use the cosmetic sheet once removed. Be sure to use the new one.
3. Deposit of a paint dust on the back of the cabinet may fall on the PWB when the machine is disassembled and re-assembled for servicing and it may then cause a machine malfunction. To avoid this, the machine internal must be cleaned whenever the machine is disassembled.

CHAPTER 2. GENERAL INFORMATION

1. General information

PC-4700 series are compact and lightweight laptop computers. They pack the power and sophistication of desk-top models into the laptop size.

In order to attain the high performance, this computer accommodates large and high contrast paper white LCD with the CCFT backlight, 3-1/2" floppy disk drive, 3-1/2" hard disk drive, and well-packed 79-key full keyboard. The display provides clear text and graphics in 640 by 400 dots especially by supporting 4-shades of gray (tiling) and 8 x 16 dots (character box) characters.

Further, PC-4741 or PC-4721 incorporates a 40MB or 20MB hard disk drive in its unit and accomplish battery operation. The full-size step keyboard provides 79 keys, enhancing the ease of use with separate function and cursor keys.

The main unit includes i80188 compatible CPU running at 10MHz, socket for coprocessor, 640KB RAM standard expandable to 1.6MB, a serial interface, a parallel printer interface, an external FDD interface. The internal options include modem card with a serial interface (for US/Canada only), color/monochrome CRT adaptor, and 1MB EMS memory card. The external expansions include 5-1/4" 360KB floppy disk drive unit.

The newly revised original BIOS assures the execution of numerous applications with the combination of MS-DOS 3.3 operating system.

PC-4700 series consists of the following 3 models:

*PC-4702: 640KB RAM; two 3-1/2" 1.44MB FDDs; display w/ backlight; 79-key keyboard; serial interface; parallel interface; external 5-1/4" FDD (360KB) interface; MS-DOS 3.30/GW-BASIC 3.22

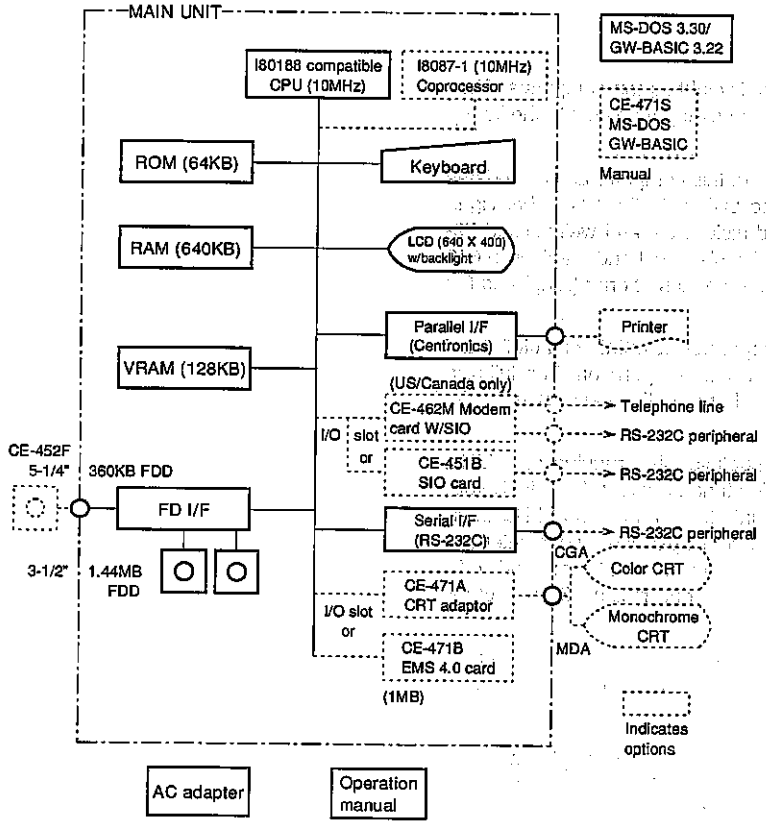
*PC-4721: 640KB RAM; a 3-1/2" 1.44MB FDD; a 20MB HDD; display w/ backlight; 79-key keyboard; serial interface; parallel interface; external 5-1/4" FDD (360KB) interface; MS-DOS 3.30/GW-BASIC 3.22

*PC-4741: 640KB RAM; a 3-1/2" 1.44MB FDD; a 40MB HDD; display w/ backlight; 79-key keyboard; serial interface; parallel interface; external 5-1/4" FDD (360KB) interface; MS-DOS 3.30/GW-BASIC 3.22

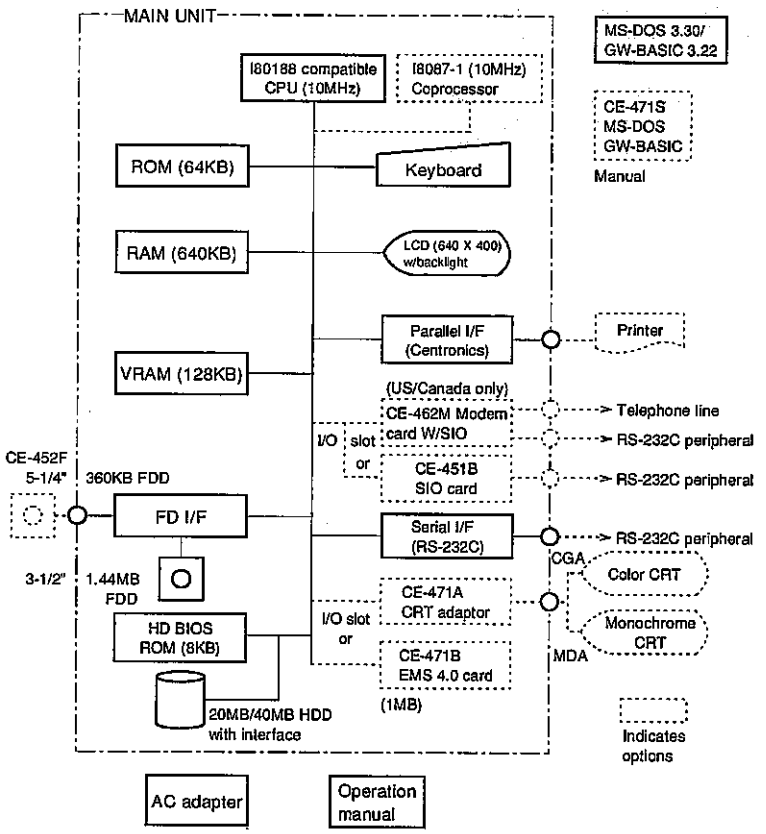
2. System Configuration

2-1. System block diagram

2-1-1. PC-4702



2-1-2. PC-4721/4741



2-2. Specification

2-2-1. Main unit

CPU : NEC V40 (i80188 compatible)
CPU clock speed – 10MHz (7.16MHz when coprocessor is installed.)
System speed – Standard/Slow selectable on set-up menu

Coprocessor : Socket for i8087-1 (10MHz version)
NOTE: CPU clock speed is changed to 7.16MHz automatically when coprocessor is installed. When it is removed, CPU clock speed is changed to 10MHz automatically.

Memory : ROM – 64KB
including BIOS, set-up functions, CG, self check, etc
512K bits EP-ROM (27C512 type) x 1 piece
ROM-8KB (HD version only)
including HD BIOS 64Kbits EP-ROM (27C64 type) x 1 piece
RAM – 640KB standard
256K bits (64K x 4 bits) DRAM x 4 pieces
1Mbits (256K x 4 bits) DRAM x 4 pieces
without parity
expandable up to 1.6MB with the optional 1MB EMS memory card (EMS 4.0)
VRAM – 128KB

Display : TST (Triple Super Twisted nematic) LCD with one CCFT (Cold Cathod Flouecent Tube) edgelight
Text – 80 char. x 25 lines, 8 x 16 dots char. Box
Graphics – 640 x 400 pixels, 4-shades of gray (tiling)
Aspect ratio – 1:1
Emulation – CGA/MDA/AT&T 640 x 400 Graphics
LCD active area – 205(w) x 155(h) mm
LCD contrast and backlight brightness are adjustable by each volume
Not detachable
90 – 131 degrees tilt angle adjustment
CCFT backlight
– white color
– life: Approx. 10,000 hours (until luminescent brightness becomes half)
– can be replaced by service man (service parts)

Data storage : PC-4702 – two side-mounted 3-1/2" 1.44MB FDD
Right side: A drive, Left side: B drive
PC-4721/4741 – one side-mounted 3-1/2" 1.44MB FDD
one internal 3-1/2" 20MB/40MB HDD
Left side: HDD (C drive), Right side: FDD (A drive)
HDD – average access time: 29 msec
power save management:
can be set "Time-Out*" on set-up menu
Always ON/2 minutes/5 minutes/10 minutes
*: spindle motor of HDD will be controlled by the value of "Time-Out"

Keyboard : full-size 79-key step keyboard
separate cursor keys
10 programmable function keys
LEDs for Num Lock, Scroll Lock, and Caps Lock
Set-Up key for pop-up set-up menu
Cylindrical and thin keytop
With click mechanizm
Not detachable

Interface : Serial (RS-232C) x 1 port (D-SUB 9 pin, male connector)
Parallel (Centronics) x 1 port (D-SUB 25 pin, female connector)
External 5-1/4" FDD (360KB) x 1 port (D-SUB 25 pin, female connecter)

I/O slot : Sharp proprietary slot x 3
– 1 slot for color/monochrome CRT adaptor
– 1 slot for modem/SIO card (for US/Canada only) or SIO card
The above cards are installed into the same space. So, only one card is available at the same time.
– 1 slot for 1MB EMS 4.0 memory card

Power Supply : Rechargeable lead battery
– low battery warning
low battery indicator
alarm
AC adaptor
EA-452V
IN : local voltage
OUT : DC 9V, 2.5A
Dimension : 115(w) x 67(d) x 55(h) mm
Weight : Approx. 425g

Volume : LCD contrast volume
Backlight brightness volume

Switch : Power ON/OFF button (software switch)
4 dip switches

Dip Switch Label	Feature	Initial setting
1	Alarm Control (Low Battery/Shut off Alarm) ON/OFF	ON
2	Speaker Control (without alarm) ON/OFF	ON
3	System all reset ON/OFF	OFF
4	Speaker Volume LOW/HIGH	OFF (HIGH)

Shut off alarm switch (alarm when upper cabinet is shut during power on.)

LED indicator : Power (green); low battery (red);
PC-4702 – drive A (green); drive B (green)
PC-4721/4741 – floppy disk (green); hard disk (green)
Caps Lock (green); Num Lock (green); Scroll Lock (green)

Other : Carrying handle; speaker; display lock slide-switch x 2

Dimension : 11(w) x 11.1(d) x 2.2(h) inch
280(w) x 282(d) x 58(h) mm
(high: cushion rubber on the bottom cabinet included, without cushion rubber: 57mm)

Weight : PC-4702 – 3.6kg
PC-4721/4741 – 3.8kg
(with battery, without AC adaptor)
battery: Approx. 830g
AC adaptor (EA-452V): Approx. 425g

Software : MS-DOS 3.30/GW-BASIC 3.22

Manual : Operation Manual (MS-DOS/GW-BASIC quick reference included)
Optional MS-DOS and GW-BASIC manuals

2-2-2. Option

Internal Options:

CE-471A color/monochrome CRT adaptor
- color/monochrome 2 modes supported
  color: CGA (640 x 200 pixels)
  monochrome: MDA (720 x 350 pixels)
  color/monochrome mode is selected by set-up functions.
- 2 character sets (CG1/CG2) supported
  CG1: general
  CG2: Denmark/Norway
  CG1/CG2 is selected by short-pin switch on the card.
- dealer option

CE-451B SIO card
- Serial (RS-232C) x 1 port (D-SUB 25pin, male connector)
- dealer option

NOTE: Max. SIO 2 ports available when CE-451B installed.
1. Standard SIO (D-SUB 9pin, male connector)
2. SIO on the optional CE-451B SIO card (D-SUB 25pin, male connector)

CE-471B EMS memory card
- 1MB EMS 4.0 memory card and EMS 4.0 software
- with operation manual
- dealer option

CE-462M modem card (for US/Canada only)
- mode/SIO 2 functions supported
  mode: 300/1200/2400 BPS; Bell 103/212A; CCITT V.21, V22 and V.22 bis
  Hayes compatible command set
  SIO: RS-232C x 1 port (D-SUB 25 pin, male connector)
  modem/SIO function is selected by set-up functions
- dealer option
- with installation instructions

NOTE: Max. SIO 2 ports available when CE-462M is installed and used as a SIO.
1. Standard SIO (D-SUB 9 pin, male connector)
2. SIO on the optional CE-462M modem card (D-SUB 25 pin, male connector)

External options:

CE-452F 5-1/4" FDD unit (without SEEG)
- 5-1/4" FDD (360KB) x 1
- AC power
- with I/F cable

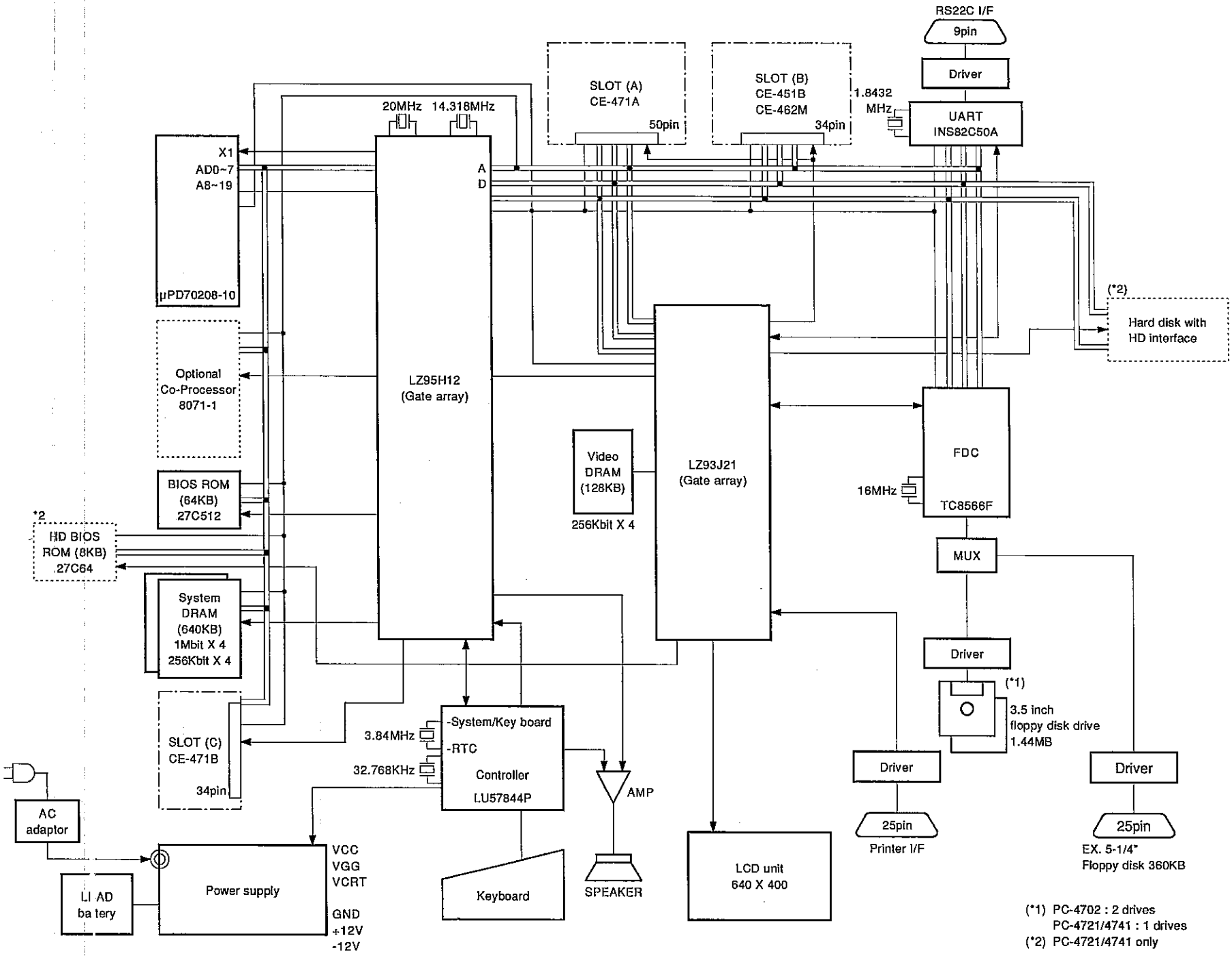
Manual:

CE-470KE/F/W/M/S key top kit
- key top (E: 18, F: 21, W: 19, M: 19, S: 24 pieces)
- tool for pulling up the key top

CE-470SE/F/G/I operation manual
- operation manual for PC-4700 series
  (E: English, F: French, G: German, I: Italian)

NOTE: PC-4700 for SEEG doesn't include the operation manual.

BLOCK DIAGRAM



3-1. Memory and I/O map

3-1-1. Memory map for the PC-4700 system

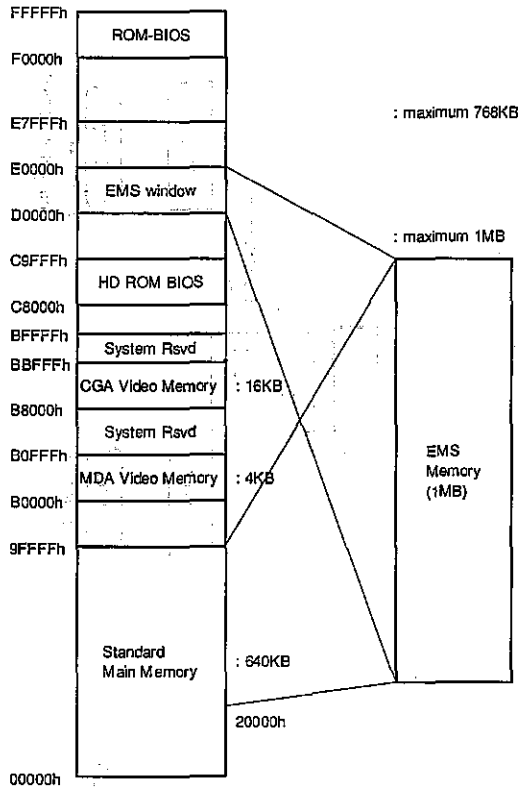


Fig. 3-1 Overall memory map

3-1-2. IO/MAP

Register	IO Address.
Emulated DMA Controller	00H..0FH
V40DMA Controller	10H..1FH
Interrupt Controller	20H..3FH
System Timer	40H..5FH
PPI	60H..62H
NMI Mask	A0H..BFH
Asynchronous Communication (Secondary)	2F8H..2FFH
Hard Disk	320H..323H
Parallel Port	378H..37FH
Parallel Port	3BCH..3BEH
VIDEO IO	3B0H..3BBH
VIDEO IO	3BFH
VIDEO IO	3C0H..3CFH
VIDEO IO	3D0H..3DFH
FLOPPY DISK IO	3F0H..3F7H
Asynchronous Communication (Primary)	3F8H..3FFH
V40 System IO	FFF0H..FFFFH

3-2. Clock generator

The clock generator is included in LZ95H12, and connected with two crystal oscillators of 14.31818MHz and 20MHz.
The two clocks pass through the clock select circuit in LZ95H12, and one of them is outputted from X1 terminal to V40 X1 terminal. The details are shown in Fig. 3-2.

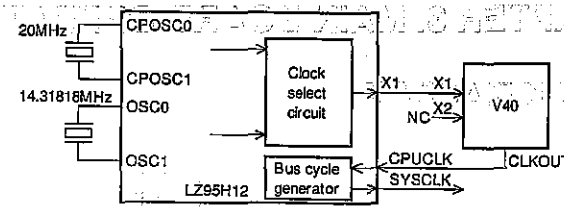
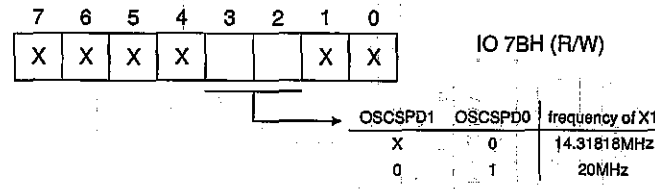


Fig. 3-2 Overall clock generate circuit

The frequency of the clock supplied from LZ95H12 X1 terminal to V40 is determined according to the states of bit 3 (OSCSPD1) and bit 2 (OSCSPD0) of the IO port (7BH) in LZ95H12 as shown below.



OSCSPD1	OSCSPD0	frequency of X1
X	0	14.31818MHz
0	1	20MHz

Assertion of the RESET signal will reset OSCSPD [0..1]. IF 8087 is not installed, ROM-BIOS sets OSCSPD0.
When setting OSCSPD0, the shift to frequency of 10MHz is made with no glitches, thus avoiding the need to reset the system.

3-3. Reset circuit

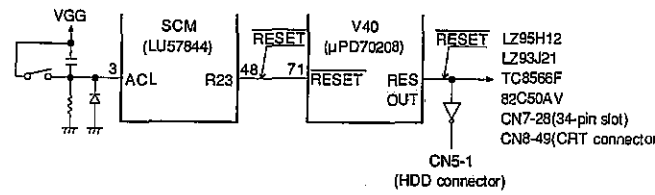


Fig. 3-3 Reset control circuit

The SCM can be reset in one of the following two ways.

1. When VGG turns on, a high state of signal is sent to the line ACL of the SCM from the differentiation circuitry composed of a capacitor and resistor.
2. When the dip switch-1, located at the lower side of the machine, set ON, it causes the ACL input high to reset the SCM. Operation starts when it turned off.

With depression of the ON/OFF switch while the machine is off or a hardware reset is given (simultaneous depression of CTRL, ALT, SETUP keys), VCC is turned active and $\overline{\text{RESET}}$ is forced high. The V40 synchronizes an async signal $\overline{\text{RESET}}$ with the internal clock and sends it out as an active high signal.

The former ($\overline{\text{RESET}}$) is sent to the V40, and the latter (RESET) to the LZ95H12, LZ93J21, TC8566F, 82C50AV, 34-pin slot, CRT connector. The RESET signal is inverted and sent to HDD connector.

3-4. Interrupt control

Eight maskable interrupts and one non-maskable interrupt are provided.

- NMI is set high by the LZ95H12 when a specific I/O is accessed.
- Maskable interrupt may be caused in one of the following:

Number	Usage	Originating device
1	Keyboard	LZ95H12
3	Asynchronous communication (Secondary)	INS82C50A
4	Asynchronous communication (Primary)	
5	Hard disk	Hard disk controller
6	Floppy disk	TC8566F
7	Parallel printer	LZ93J21

3-5. Bus configuration

The PC-4700 system uses the forrowing two buses.

1) CPU (AD) bus
2) System Data (SD) bus

The bus configuration is shown in Figure 3-4.

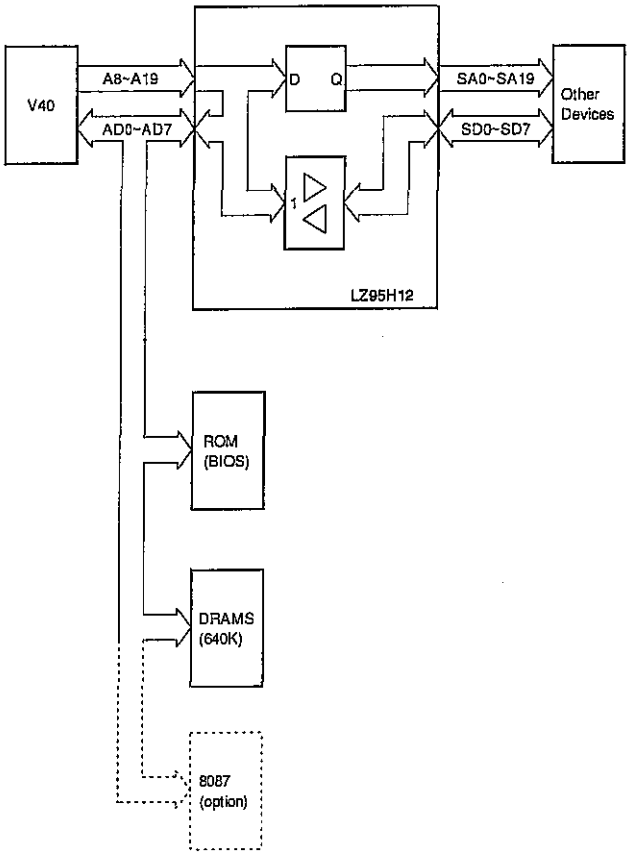


Fig. 3-4 Bus configuration

3-6. Memory

3-6-1. Block diagram

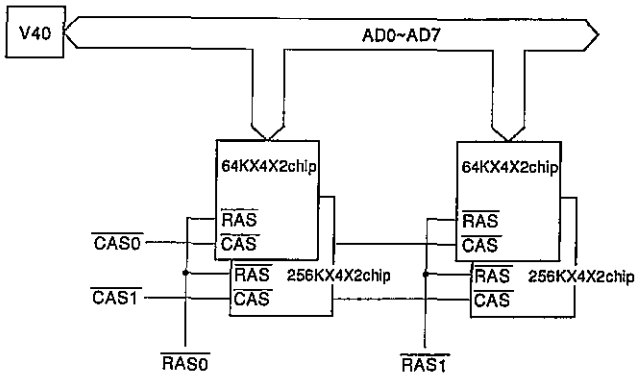


Fig. 3-5 RAM section block diagram

3-6-2. LZ95H12 address assignment

$\overline{RAS}$ and $\overline{CAS}$ are generated from LZ95H12. $\overline{RAS0}$ is set active if $\overline{RAS}$ is even address or $\overline{RAS1}$ active if $\overline{RAS}$ is odd address.

$\overline{CAS}$ signal is assigned to $\overline{CAS0}$ ~ $\overline{CAS4}$ as shown in Table 3-1.

Table 3-1

Input						Output								
A19	A18	A17	A16	A0	$\overline{REFRQ}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$	$\overline{CAS4}$	$\overline{ROMCE}$	
X	X	X	X	X	0	0	0	1	1	1	1	1	1	REFRESH
1	1	1	1	X	1	1	1	1	1	1	1	1	0	F0000H~FFFFFH
0	0	0	X	0	1	0	1	0	1	1	1	1	1	00000H~1FFFFH even
0	0	0	X	1	1	1	0	0	1	1	1	1	1	00000H~1FFFFH odd
Neither of A19 ~ A17 is "0"			X	0	1	0	1	1	0	1	1	1	1	20000H~9FFFFH even
			X	1	1	1	0	1	0	1	1	1	1	20000H~9FFFFH odd

3-6-3 Memory access timing

① Normal DRAM access

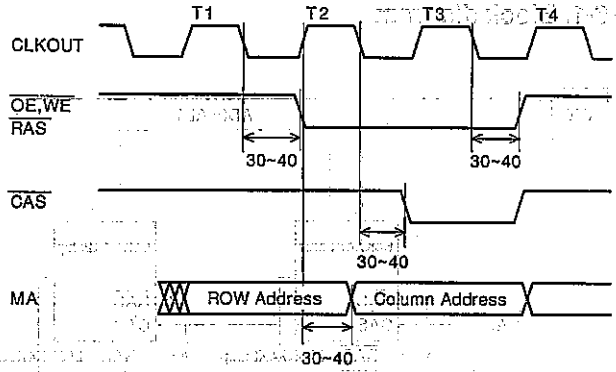
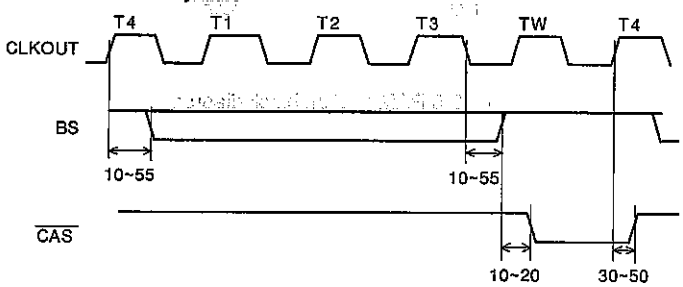


Fig. 3-6 DRAM access timing (normal)

② At DMA memory write



Same as ① for the timing of $\overline{OE}$, $\overline{WE}$, $\overline{RAS}$, and MA.

Fig. 3-7 DRAM access timing (DMA memory write)

③ ROM access

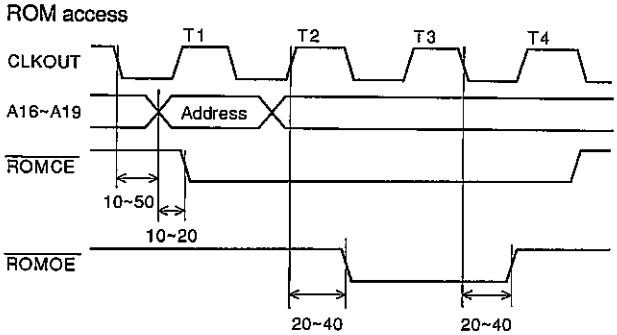


Fig. 3-8 ROM access timing

3-7. 8087 interface

The interface log of 8087 is stored in LZ95H12. The signal connection is shown in Fig. 3-9.

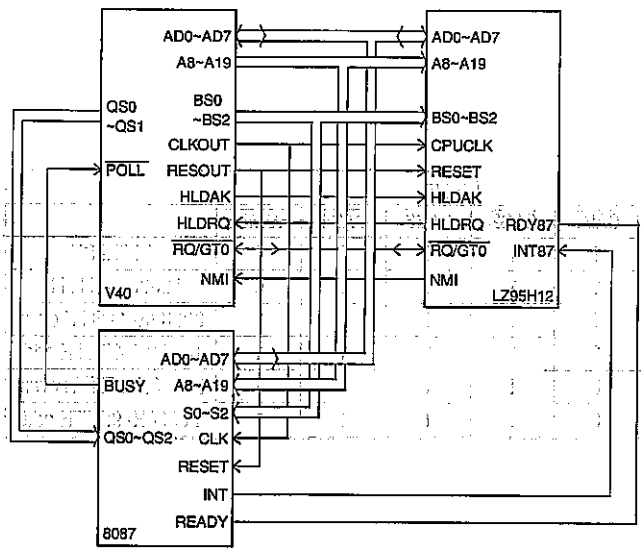


Fig. 3-9 8087 interface signal connection

3-8. READY control circuit

The signal READY (RDYV40) for V40 is controlled by LZ95H12. LZ95H12 and LZ95J21 control $\overline{EXTM}$, $\overline{EXTIO}$, SLOCYC, and READY signals for the devices accessed. LZ95H12 determines the bus cycle according to these signals, to control RDYV40. The block diagram is shown in Fig. 3-10.

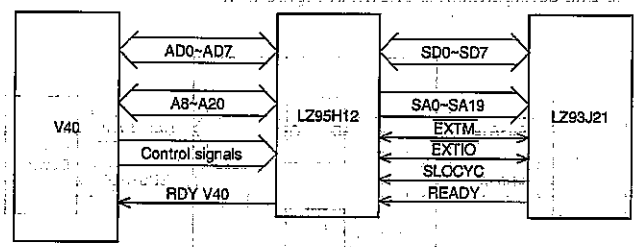


Fig. 3-10 Overall ready control signals

3-9. DMA control

Although the V40 has four DMA channels, two channels are used. DRQ2 and $\overline{DACK2}$ are used for controlling the floppy.

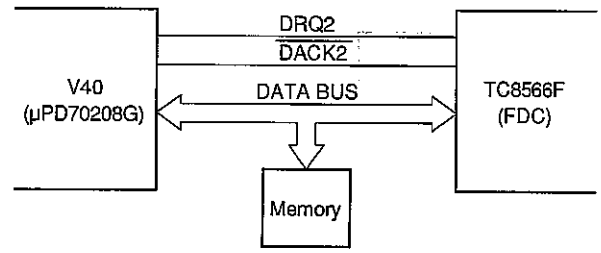


Fig. 3-11 Overall DMA control signals

When the V40 starts to DMA after setting the TC8566F register, the TC8566F sets DRQ2 high. After the V40 receives this signal, $\overline{DACK2}$ is set low to perform DMA transfer between the TC8566F and the memory.

DRQ3 and $\overline{DACK3}$ are used for controlling the hard disk. DRQ3 is supplied from the LSI in the hard disk controller. When DRQ3 becomes high, V40 makes $\overline{DACK3}$ low to perform DMA transfer between with the controller.

3-10. Bus cycle generator (including LZ95H12)

3-10-1. General

The LZ95H12 bus cycle generator produces the SYSCLK, ALE, STC, $\overline{SMRD}$, $\overline{SMWR}$, $\overline{SIORD}$ and $\overline{SIOWR}$ signals. It interprets the READY signal and drives the RDYV40 signal to control the number of wait states. The LZ95H12 determines the speed of the devices involved in the transfer. Devices are grouped into three speed categories:

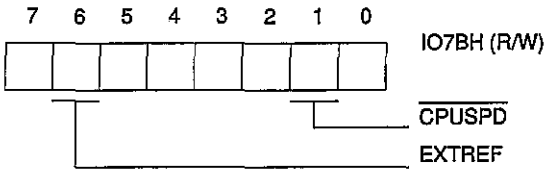
1. fast AD bus devices;
2. fast SD bus devices; and
3. slow SD bus devices.

Fast AD devices are the V40, the 8087, the LZ95H12, the system ROM, the system DRAM. Fast SD bus devices are those devices which are controlled by the LZ93J21 for which the SLOCYC signal is not asserted. This signal is sampled at the start of first T-cycle following the assertion of the $\overline{SMRD}$, $\overline{SMWR}$, $\overline{SIORD}$ or $\overline{SIOWR}$. At 7.16MHz, this occurs at the start of T3. At 10 MHz this occurs at the start of the first TW. All other devices are slow SD bus devices.

There are three speeds of non-refresh cycles: fast, medium and slow. Fast speed cycle execute with no wait states, except for IO, NMI trapping cycles, which take nine T-cycles. Medium speed cycles may also insert wait states in response to a reset READY signal. A special extended medium speed cycle that drives SYSCLK from CPUCLK is also implemented. At 7.16 MHz, the minimum medium speed cycle takes 5 T-cycles. At 10 MHz, the minimum medium speed cycle takes 6 T-cycles. Medium and slow speed cycles have the same timing until SLOCYC is sampled.

If the $\overline{\text{CPUSPD}}$ (IO7BH bit 1) bit is set, the bus cycle generator will only generate slow speed memory cycles. This is done to accommodate programs using software timing loops. Assertion of the RESET signal will reset $\overline{\text{CPUSPD}}$. If $\overline{\text{CPUSPD}}$ is reset, then speed of the cycle is dependent on the slowest device involved. If the slowest device is a fast AD bus device then a fast speed cycle is generated. If the slowest device is a fast SD bus device, then a medium speed cycle is generated. Otherwise, a slow speed cycle is generated. When "speed: slow" is selected in the set up menu, $\overline{\text{CPUSPD}}$ = 1 (High)

There are two speeds for refresh cycle-fast and slow. If the EXTREF (IO7BH bit 6) bit is set, the bus cycle generator will generate a slow speed cycle. Thus DRAM on the SD bus may be refreshed. If EXTREF and $\overline{\text{CPUSPD}}$ are reset, then the bus cycle generator will generate a fast speed cycle. Thus any DRAM on the SD bus must provide its own refresh. Resetting EXTREF may result in as much as a 5% increase in system throughput. Assertion of the RESET signal will reset EXTREF. When the optional EMS card (CE-453B) is installed, EXTREF = 1 (High).



3-10-2. SYSCLK Generation

For 7.16 MHz cycles, CLKOUT drives SYSCLK.
For 10 MHz fast speed cycles, SYSCLK is set during T2 and is reset during the rest of the cycle. For 10 MHz medium speed cycles, SYSCLK is set during T2, the first TW and T4 and is reset during the rest of the cycle. For 10 MHz extended medium speed cycles, SYSCLK is set during T2 and driven by CPUCLK for the rest of the cycle. For 10 MHz slow speed cycles, SYSCLK is set during T2, during the odd TW's and during T4 and is reset during the rest of the cycle. There are always an even number of TW's in a 10 MHz slow speed cycle. For 10 MHz cycles, SYSCLK is always reset during TI's and interrupt acknowledge cycles.

3-10-3. $\overline{\text{SWRD}}$, $\overline{\text{SMWR}}$, $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ Generation

$\overline{\text{SMRD}}$ and $\overline{\text{SMWR}}$ are not asserted during non-refresh cycles that access fast AD bus memory devices. $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ are not asserted during non-refresh cycles that access LZ95H12 internal IO devices or V40 internal private IO devices. $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ are asserted during accesses to emulated MDA/CGA IO addresses. $\overline{\text{SMRD}}$ and $\overline{\text{SIOWR}}$ are not asserted during fast refresh cycles.

For 7.16 MHz cycles, the $\overline{\text{SMRD}}$ and $\overline{\text{SIORD}}$ signals may be reset during T2, T3 and TW. These signals are set during the rest of the cycle. The same is true for $\overline{\text{SMWR}}$ and $\overline{\text{SIOWR}}$ during non-refresh, non-DMA cycles. For DMA memory write cycles, the $\overline{\text{SMWR}}$ signal may be reset during T3 and TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle. For refresh and DMA memory read cycles, the $\overline{\text{SIOWR}}$ signal may be reset during T3 and TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle.

For 10 MHz fast speed cycles, the $\overline{\text{SMRD}}$, $\overline{\text{SMWR}}$, $\overline{\text{SIORD}}$ and $\overline{\text{SIOWR}}$ signals are set during the cycle. For 10 MHz medium speed cycles, the $\overline{\text{SMRD}}$ and $\overline{\text{SIORD}}$ signals may be reset during T3 and TW. They are set during the rest of the cycle. The same is true for $\overline{\text{SMWR}}$ and $\overline{\text{SIOWR}}$ during non-refresh, non-DMA cycles. For DMA memory write cycles, the $\overline{\text{SMWR}}$ signal may be reset during all TW's except the first half of the first TW $\overline{\text{SMWR}}$ is set during the rest of the cycle. For refresh and DMA memory read cycles, the $\overline{\text{SIOWR}}$ signal may be reset during all TW's except the first half of the first TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle. For 10 MHz slow speed cycles, the $\overline{\text{SMRD}}$ and $\overline{\text{SIORD}}$ signals may be reset during T3 and all TW's except the last TW. They are set during the rest of the cycle. The same is true for $\overline{\text{SMWR}}$ and $\overline{\text{SIOWR}}$ during non-refresh, non-DMA cycles. For DMA memory write cycles, the $\overline{\text{SMWR}}$ signal may be reset during all TW's except the first TW and last TW. $\overline{\text{SMWR}}$ is set during the rest of the cycle. For refresh and DMA memory read cycles, the $\overline{\text{SIOWR}}$ signal may be reset during all TW's except the first TW and last TW. $\overline{\text{SIOWR}}$ is set during the rest of the cycle.

3-10-4. READY Interpretation and RDYV40 Generation

During fast speed cycles RDYV40 is set. RDYV40 is set during T1 and TI.

For 7.16 MHz medium speed cycles, RDYV40 is reset during T2 and then READY drives RDYV40 during the rest of the cycle. For 7.16 MHz slow speed CPU/COP memory cycles, RDYV40 is reset during T2 and T3 and then RDYV40 is driven by READY during the rest of the cycle. For 7.16 MHz slow speed IO, refresh and DMA cycles, RDYV40 is reset during T2, T3 and the first two TW's and then RDYV40 is driven by READY during the rest of the cycle.

For 10 MHz medium speed cycles, RDYV40 is reset during T2 and T3 and then RDYV40 is driven by READY during the rest of the cycle. For 10 MHz slow speed CPU/COP memory cycles, RDYV40 is reset during T2, T3 and the first two TW's. READY is sampled at the start and the end of the odd TW's starting with the first TW. If READY is reset for either sample, then RDYV40 remains reset for two more T-cycles and READY is again sampled. If READY is set for both samples, then RDYV40 remains reset for two more T-cycles and is then set for the rest of the cycle. For 10 MHz slow speed CPU/COP IO, refresh and DMA cycles, RDYV40 is reset during T2, T3 and the first four TW's. READY is sampled at the start and the end of the odd TW's starting with the third TW. If READY is reset for either sample, then RDYV40 remains reset for two more T-cycles and READY is again sampled. If READY is set for both samples, then RDYV40 remains reset for two more T-cycles and is then set for the rest of the cycle.

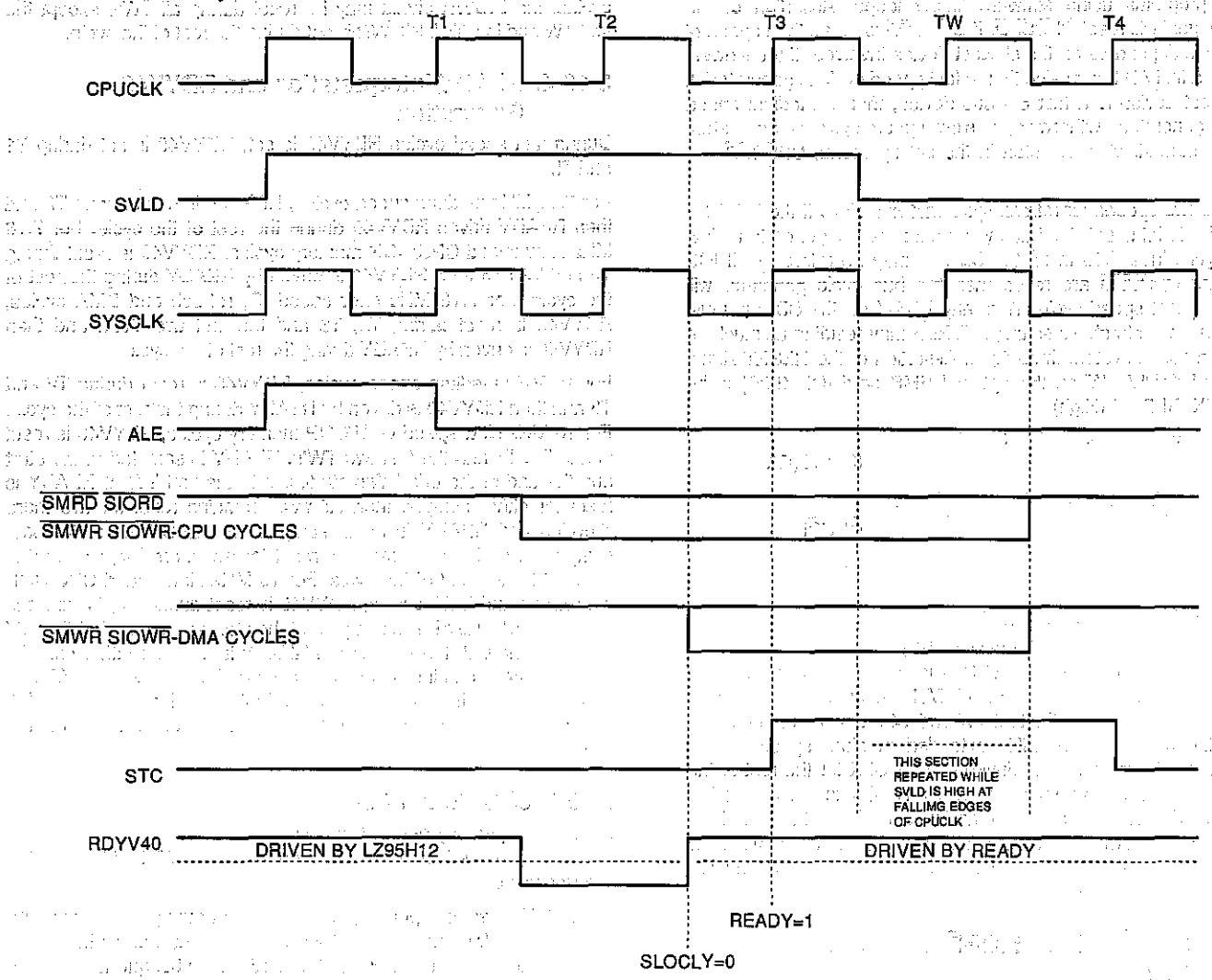
3-10-5. STC Generation

During fast speed cycles, STC is reset.
For 7.16 MHz medium and slow speed cycles, STC is driven by the inverted value of $\overline{\text{TC}}$.

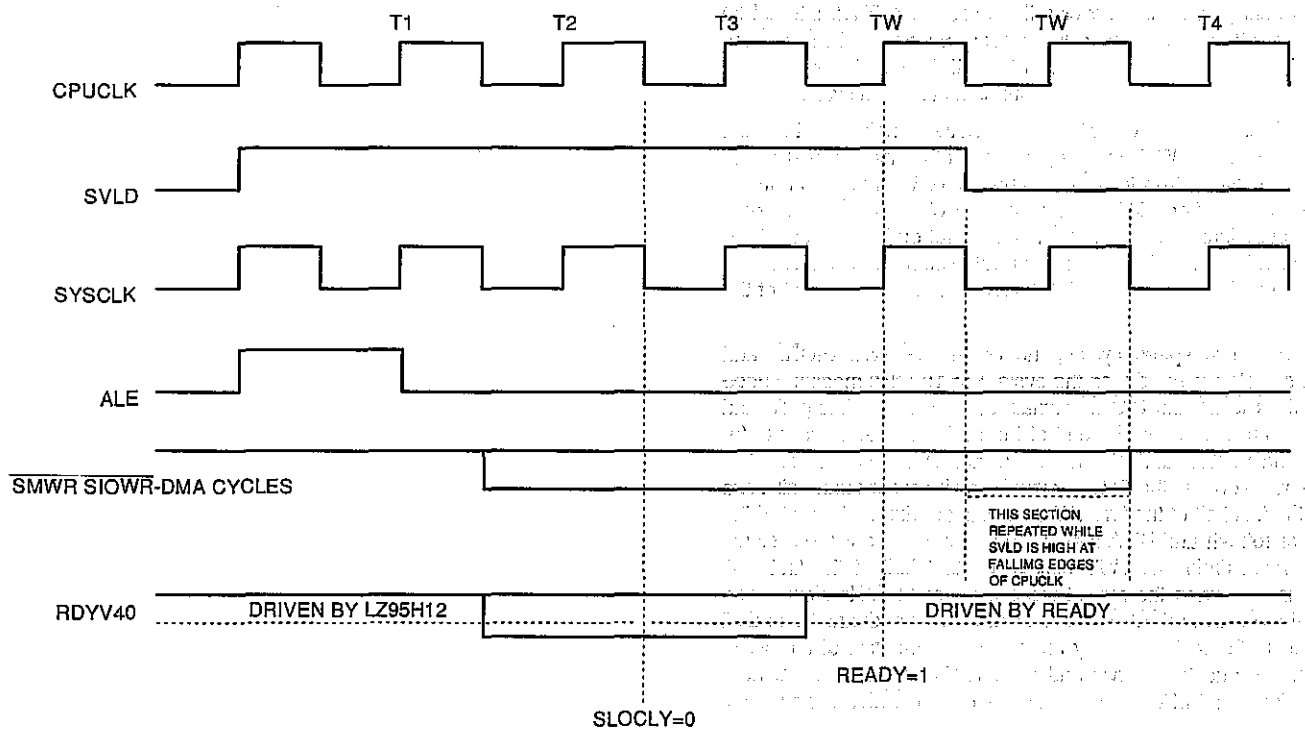
For 10 MHz medium speed cycles, STC is set during the second and subsequent TW's and during T4 while $\overline{\text{TC}}$ is reset. For 10 MHz slow speed cycles, STC is set during the third and subsequent TW's and during T4 while $\overline{\text{TC}}$ is reset. STC is reset during the rest of the cycle.

3-10-6. Timing chart

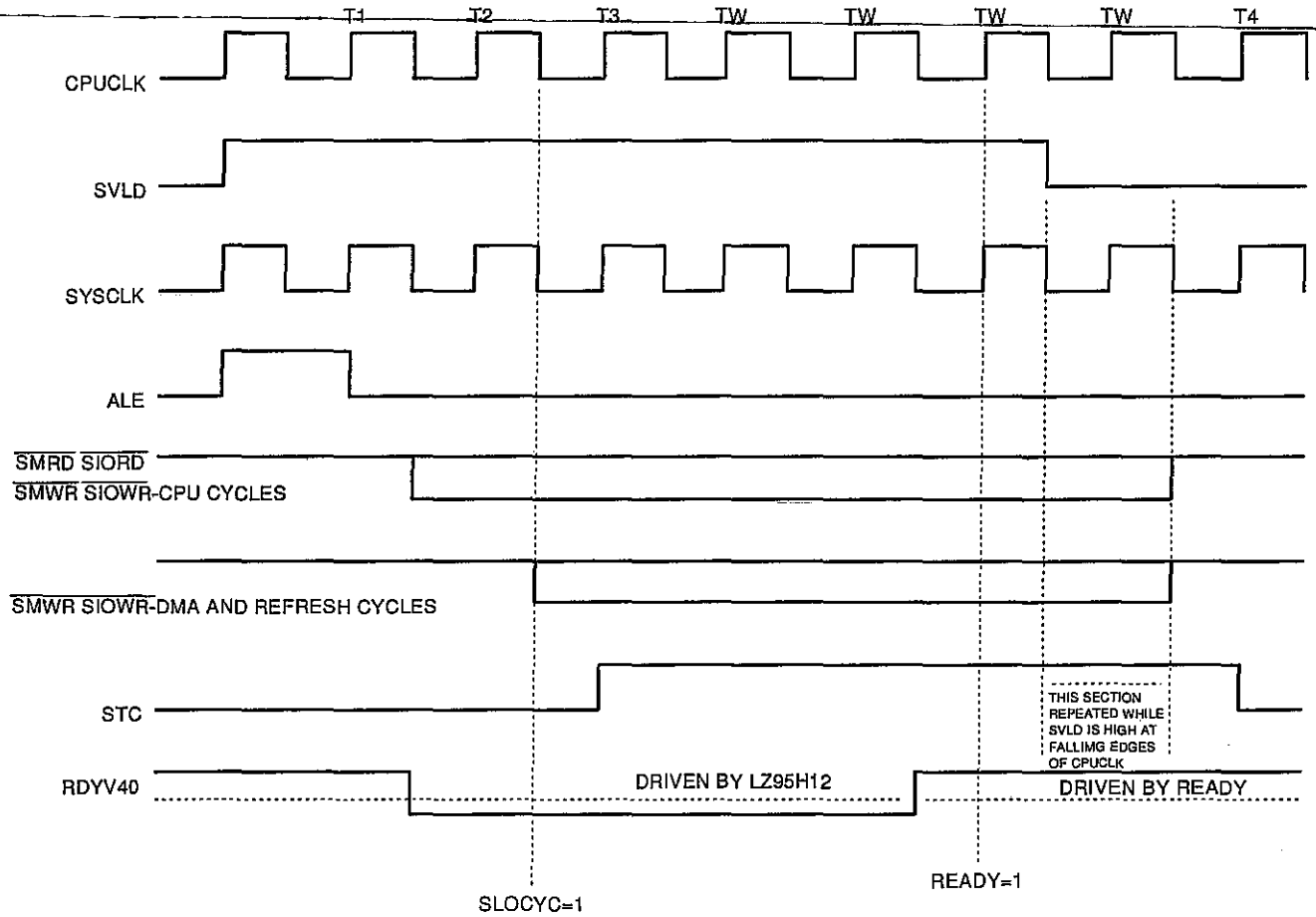
① 7.16 MHz MEDIUM cycle



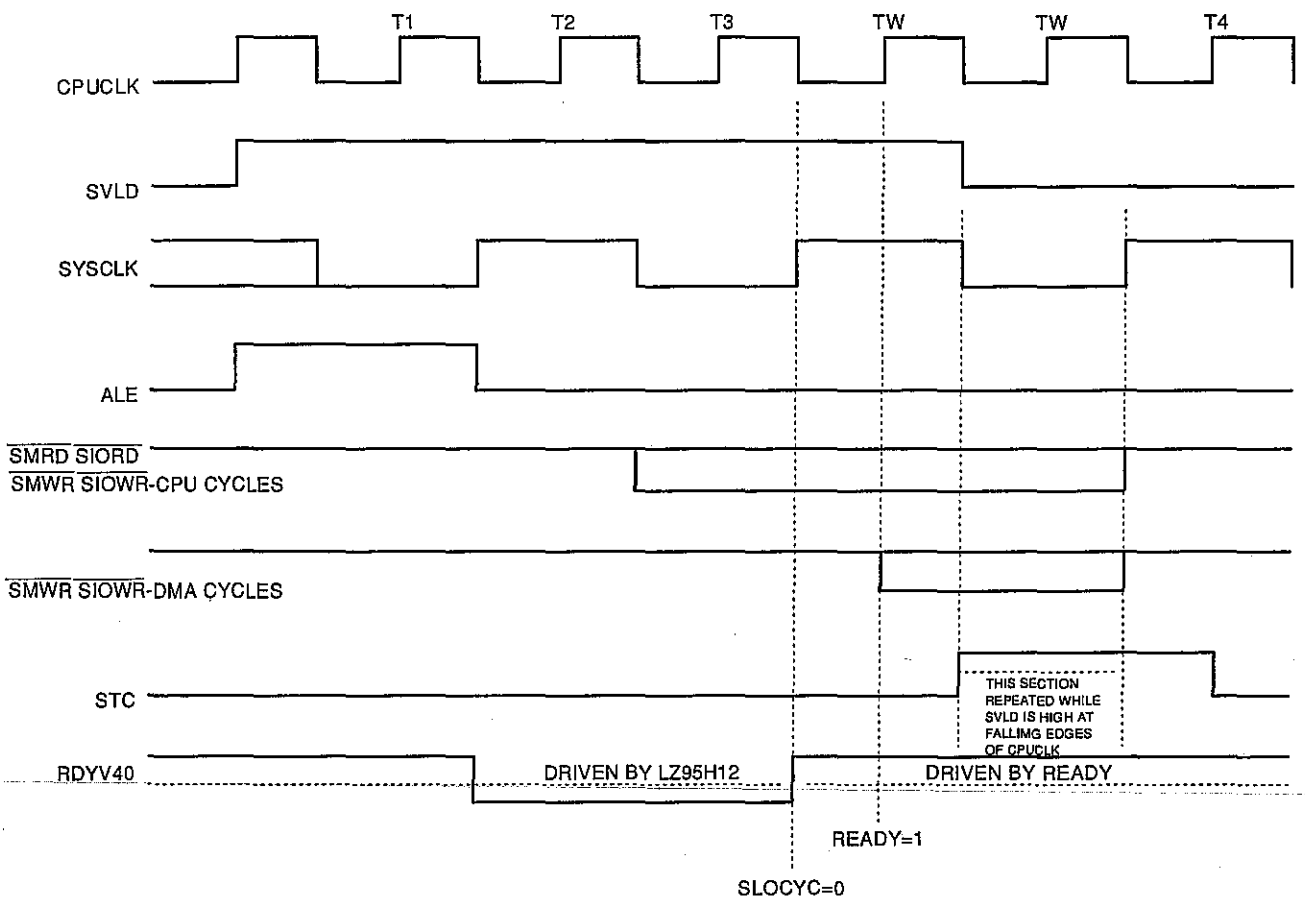
② 7.16 MHz SLOW cycle (CPU-MEMORY cycle)



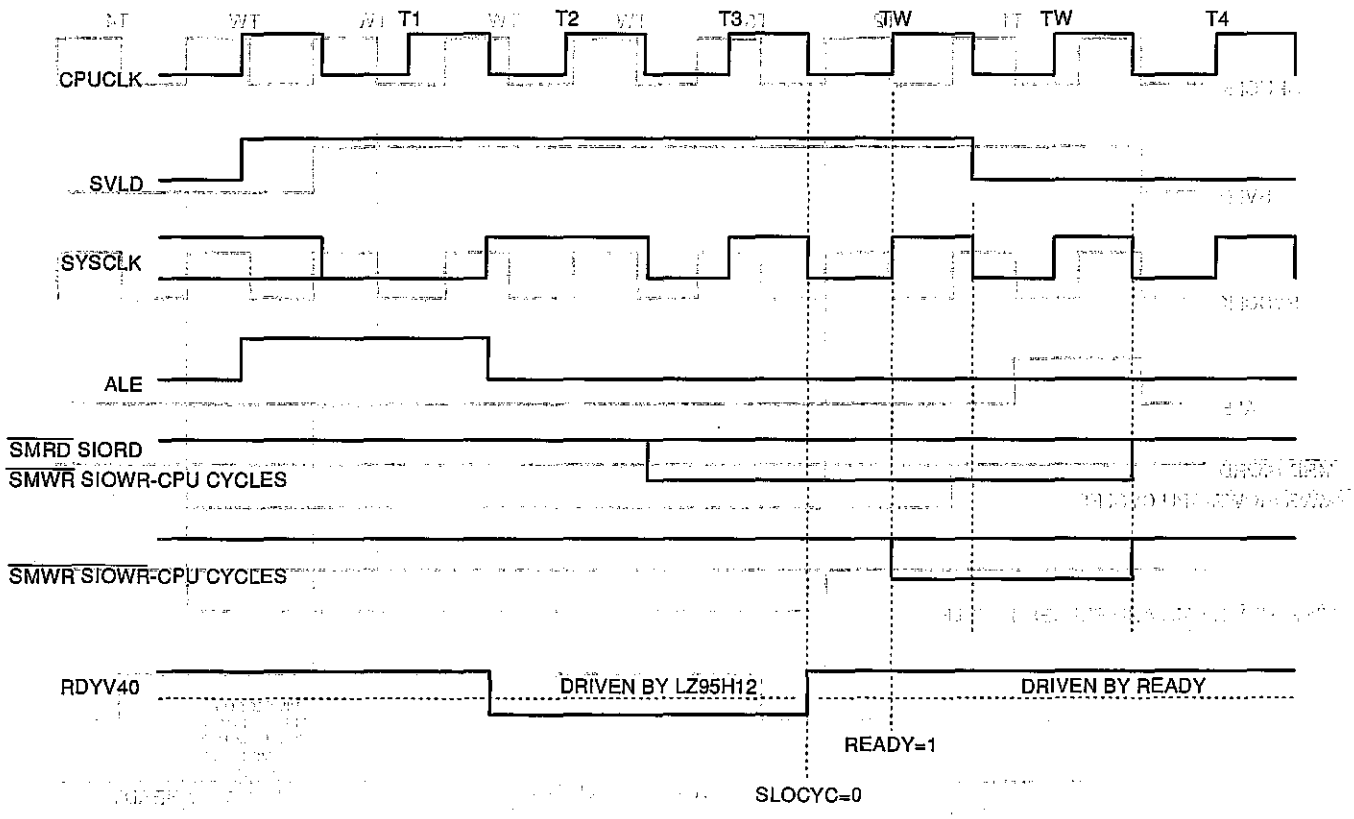
③ 7.16 MHz SLOW cycle (IO, DMA, REFRESH cycle)



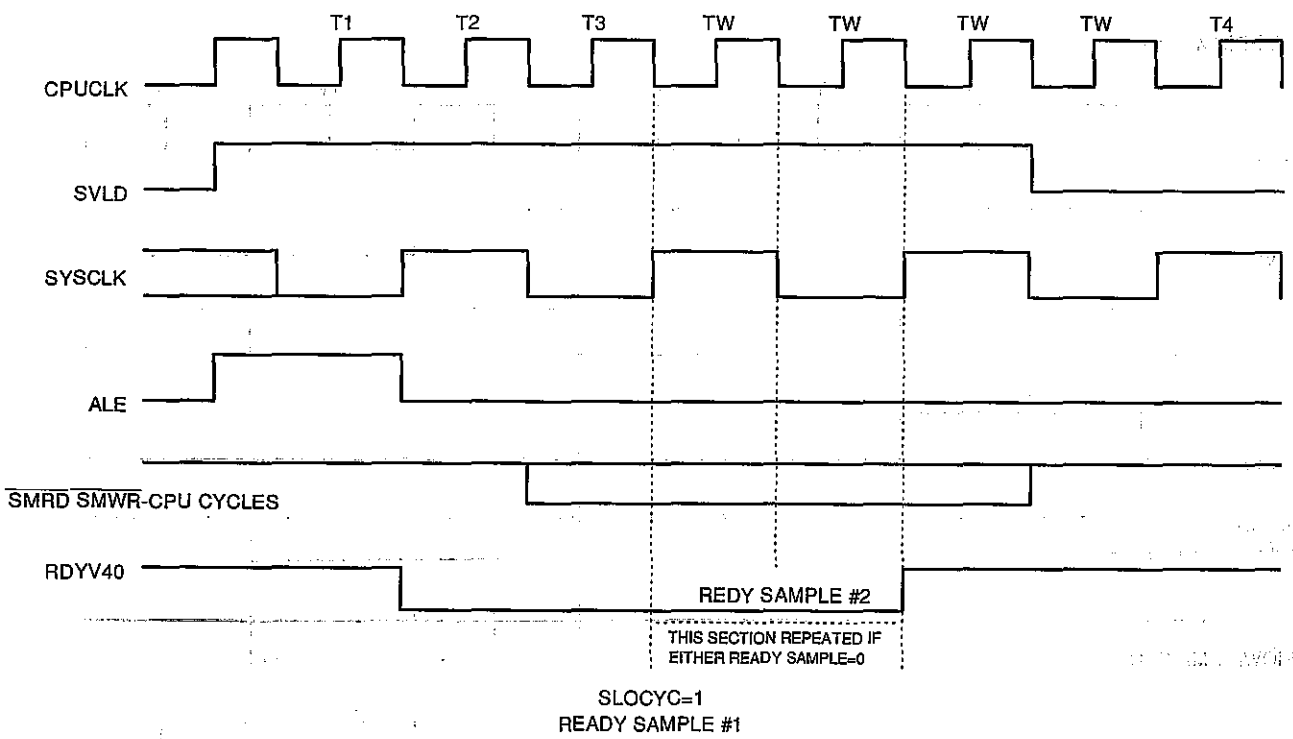
④ 10 MHz MEDIUM cycle



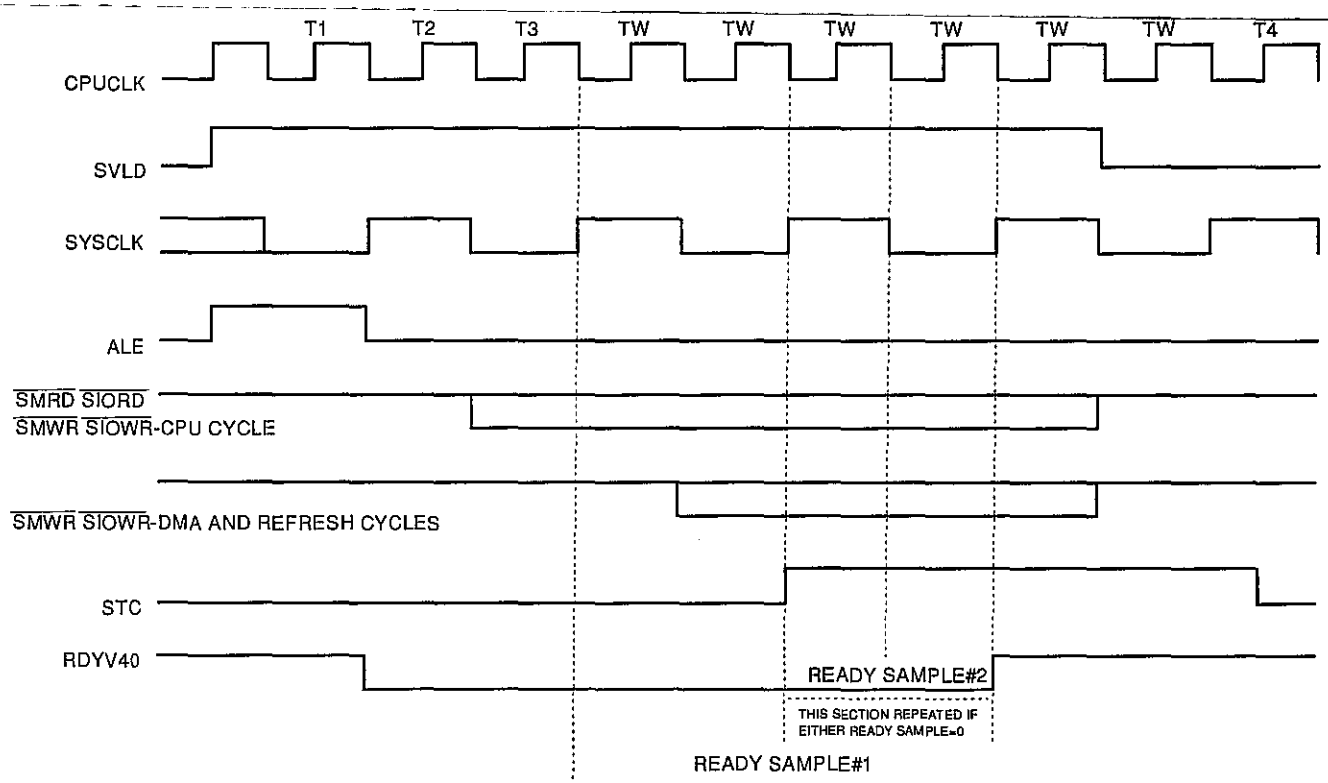
⑤ 10 MHz Extended MEDIUM cycle



⑥ 10 MHz SLOW cycle (CPU-MEMORY cycle)



⑦ 10 MHz SLOW cycle (IO, DMA, REFRESH cycle)



3-11. Printer interface

Fig. 3-12 shows a functional block diagram of the printer interface circuit. This circuit consists of the print data register, printer status port and printer control register.

The print data register, which is assigned at the I/O address 378H or 3BCH, stores data to be sent to the printer. The contents of this register can be read by the CPU at the I/O address 378H or 3BCH via the buffer.

The printer status port reads status information sent from the printer. This port is assigned at the I/O address 379H or 3BDH.

The printer control register stores control codes to be sent to the printer. This register assigned at the I/O address 37AH or 3BEH. Bit 4 of this register determines whether the $\overline{ACK}$ signal from the printer makes enable or disable as the CPU interrupt signal. When this bit is HIGH, interruption is enabled.

The contents of this register can be read by the CPU at the I/O address 37AH or 3BEH.

Assignment of the printer interface I/O address to either 37XH or 3BXH is dependent on the state of PPSEL (parallel port select bit 4) of the PC-4600 register CFR (Configuration Register) which is assigned to the I/O address 7FH. If PPSEL is 0, the printer interface I/O address is assigned to 3BXH. If PPSEL is 1, the address is assigned to 37XH.

It is possible to disable the standard printer adaptor by resetting PPS (bit 1) of the PCR (Planar Control Register) I/O address 65H which is normally set on.

Table 3-2 shows the printer I/O address definition.
Fig. 3-13 shows the printer timing chart.

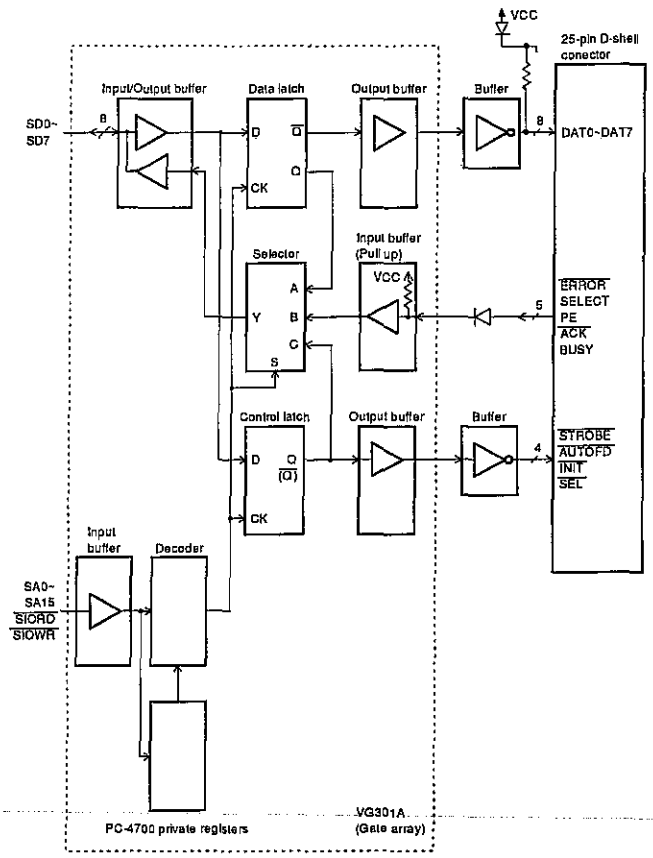


Fig. 3-12 Function block diagram

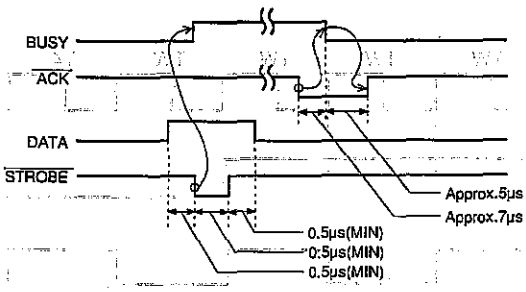


Fig. 3-13 Timing chart

I/O Address		Read/ Write	Bit	Description
65H		R/W	1	PPS. 1: Enables the standard printer adaptor (normally set 1).
7FH		R/W	4	PPSEL (Parallel Port Select) 0: Printer adaptor I/O address is assigned to 36XH. 1: Printer adaptor I/O address is assigned to 37XH.
	PPSEL	R/W	0	Print data 0 (LSB)
3BCH	0		1	Print data 1
			2	Print data 2
			3	Print data 3
			4	Print data 4
378H	1		5	Print data 5
			6	Print data 6
			7	Print data 7 (MSB)
	PPSEL	R	0	Not used (0 read)
3BDH	0		1	Not used (0 read)
			2	0 or 1 read
			3	$\overline{\text{ERROR}}$ read
379H	1		4	SELECT read
			5	PE read
			6	$\overline{\text{ACK}}$ read
			7	$\overline{\text{BUSY}}$ read
	PPSEL	R/W	0	STROBE written
3BEH	0		1	AUTOFD written
			2	$\overline{\text{INIT}}$ written
			3	SEL written
37AH	1		4	IRQENA, 1: Enables interrupt request.
			5	Not used (0 read)
			6	Not used (0 read)
			7	Not used (0 read)

Table 3-2 I/O address definition

3-12. Serial interface

As a standard, the PC-4700 has a serial interface which is assigned at the I/O address 3F8H through 3FFH or 2F8H through 2FFH.

Assignment of the serial interface I/O address to 3FXH or 2FXH is determined by the SCM (LU57832) output signal COM1/$\overline{2}$. When COM1/$\overline{2}$ is at a low, the serial interface I/O address is assigned to 3FXH. If high, the address is assigned to 2FXH.

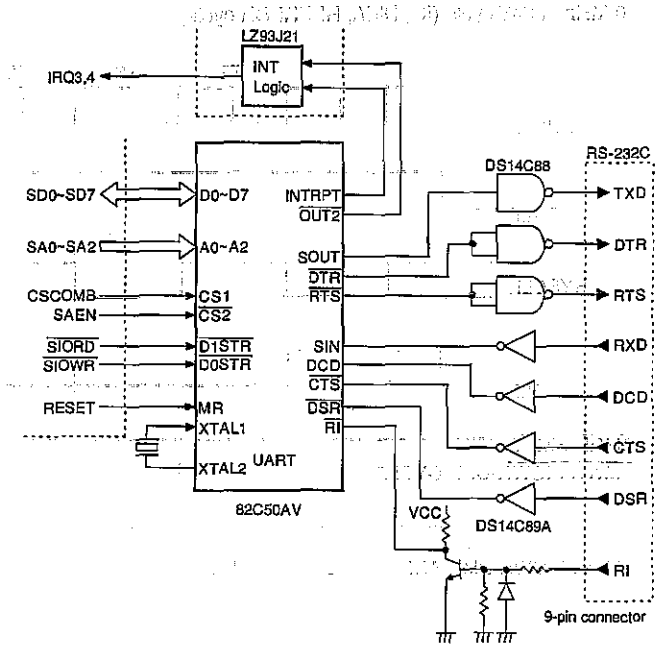


Fig. 3-14 Serial interface circuit

The serial interface circuit consists of transmitter DS14C88, receivers DS14C89A and the UART (INS82C50A). The convert TTL compatible signals sent from the UART to −12V to +12V signals conforming to the EIA standard, and output them via the RS-232 connector. The convert the EIA level reception signal to the TTL level and send it to the UART. The functional configuration of the UART is programmed by software via the data bus.

The UART performs a serial-to-parallel conversion of data characters received from a peripheral device or a MODEM, and a performs a parallel-to-serial conversion of data characters received from the CPU. The CPU can read the complete status of the UART any time during the functional operation. Status information includes the type and condition of the transfer operations performed by the UART, and provides error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator. Also the UART has a complete modem control capability and a processor-interrupt system that minimizes the computing time for handling the communications link.

When the CPU assigns one of the address 3F8H through 3FFH or 2F8H throu 2FFH as an I/O address, the HIGH level CSCOMB signal sent from the VG301A (Gate Array) is emitted to the UART. The UART therr selects the internal register to be ZORC connected to the data bus according to the state of the DLAB (Divisor Latch Access Bit). The DLAB is bit 7 of the line control register. Table lists the state of registers indicates at each I/O address, and the table lists the bit assignment of each register.

I/O Address	A2	A1	A0	SIORD	SIOWR	DLAB	
3F8H or 2F8H	L	L	L	L	H	X	Receive buffer register
3F8H or 2F8H	L	L	L	H	L	X	Transmit holding register
3F8H or 2F8H	L	L	L	*	*	1	Divisor latch LSB
3F9H or 2F9H	L	L	H	*	*	1	Divisor latch LSB
3F9H or 2F9H	L	L	H	*	*	0	Interrupt enable register
3FAH or 2FAH	L	H	L	*	*	X	Interrupt identification register
3FBH or 2FBH	L	H	H	*	*	X	Line control register
3FCH or 2FCH	H	L	L	*	*	X	Modem control register
3FDH or 2FDH	H	L	H	*	*	X	Line status register
3FEH or 2FEH	H	H	L	*	*	X	Modem status register

*: $\overline{\text{SIORD}}$ becomes LOW at read operation
$\overline{\text{SIOWR}}$ becomes LOW at write operation
X: Not applicable.

I/O Address	Bit	Description
~~3F9H or 2F9H~~	~~0~~	~~H: Enable data~~
Interrupt enable register	1	H: Enable TX holding register empty interrupt
	2	H: Enable receive line status interrupt
	3	H: Enable modem status interrupt
	4 – 7	Always LOW
3FAH or 2FAH Interrupt identification register	0	H: No interrupt pending
	1	Interrupt identification bit 0
	2	Interrupt identification bit 1
	3 – 7	Always LOW
3FBH or 2FBH Line control register	0	Word length select bit 0
	1	Word length select bit 1
	2	Number of stop bit
	3	Parity enable
	4	Even parity select
	5	Stuck parity
	6	Set break
	7	Divisor latch access bit (DLAB)
3FCH or 2FCH Modem control register	0	Data terminal ready (DTR)
	1	Request to send (RTS)
	2	Out 1
	3	Out 2
	4	Loopback
	5 – 7	Always LOW
3FDH or 2FDH Line status register	0	Data ready (DR)
	1	Overrun error (OR)
	2	Parity error (PE)
	3	Framing error (FE)
	4	Break interrupt (BI)
	5	Transmit holding register empty (THRE)
	6	TX Shift empty (TSRE)
	7	Always LOW
3FEH or 2FEH Modem status register	0	Delta clear to send (DCTS)
	1	Delta data set ready (DDSR)
	2	Trailing edge ring indicator (TERI)
	3	Delta data carrier detect (DDCD)
	4	Clear to send (CTS)
	5	Data set ready (DSR)
	6	Ring indicator (RI)
	7	Delta carrier detect (DCD)

3-13. Speaker interface

A small, permanent magnet speaker is used in the sound system. The speaker can be driven from one or two of sources. It also can be driven by the SCM, CE-462M (modem).

- An LZ95H12 output bit
- A timer clock channel, output programmable within the function of the V40 timer. The timer gate can also be controlled by the LZ95H12 PPI output port.

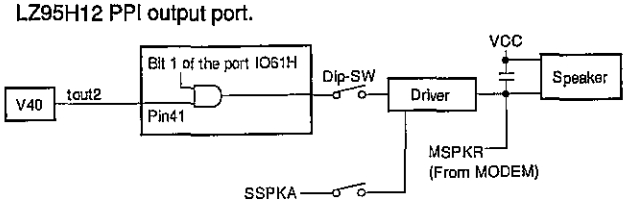


Fig. 3-15 Speaker controll circuit

3-14. RTC/CMOS RAM circuit

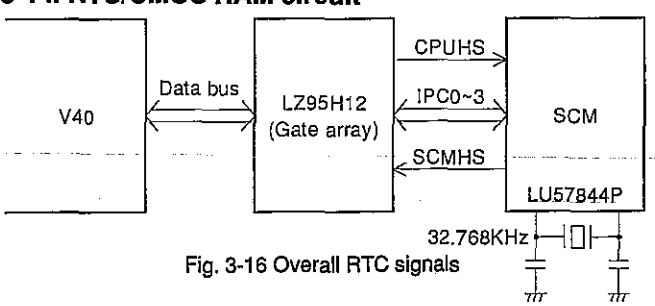


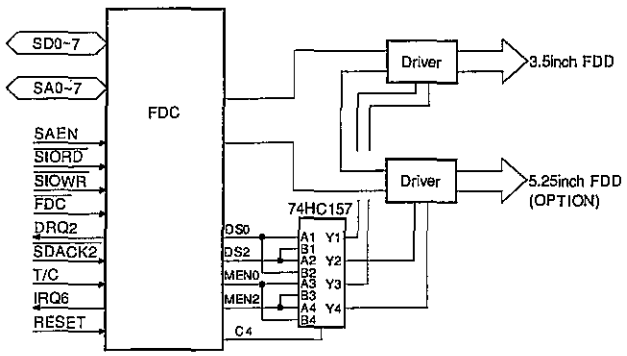
Fig. 3-16 Overall RTC signals

The SCM has a 32.768KHz crystal oscillator for the timer clock besides the program executing oscillator, and divided to cause an interrupt to the SCM itself at the given interval. Timer clock is counted in this interrupt routine and stored in the internal RAM (C-MOS RAM). This value can be read by the V40 via the LZ95H12 by means of handshaking.

For setup data are contained in SCM internal RTC and others, they can be read and written from V40 via LZ95H12 as handshaked with SCM, similar as RTC.

3-15. FDD interface circuit

The FDD interface circuit supports two floppy disk units at a maximum. Fig. 3-16 shows the block diagram. A TC8566F floppy disk controller is used to interface the floppy disk units with the CPU.



NOTE: The 74HC157 is used to select between the built-in 3.5 inch FDD and optional 5.25 inch FDD for drive A in the set-up menu.

Fig. 3-16 FDD interface block diagram

3-15-1. TC8566F floppy disk controller

The TC8566F floppy disk controller contains a VFO and peripheral logic circuit on a single chip.
Two control registers, main status register, and data register are on the chip. Table 3-3 shows the relation between address line and registers.

AEN	$\overline{CS}$	A7	A6	A5	A4	A3	A2	A1	A0	Function
H	X	X	X	X	X	X	X	X	X	No selection
X	H	X	X	X	X	X	X	X	X	
X	X	L	X	X	X	X	X	X	X	
X	X	X	L	X	X	X	X	X	X	
X	X	X	X	L	X	X	X	X	X	
X	X	X	X	X	L	X	X	X	X	
X	X	X	X	X	X	H	X	X	X	
L	L	H	H	H	H	L	L	L	L	Prohibit
L	L	H	H	H	H	L	L	L	H	
L	L	H	H	H	H	L	L	H	L	Control register-0
L	L	H	H	H	H	L	L	H	H	Control register-1
L	L	H	H	H	H	L	H	L	L	Main status register
L	L	H	H	H	H	L	H	L	H	Data register
L	L	H	H	H	H	L	H	H	L	No selection
L	L	H	H	H	H	L	H	H	H	

Table 3-3

3-15-1-1. Control register-0

This an 8-bit write only register.

Bit position	Symbol	Name	Significance
D7	MEN3	Motor enable-3	Control bit to control the motor in the No. 3 drive unit.
D6	MEN2	Motor enable-2	Control bit to control the motor in the No. 2 drive unit.
D5	MEN1	Motor enable-1	Control bit to control the motor in the No. 1 drive unit.
D4	MEN0	Motor enable-0	Control bit to control the motor in the No. 0 drive unit.
D3	ENID	Enable INT & DMA request	Used to set INTRQ and DRQ2 into effect. When this bit is at a low. INTRQ and DRQ2 stay inactive.
D2	$\overline{FRST}$	Not FDC reset	Used to reset the internal FDC. When this bit is 0, the FDC block is reset.
D1	DSB	Drive select B	Used to select FDC. The following is selected with DSB and DSA. (0, 0): No. 0 drive unit (0, 1): No. 1 drive unit (1, 0): No. 2 drive unit (1, 1): No. 3 drive unit But, if CDS is low, those bits are not in effect and bits are not in effect and the internal FDC select signal becomes effective. All bits will be cleared when RESET is set high.
D0	DSA	Drive select A	

All bits will be cleared when RESET is set high.

Table 3-4

3-15-1-2. Control register-1

This an 8-bit write only register.

Bit position	Symbol	Name	Significance
D3	C3	Control-5	These bits are open to user. Bit state appears on C5 and C4. If C4 is connected with MIN, for instance, the mini-floppy disk can be changed to the standard floppy disk by means of software.
D4	C4	Control-4	
D2	SBM	Standby mode	This bit indicates standby mode. Standby mode would not occur when this bit is at 0.
D0	FDCTC	FDC terminal counter	Used to control the FDC terminal count. When data transfer is terminated in the non-DMA mode, the terminal count is sent to the internal FDC block in reference to this bit.

Table 3

All bits will be cleared when RESET is set high. For data bus, D7, D5, D3, D1, are bit enable signal for D6, D4, D2, and D0, it is possible to change bit independently. For instance, writing 03H changes only FDCTC to 1 without changing the contents of C6, C4, and SBM.

3-15-2. Interfacing the FDC register with CPU

Interfacing the FDC register with CPU

The FDC has two registers which can be accessed by the main system processor. The one is main status register and the other is data register. The main status register indicates the FDC status information and can be accessed at any time. The 8-bit data register stores data, command, parameter, and FDD status. Data byte is written in the data register or read from the data register for programming or to obtain the results after command execution. The main status register is read only to facilitate data transfer between the FDC and the processor. The following shows the relation among the main status register, data register, $\overline{IOR}$, $\overline{IOW}$, and $\overline{CS}$.

Condition: A7=A6=A5=A4=A2=1, A3=A1=0, AEN=0

$\overline{CS}$	A0	$\overline{IOR}$	$\overline{IOW}$	Function
Low	Low	Low	Low	Prohibited
Low	Low	Low	High	Main status register read
Low	Low	High	Low	Prohibited
Low	High	Low	Low	Prohibited
Low	High	Low	High	Data register read
Low	High	High	Low	Data register write

Table 3-6

Each main status register bit is defined as in Table 3-7.
The main status register bits, RQM and DIO, indicate whether the data register is ready or which direction data are on the data bus.

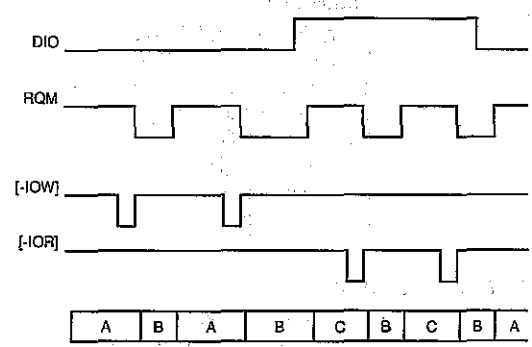


Fig. 3-17 Main status register timing

A (DIO=low, RQM=high):
Data register is enabled to write by the processor.
B (RQM=low)
Data register is not ready.
C (DIO=high, RQM=high)
Data register is read by the processor and a next data byte is already on.

Bit Position	Symbol	Name	Significance
D7	RQM	Request for master	Indicates that data are sent to the processor from the data register, or it is ready to receive data from the processor.
D6	DIO	Data input/output	Indicates data transfer direction when transferring data between the data register and the process or. A high on this line indicates that data are transferred from the data register to the processor. A low on this line indicates that data are transferred from the processor to the data register.
D5	NDM	Non-DMA mode	Indicates that the FDC is in the non-DMA mode. This bit can be active only in the execution phase of the non-DMA mode. A low on this line indicates that the execution phase has been completed.
D4	CB	FDC busy	This bit is set when a read-wirte related command is in execution or during execution of command phase or result phase.
D3	D3B	FDD3 busy	Indicates that the NO. 3 drive is in the seek mode.
D2	D2B	FDD2 busy	Indicates that the NO. 2 drive is in the seek mode.
D1	D1B	FDD1 busy	Indicates that the NO. 1 drive is in the seek mode.
D0	D0B	FDD0 busy	Indicates that the NO. 0 drive is in the seek mode.

Table 3-7. Main status register

The FDC may execute 15 different commands. Execution takes place with a multiple byte transfer by the processor, and results after command execution is indicates after multiple byte transfer to the processor. For multiple number of bytes are transferred between the FDC and the processor, it may be assumed to constitute the following blocks.

Command phase:

The FDC receives from the processor information required for the given operation.

Execution phase:

The FDC executes the given command.

Result phase:

After completion of the operation, the result status information are sent to the processor.

During execution of command phase and result phase, the processor needs to read the main status register before the byte information is written in the data register or read byte information from the data register. In order to write command and parameter bytes in the FDC, the main status register bit D7 must be high and bit D5 low. For majority of commands requires a multiple bytes, the main status register must be read before transferring bytes to the FDC. Also, the main status register bits D7 and D5 must be high before reading bytes from the data register during execution of the result phase. For the command phase and result phase, the main status register must be read before transferring bytes to the FDC, but may not be required necessarily for the execution phase. When the FDC is in the non-DMA mode, receive of data bytes (when the FDC is reading data from the FDD), INT (INT=1) is caused. If $\overline{IOR}$ ($\overline{IOR}$=0) is issued, it not only send data on the data bus, INT may also be reset. However, if the processor may not be fast enough to handle the interrupt (within 13μs in the MFM mode), the main status register is interrogated. The bit D7 (RQM) function as INT. In the same manner, INT may be reset with $\overline{IOW}$ while write command is in execution.

INT is not issued while the execution phase is being executed when the FDC is in the DMA mode. The FDC issues DRQ (DMA request) when data bytes are ready, to which the controller set $\overline{DAC}$ low (DMA acknowledge) and $\overline{IOR}$ low to respond to it. DRQ is reset when DMA acknowledge is set low for a read related command. For a write related command, $\overline{IOW}$ functions the same as $\overline{IOR}$. An interrupt is request upon completion of the execution phase (TC received) which indicates the start of the result phase. After reading the first data byte in the result phase, INT is forced to reset. In the result phase, all data bytes shown in the command list must be read. For instance, in the result phase of read data command, there are seven data bytes. In order to finish the read data command, these all seven data bytes must be read. Otherwise, the FDC may not receive a new command. For other commands, all data bytes must have been read in the result phase. The FDC has five status registers. The above mentioned main status register may be read at any time by the procesor. Four result status registers (ST0, ST1, ST2, ST3) can be used only in the result phase and can be read at the termination of command. Size of the result status register depends on the command executed. Sequence of data bytes sent to the FDC in the command phase and data bytes read from the FDC in the result phase is as shown in the command list. In other words, a command code must be first sent, to be followed by other bytes in the given order. So, nothing could be short for the command phase and the result phase. When the last data byte of the command phase is sent to the FDC, the execution phase takes place automatically. Similarly, after reading the last data byte in the result phase, the command automatically terminates and the FDC becomes ready to accept a next command.

3-16. Keyboard interface

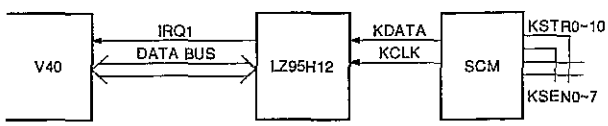
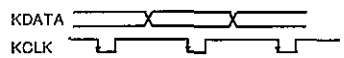


Fig. 3-18 Overall key signals

The SCM issues strobe through KSTR0~10 at every 6ms to scan the level on KSEN0~7 to sense key depression. The code is sent to the LZ95H12 on KDATA with a clock on KCLK. The following shows its timing.



After receiving the code in the shift register, the LZ95H12 turns IRQ1 high with which the V40 read the data from the LZ95H12.

(2) Keyboard LEDs (CAPS LOCK, NUM LOCK, SCRL LOCK)

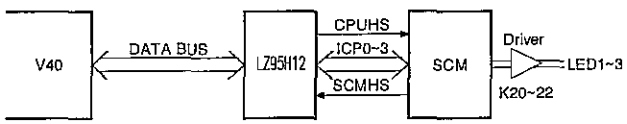
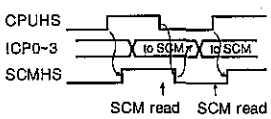


Fig. 3-19 Keyboard LEDs

LED is activated after the SCM receives the command sent from the V40 via the LZ95H12. Communication between the LZ95H12 and the SCM is carried out by handshaking. The data are sent on four bidirectional bus ICP0~3. The signal CPUHS is used from the LZ95H12 for handshake control and SCMHS from the SCM. The figure below shows an example of data transfer.



3-17. LCD control circuit

3-17-1. I/O mapping

The table below shows the I/O address assignment of the MDA and ATT (CGA).

I/O Address	Read/ Write	Bit	Description
77H	R/W	0	ATT (CGA/MDA). 1: ATT (CGA) Mode, 0: MDA Mode
		4	RVVD (Reverse video) 1: Reverse video enable
78H	R/W	4	CURBLK0, 1 (Cursor Blink Rate 0, 1)
		5	0: Steady 1: 1/64 S blink 2: 1/32 S blink 3: 1/16 S blink
		6	ATTBLK0, 1 (Attribute blink Rate 0, 1)
		7	0: Steady 1: 1/64 S blink 2: 1/32 S blink 3: 1/16 S blink
Index Register 3B4H (ATT=0) 3D4H (ATT=1)	W	0	IDX0 (Index Address 0)
		1	IDX1 (Index Address 1)
		2	IDX2 (Index Address 2)
		3	IDX3 (Index Address 3)
		4	IDX4 (Index Address 4)
		5	Not used
		6	Not used
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0AH)	W	0	CSSL0 (Cursor Start Scan Line 0)
		1	CSSL1 (Cursor Start Scan Line 1)
		2	CSSL2 (Cursor Start Scan Line 2)
		3	CSSL3 (Cursor Start Scan Line 3)
		4	CSSL4 (Cursor Start Scan Line 4)
		5	CSSL5 (Cursor Start Scan Line 5)
		6	CSSL6 (Cursor Start Scan Line 6)
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0BH)	W	0	CESL0 (Cursor End Scan Line 0)
		1	CESL1 (Cursor End Scan Line 1)
		2	CESL2 (Cursor End Scan Line 2)
		3	CESL3 (Cursor End Scan Line 3)
		4	CESL4 (Cursor End Scan Line 4)
		5	CESL5 (Cursor End Scan Line 5)
		6	CESL6 (Cursor End Scan Line 6)
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0CH)	W	0	DSA8 (Display Start Address 8)
		1	DSA9 (Display Start Address 9)
		2	DSA10 (Display Start Address 10)
		3	DSA11 (Display Start Address 11)
		4	DSA12 (Display Start Address 12)
		5	DSA13 (Display Start Address 13)
		6	Not used
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0DH)	W	0	DSA0 (Display Start Address 0)
		1	DSA1 (Display Start Address 1)
		2	DSA2 (Display Start Address 2)
		3	DSA3 (Display Start Address 3)
		4	DSA4 (Display Start Address 4)
		5	DSA5 (Display Start Address 5)
		6	DSA6 (Display Start Address 6)
		7	DSA7 (Display Start Address 7)
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0EH)	R/W	0	CSA8 (Cursor Address 8)
		1	CSA9 (Cursor Address 9)
		2	CSA10 (Cursor Address 10)
		3	CSA11 (Cursor Address 11)
		4	CSA12 (Cursor Address 12)
		5	CSA13 (Cursor Address 13)
		6	Not used
		7	Not used
Data Register 3B5H (ATT=0) 3D5H (ATT=1) (Register Address=0FH)	R/W	0	CSA0 (Cursor Address 0)
		1	CSA1 (Cursor Address 1)
		2	CSA2 (Cursor Address 2)
		3	CSA3 (Cursor Address 3)
		4	CSA4 (Cursor Address 4)
		5	CSA5 (Cursor Address 5)
		6	CSA6 (Cursor Address 6)
		7	CSA7 (Cursor Address 7)
3B8H (ATT=0)	W	0	Not used
		1	Not used
		2	Not used
		3	0: Video disabled, 1: Video enabled
		4	Not used
		5	MSB of attribute is 0: intensity, 1: blink
		6	Not used
		7	Not used
3D8H (ATT=1)	W	0	0: 40 x25 Alpha, 1: 80 x 25 Alpha
		1	0: Character Mode, 1: Graphics Mode
		2	Not used
		3	0: Video disabled, 1: Video enabled
		4	Not used
		5	MSB of attribute is 0: intensity, 1: blink
		6	Not used
		7	Not used
3B8H (ATT=0)	R	0	Horizontal sync
		1	Not used (0 read)
		2	Not used (0 read)
		3	Black/white video
		4	Not used (0 read)
		5	Not used (0 read)
		6	Not used (0 read)
		7	Not used (0 read)
3D8H (ATT=1)	R	0	Display enable
		1	Not used (0 read)
		2	Not used (0 read)
		3	Vertical sync
		4	Not used (1 read)
		5	Not used (1 read)
		6	Not used (1 read)
		7	Not used (1 read)
3DEH (ATT=1)	W	0	640 x 200 APA 0: two 16K alpha pages, 1: one 32K alpha page
		1	Not used
		2	Not used
		3	0: Select low page, 1: select high page
		4	Not used
		5	Not used
		6	0: underline disabled, 1: underline enabled
		7	Not used

3-17-2. VRAM mapping

The LCD control circuit has four 256K-bit (64 x 4-bit) DRAM chips which are used for VRAM, character generator table, and system work area. A 4KB area is used as a VRAM (display buffer) in the MDA mode, or 16KB in the CGA mode, or 32KB in the ATT mode. The ATT mode is an expanded version of the CGA mode which supports 640 x 400 APA mode.

The figure next shows the display buffer memory allocation in each mode.

The 4Kbytes monochrome adapter display buffer is mirrored into eight different address 4Kbytes address ranges. The 16Kbytes graphics adapter display buffer is mirrored into two 16Kbytes address ranges.

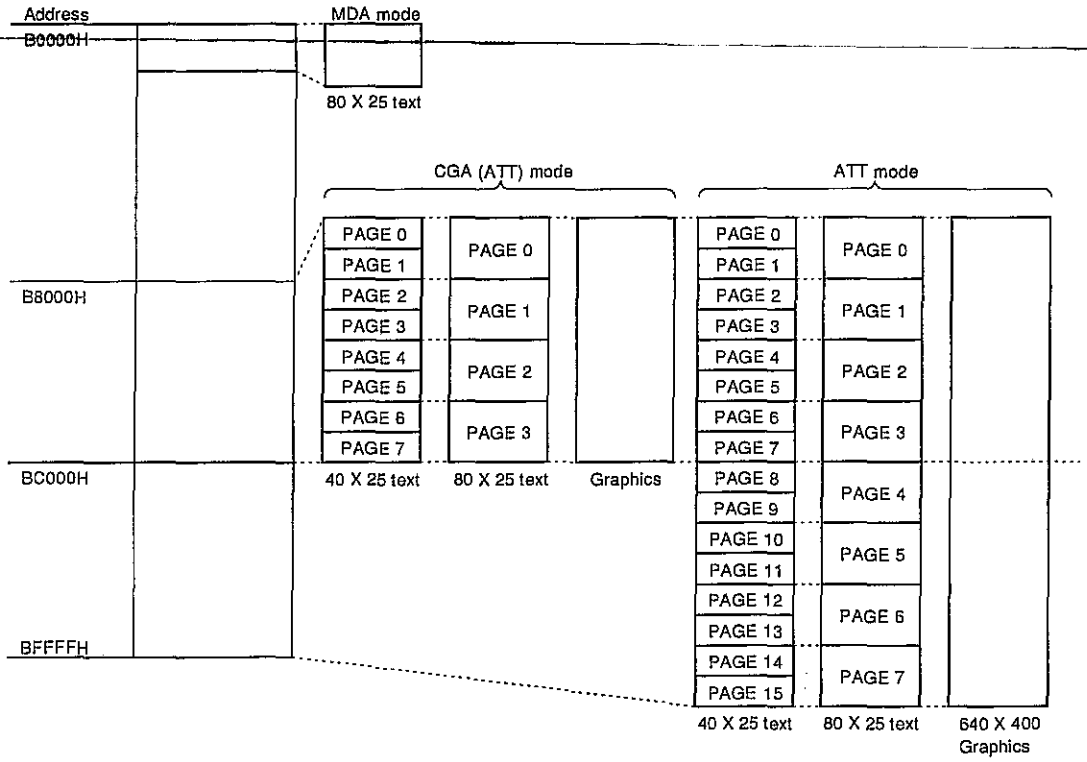


Fig. 3-20 Display buffer memory allocation

3-17-2-1. Text mode

- 80 x 25 text (MDA)
- 80 x 25 text (CGA/ATT)
- 40 x 25 text (CGA/ATT)

The LCD control circuit supports the text 80 x 25 MDA alphanumeric mode and 80 x 25/40 x 25 CGA/ATT alphanumeric mode.

Every character to be displayed has one byte of character code with one byte of attribute. The attribute has four functions described next.

Background			Foreground			Display mode
R	G	B	R	G	B	
0	0	0	0	0	0	Non display
0	0	0	0	0	1	With underline
0	0	1	1	1	1	Normal display
1	1	1	0	0	0	Reverse display

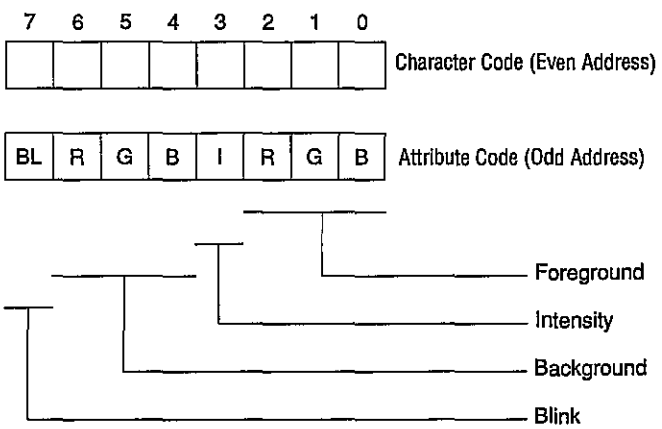


Fig. 3-21 Attribute assignment

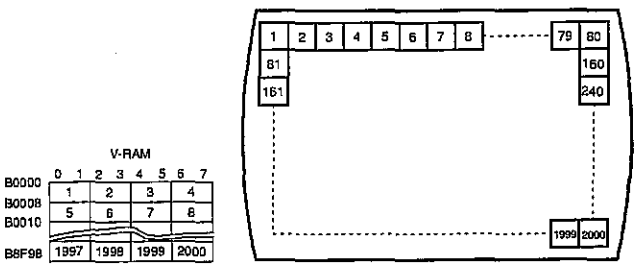


Fig. 3-22 VRAM map in the 80 x 25 text mode (MDA)

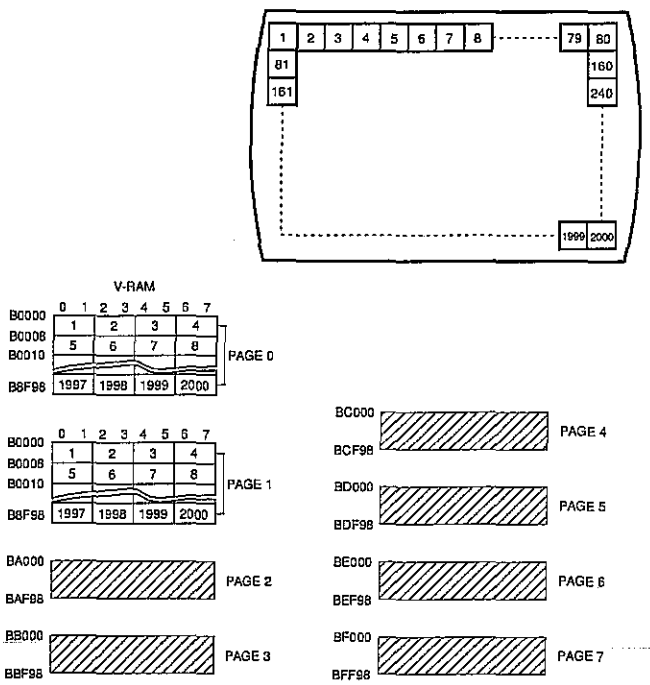


Fig. 3-23 V-RAM map in the 80 x 25 text mode (ATT)

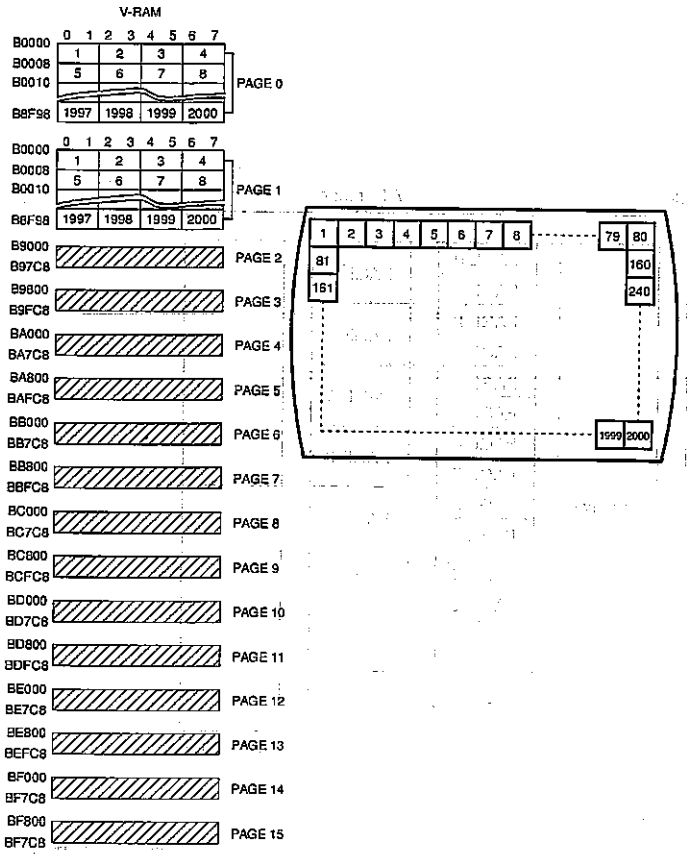


Fig. 3-24 V-RAM map in the 40 x 25 text mode (ATT)

3-17-2-2. Graphics mode

- 320 x 200 graphics (ATT)
- 640 x 200 graphics (ATT)
- 640 x 400 graphics (ATT)

The LCD circuit supports the 320 x 200 graphics mode, 640 x 200 graphics mode, and 640 x 400 graphic mode.
And this circuit uses black for the foreground color and white for the background color in both 640 x 200 and 640 x 400 graphics modes. Each pixel in the 320 x 200 graphics mode is presented by a 2 x 2 block of LCD screen pixels.

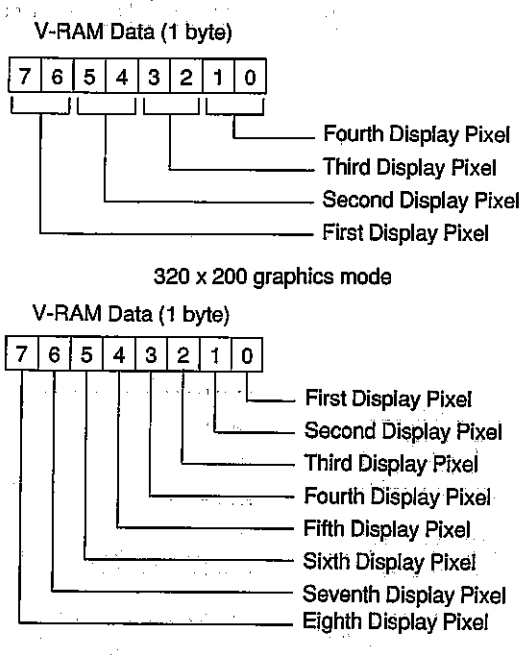


Fig. 3-25 Bit assignment

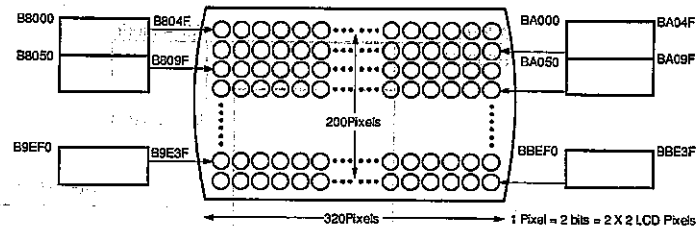


Fig. 3-26 V-RAM map in the 320 x 200 graphics mode

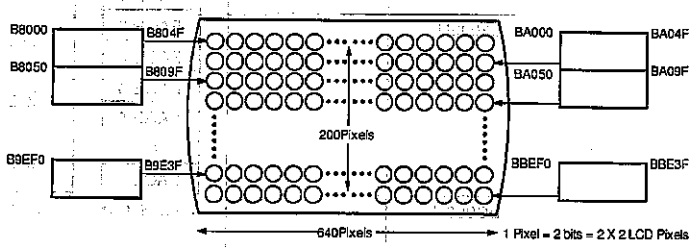


Fig. 3-27 V-RAM map in the 640 x 200 graphics mode

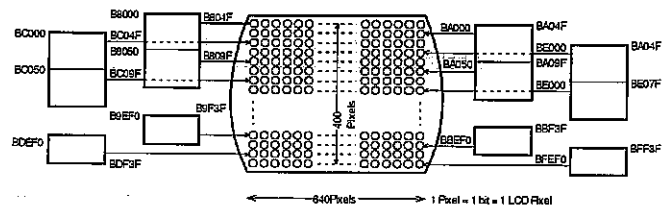


Fig. 3-28 V-RAM map in the 640 x 400 graphics mode

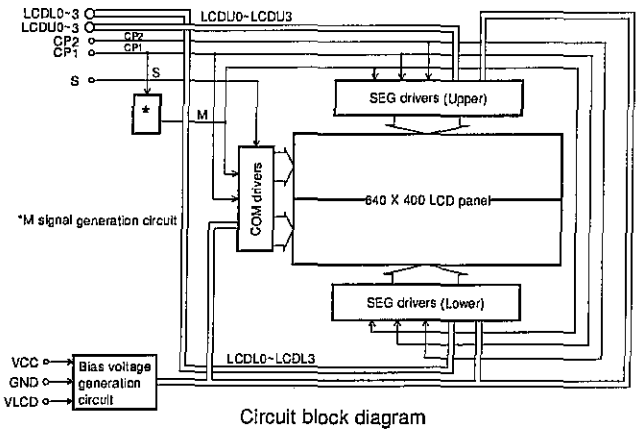
CHAPTER 4. LCD UNIT

4-1. Structure

A 640 x 400 full dot graphics display unit is employed for the LCD unit which consists of a printed circuit board that contains the LCD panel and its electronic circuits, an electrically connected film carrier LSI chip, and a mechanically held plastic chassis, and a bezel.

4-2. Operational theory

Circuit block diagram and interface signals are shown in the figure next.

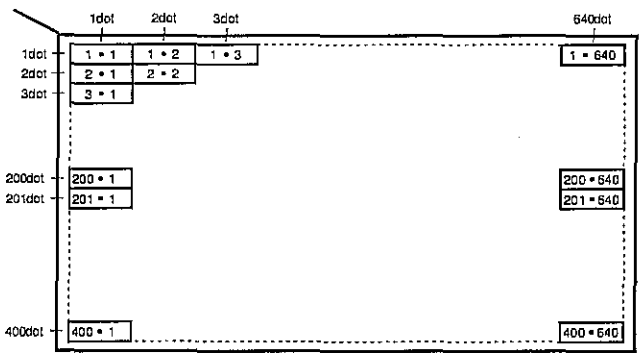


Circuit block diagram

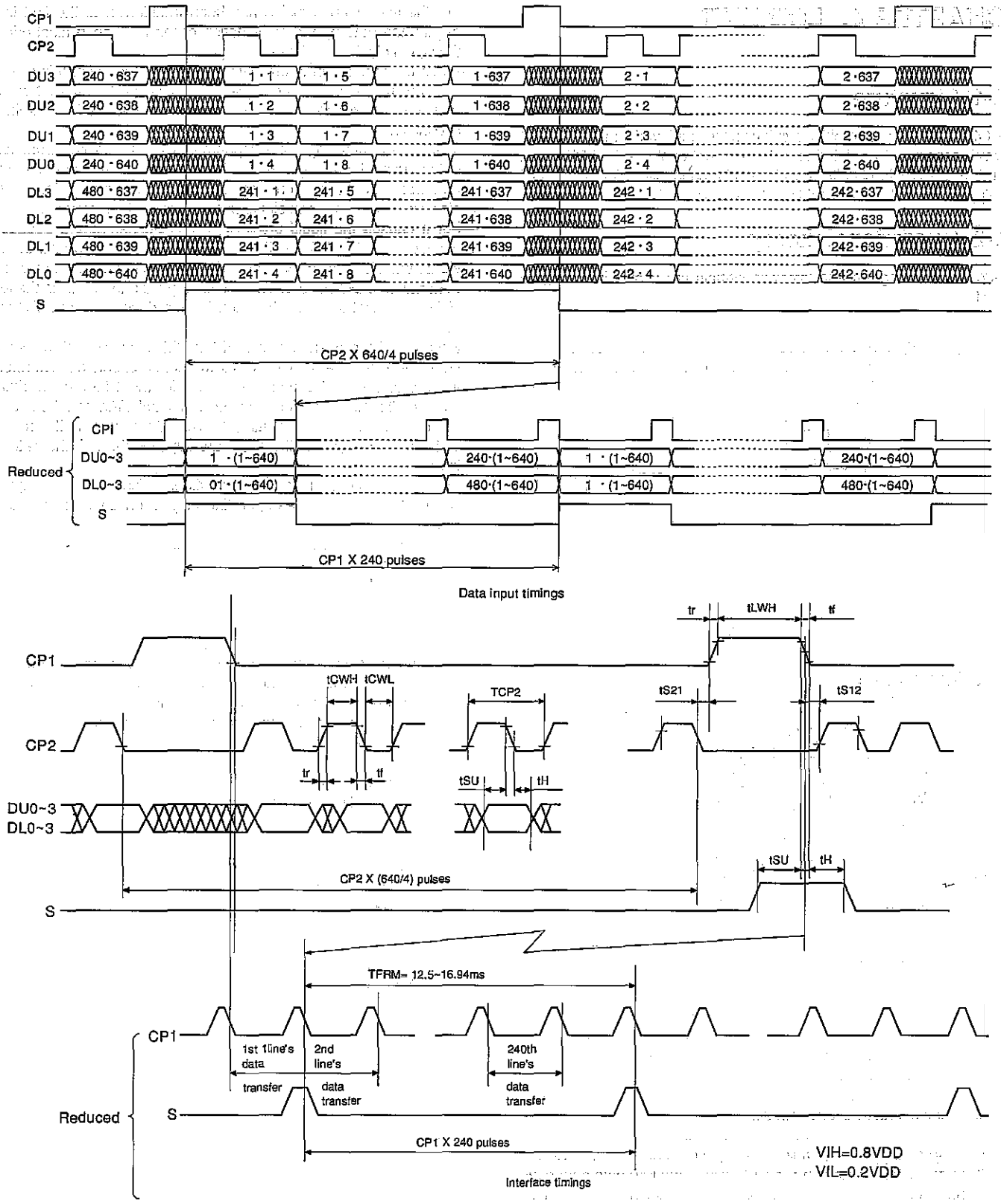
Interface signals

Pin NO.	Symbol	Description	Active signal level
1	S	Scan start signal	"H"
2	CP1	Input data latch signal	H → L
3	CP2	Data input clock signal	H → L
4	PVBKL	Back light power control signal	H (ON), L (OFF)
5	GND	Ground	—
6	V_{LCD}	Liquid crystal drive power (–)	—
7	LCDU0	Display data signal (upper half)	H(ON), L(OFF)
8	LCDU1	〃	〃
9	LCDU2	〃	〃
10	LCDU3	〃	〃
11	LCDL0	Display data signal (lower half)	H(ON), L(OFF)
12	LCDL1	〃	〃
13	LCDL2	〃	〃
14	LCDL3	〃	〃

The display screen of this unit is configured of 640 x 400 dots two screens, each screen driven with 1/200 duty.
An 80-pin LSI is used for the LCD driver that consists of a shift register, latch, and LCD drive circuit.
Data are inputted for each line (640 dots) of the screen. From the left side of the screen, 4-bit parallel data are sent one at a time via the shift register with the clock pulse CP2. When the 640 dots data have been received for one display line, the data are latched as a parallel data with respect to the 640 signal electrodes at a high to low transition of the latch signal CP1 to send the drive signal by the drive circuit to the corresponding electrodes.
For the scan start signal S has been transferred at the first line to display the data by the combination of the LCD scan electrode and the signal electrode address voltage.
While the first line data are being displayed, the second line display data are received. Upon completing transfer of 640 data, it will then be latch at a high to low transition of CP1 to change it to display the second line.
In this way, data input are repeated to the 200th line from top to bottom using the multiplexed method. After completion of one screen (one frame), data are then received from the first line again. The scan start signal S is the scan signal to drive horizontal electrode.
For it causes the liquid crystal elements to deteriorate because of chemical reaction if DC voltage is added to the LCD panel, the drive signal waveform must be inverted at every screen in order to avoid generation of DC voltage. The circuit employed to do this is the async M signal circuit from which generated the drive waveform AC signal M.
Because of the characteristics of the CMOS driver LSI, power consumption increases as CP2 clock frequency increases. Therefore, it incorporates four shift registers to transfer the 4-bit parallel data via these shift registers to decrease the CP2 clock data transfer speed. In this circuit, a 4-bit display data (LCDU0 ~ 3 for upper half screen and LCDL0 ~ 3 for lower half screen) are supplied through the data input lines.
To further abate the power consumption, it also has a data input bus line system which comes operating only when appropriate data are received.
The following shows the screens signal electrode data inputs vs. driver LSI chip select signal.
The driver LSI of the left end screen is first elected. When the 80-dot data (20CP2) has been supplied, the driver LSI adjacent to right is then selected. This continues until the data are sent to the driver LSI at the screen right.
This process occurs simultaneously for signal electrode signal LSIs of both screens. In this manner, data of both screens are supplied via 4-bit bus line starting from the left end of the screen.
For the graphics display unit does not contain the refresh RAM, it becomes necessary to input the data and timing pulse when the screen is still.
The following shows the dot table of the display, data input timing chart, and input signal timing.



NOTE : 1 and 2 indicate first horizontal dot and second dot.
Display dot chart.



Rated interface timings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Frame cycle	T_{FRM}	13.15		16.94	ms
Clock cycle	T_{CP2}	300			ns
"H" level clock width	t_{CWH}	125			ns
"L" level clock width	t_{CWL}	125			ns
"H" level latch clock width	t_{LWH}	130			ns

Data setup time	t_{SU}	100			ns
Data hold time	t_H	60			ns
Clock allowable time from CP2 ↓ to CP1 ↑	t_{S21}	0			ns
Clock allowable time from CP1 ↓ to CP2 ↑	t_{S12}	0			ns
Clock rise and fall time	tr, tf			30	ns

CHAPTER 5. POWER SUPPLY CIRCUIT

5-1. Block diagram

Fig. 5-1 shows the block diagram.

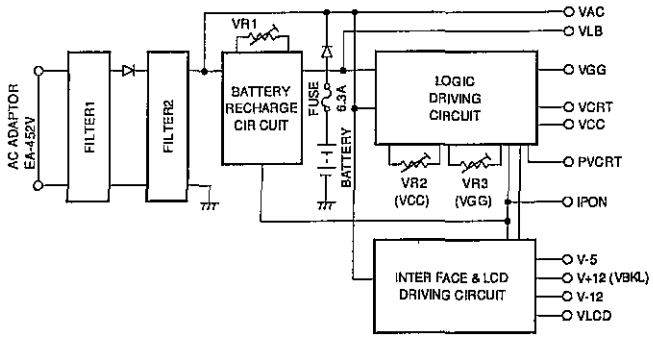


Fig. 5-1 Block diagram

5-2. Electric characteristics

(1) Input voltage

This power supply unit could be operated by using one of the following input voltage and the combination of them.

a. AC adaptor (CE-452V) 9.0V±0.5V 2.5A
b. Lead battery (UBATZ1003ACZZ) 5.0V–6.5V 4.2Ah

(2) Non-load current

Table 6-2 shows the input current from the battery connector when all outputs are non-load with 6.3V input from battery connector without using AC adaptor.

IPON	CURRENT
Low	less than 500μA
High	less than 200mA

Table 5-1

(3) Monitering output

The power supply unit outputs the following 2 monitering outputs.

a. VLB

The VLB tells the battery voltage to the system.
The output connect the battery terminal through the diode.

b. VAC

The VAC tells whether the AC adaptor is connected or not.
The output should be more than 6.5V while the AC adaptor is connected.

(4) Battery voltage detection

When VLB voltage is changed according to the value in table 6-2 without connecting AC adaptor, the VGG output voltage satisfies the value in the table 2.
(IPON is set to low. VGG load is adjusted to 1mA.)

VLB voltage (V)	VGG voltage (V)
from 0 to 4.0	less than 0.3
from 0 to 5.1	4.75 – 5.25
from 6.0 to 4.8	4.75 – 5.25
from 6.0 to 4.0	less than 0.3

Table 5-2

(5) Output voltage

The power supply unit could supply the following outputs by either the inputs of AC adaptor or battery.
The converting efficiency should be more than 70% when using the battery as the input.

a. VGG (+5V±0.25V)

The VGG output is always supplied to the logic ICs on the Main PCB.

b. VCC (+5V±0.25V)

The VCC output is supplied to the logic ICs on the Main PCB, LCD unit, FDD unit, and HDD unit while the control signal IPON is high.

c. V+12, V_{BKL} (+12V±0.6V)

The V+12 and V_{BKL} output is supplied to the ICs and Inverter for CCFT Backlight while the IPON is high.

d. V–12 (–12V±1.0V)

The V–12 output is supplied to the ICs while the IPON is high.

e. V–5 (–5V±0.25V)

The V–5 output is supplied to the optional MODEM unit while the IPON is high.

f. VLCD (–24V±1.2V)

The VLCD output is supplied to the LCD unit while the IPON is high.

g. VCRT (+5V±0.25V)

The VCRT output is supplied to the optional CRT adaptor while the control signals IPON and PVCRT are high.

The following table is output characteristics of all outputs.

OUTPUT	CONDITION	VOLTAGE (V)	CURRENT (mA)	RIPPLE (mVp-p)
VGG		5.0±0.25	0.1 ~ 15	less than 100
VCC	IPON = High IPON = Low	5.0±0.25 less than 0.3	300 – 2800	less than 100
V+12 V_{BKL}	IPON = High IPON = Low	12.0±0.6 0±0.3	0 – 270	less than 150
V–12	IPON = High IPON = Low	–12.0±1.0 0±0.3	0 ~ –20	less than 150
V–5	IPON = High IPON = Low	–5.0±0.25 0±0.3	0 ~–20	less than 100
VCRT	PVCRT = High PVCRT = Low	5.0±0.25 less than 0.3	0 ~120	less than 100
VLCD	IPON = High IPON = Low	–24±1.2V 0+0.3	–10 ~–25	less than 200

Table 6-3

NOTES 1) The control signals are from the CMOS IC powered by VGG, and the range of high is 4.0 to 5.25V, low is less than 0.5V.
2) PVCRT = High means IPON = High too.
3) The currents of the VCC is the peak current. It is continuously supplied less than 1.6A.

(6) Input current of IPON, PVCRT, PVBKL

When IPON, PVCRT, is high level (+4.0V) at on mode, the input current of them satisfy the Table 6-4.

	Input current
IPON	less than 1mA
PVCRT	less than 1mA

Table 5-4

5-3. Battery recharge circuit

When the AC adapter or V_{EX} is supplied, if IPON is at low (the set is OFF), the charging characteristic of the battery is as shown in Fig. 6-2. To check the operation, provide a dummy resistor to the battery connector and check points A – D in Fig. 6-2 and Table 6-5.

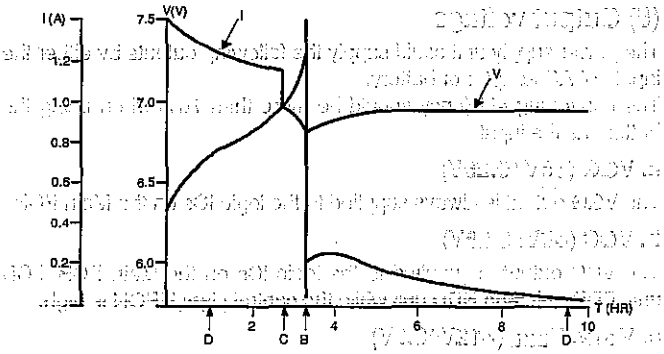


Fig. 5-2 Recharge characteristic

Table 5-5 Recharge circuit test point

Point	Voltage	Current	Remarks
A	6.85±0.05V	10mA	IPON at low, control with VR1.
B	7.5±0.2V	0.8~1.0A	Voltage/current are changed around this point.
C	6.85±0.1V	1~1.3A	Current reduces around this point.
D	6.5±0.2V	1.1~1.4A	Current is constant though voltage is varied.

Time required for charging the battery is about 8 hours when the set is OFF (IPON is at low), and 20 to 30 hours when the set is ON (IPON is at high).

5-4. Description of black/white liquid crystal backlight inverter (type: IV18106)

5-4-1. General

This PWB unit is employed to drive the LCD backlight (cold cathode ray tube) which will be directly installed to the plastic cabinet inside the display. Three connectors are used for the I/O and control signal interfacing.

NOTES:
1. This unit drives the entire backlight circuit with the power supply only, except that it is connected with an external VR and control lines.
2. Since it is an assembly unit, parts replacement and repair are not allowed. In case it has to be replaced with a new one, unfasten the connectors and remove screws.
3. Pay attention to a high tension voltage of 1000V on the secondary side when operating. For wires that are exposed over and below the transformer, these must be treated with care as it may result in wire breakage.
4. Since this unit is compact and low profile, the board height is low, width narrow, and long in the longitudinal direction, it would be liable to damage if subjected to twisting. So, never drop or twist it to avoid possible damage.

5-4-2.Electrical characteristics

(1) Maximum allowable ratings

Parameter	Symbol	Rating
Input voltage	Vin	16V
Input power	Pin	3.6W
Operating temperature	Ta	0~50°C
Storage temperature	Ts	-20~75°C
Operating humidity	RH	80% with maximum wet ball humidity at 35°C

Table 5-6

(2) Electrical characteristics

Parameter	Symbol	Nominal	Note
Input voltage	Vin	DC12V	(9.0~16.0V)
Input current	Iin	0.24A	Lamp load Vin=12V, VR=0Ω
No-load release voltage	Vs	AC100Vrms	
Tube current	IL	5.0mA	
Oscillation frequency	f	65kHz	
Chipping frequency	fch	60kHz	

Table 5-7

The following circuit is used for intensity adjustment.

(3) Connector pin layout

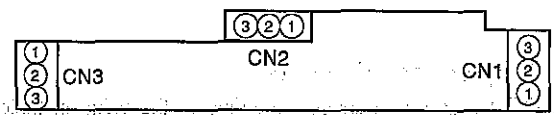


Fig. 5-3
PWB top view

(a) CN1 pin configuration

Pin No.	Signal name	Symbol
①	GND.	GND.
②	N.C	
③	OUT	OUT

(b) CN2 pin configuration

Pin No.	Signal name	Symbol
①	+B supply	+B
②	N.C	
③	GND.	GND.

(c) CN3 pin configuration

Pin No.	Signal name	Symbol
①	Intensity control VR	VR
②	GND.	GND.
③	Control	CONT

5-4-3. Circuit diagram

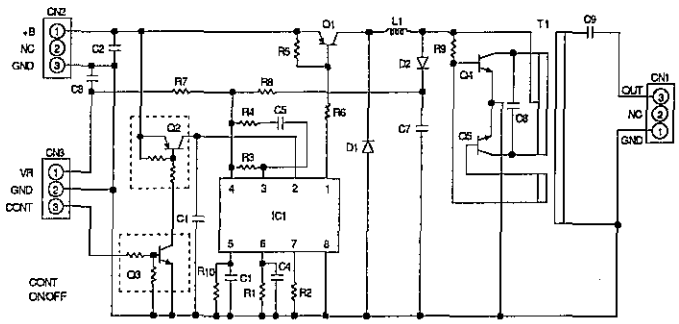


Fig. 5-4

CHAPTER 6. HARD DISK

CP4024 (20MB)

SPECIFICATION SUMMARY

CAPACITY	21.8 Mbytes Formatted

PHYSICAL CONFIGURATION

Head Type	Composite
Disk Type	Plated Thin Film
Actuator Type	Rotary Voice-Coil
Number of Disks	1
Data Surfaces	2
Data Heads	2
Servo	Embedded
Tracks per Surface	627
Track Density	1150 TPI
Track Capacity Formatted	17,408 Bytes
Bytes per Block	512
Blocks per Drive	42,636
Sectors per Track	35 physical; 34 user

PERFORMANCE

Seek Times*	Track to Track: 8 ms Average: 29 ms** Maximum: 50 ms
Average Latency	10.3 ms
Rotation Speed (± .1%)	2913 RPM
Controller Overhead	1 ms
Data Transfer Rate (To/From Media)	1.125
Data Transfer Rate (To/From Buffer)	3.375
Start Time (Power Up)***	
(0-3575 RPM)	typical: 5 seconds maximum: 10 seconds
(0 RPM - READY)	typical: 7 seconds maximum: 15 seconds
Stop Time (Power Down)	typical: 5 seconds maximum: 10 seconds
Start/stop cycles	20,000 min.
Interleave	1:1

* At nominal D.C. input voltages.

** Average seek time is determined by dividing the total time required to seek between all possible ordered pairs of track addresses, by the total number of these ordered pairs.

*** These numbers assume spin recovery is not invoked. If spin recovery is invoked, the max could be 40 sec. Briefly removing power can lead to spin recovery being invoked.

CP4024

READ/WRITE

Interface	Task File
Recording Method	2 of 7 RLL code
Recording Density (ID)	23,148 bits per inch
Flux Density (ID)	15,432 flux reversals per inch

POWER REQUIREMENTS

	TYPICAL		MAX	
	+5V DC ±10%	POWER	+5V DC ±10%	POWER
R/W MODE	750 ma	3.8 W	.789 ma	3.9 w
SEEKING MODE	500 ma	2.5 W	.52 ma	2.59 W
IDLE MODE	300 ma	1.5 W	.388 ma	1.94 W
STANDBY MODE	130 ma	0.65 W	.188 ma	.94 W
SLEEP MODE	70 ma	0.4 W	.120 ma	.60 W
SPIN-UP MODE	1.25 amp	6.25 W	1.45 amp	7.25 W

NOTES:
1) READ/WRITE mode occurs when data is being read from or written to the disk.
2) SEEKING MODE occurs while the actuator is in motion.
3) IDLE MODE occurs when the drive is not reading, writing or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.
4) STANDBY MODE occurs when the motor is stopped, actuator parked and all electronics except interface control is in sleep state. STANDBY MODE will occur after a programmable timeout since last host access occurs. Drive ready and seek complete status exist. The drive will leave STANDBY MODE upon receipt of a command which requires disk access or upon receipt of a spin up command.
5) SLEEP MODE occurs when the host issues the SLEEP command to the drive. SLEEP MODE is the same as STANDBY MODE except that interface control is also powered down. To exit the SLEEP MODE, the Host Reset line on the interface must be asserted. The SRST bit in the Digital Output Register is useful for this purpose.
6) Maximum noise allowed (DC to 1 MHZ, with equivalent resistive load): +5V DC: 2%.
7) SPIN UP MODE current draw is for 5 seconds max.

CP4044 (40MB)

SPECIFICATION SUMMARY

CAPACITY	42.9 Mbytes Formatted

PHYSICAL CONFIGURATION

Head Type	MIG
Disk Type	Plated Thin Film
Actuator Type	Rotary Voice-Coil
Number of Disks	1
Data Surfaces	2
Data Heads	2
Servo	Embedded
Tracks per Surface	1104
Track Density	1400 TPI
Track Capacity Formatted	19,456 Bytes
Bytes per Block	512
Blocks per Drive	83,904
Sectors per Track	39 physical; 38 user

PERFORMANCE

Seek Times*	Track to Track: 8 ms Average: 29 ms** Maximum: 50 ms
Average Latency	10.3 ms
Rotation Speed (± .1%)	2904 RPM
Controller Overhead	1 ms
Data Transfer Rate (To/From Media)	1.25
Data Transfer Rate (To/From Buffer)	3.75
Start Time (Power Up)***	
(0-3575 RPM)	typical: 5 seconds maximum: 10 seconds
(0 RPM - READY)	typical: 7 seconds maximum: 15 seconds
Stop Time (Power Down)	typical: 5 seconds maximum: 10 seconds
Start/stop cycles	20,000 min.
Interleave	1:1

* At nominal D.C. input voltages

** Average seek time is determined by dividing the total time required to seek between all possible ordered pairs of track addresses, by the total number of these ordered pairs.

*** These numbers assume spin recovery is not invoked. If spin recovery is invoked, the max could be 40 sec. Briefly removing power can lead to spin recovery being invoked.

CP4044

READ/WRITE

Interface	Task File
Recording Method	2 of 7 RLL code
Recording Density (ID)	32,729 bits per inch
Flux Density (ID)	21819 flux reversals per inch

POWER REQUIREMENTS

	TYPICAL		MAX	
	+5V DC ±10%	POWER	+5V DC ±10%	POWER
R/W MODE	750 ma	3.8 W	.789 ma	3.9 W
SEEKING MODE	500 ma	2.5 W	.52 ma	2.59 W
IDLE MODE	300 ma	1.5 W	.388 ma	1.94 W
STANDBY MODE	130 ma	0.65 W	.188 ma	.94 W
SLEEP MODE	70 ma	0.4 W	.120 ma	.60 W
SPIN-UP MODE	1.25 amp	6.25 W	1.45 amp	7.25 W

NOTES:
1) READ/WRITE mode occurs when data is being read from or written to the disk.
2) SEEKING MODE occurs while the actuator is in motion.
3) IDLE MODE occurs when the drive is not reading, writing or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.
4) STANDBY MODE occurs when the motor is stopped, actuator parked and all electronics except interface control is in sleep state. STANDBY MODE will occur after a programmable timeout since last host access occurs. Drive ready and seek complete status exist. The drive will leave STANDBY MODE upon receipt of a command which requires disk access or upon receipt of a spin up command.
5) SLEEP MODE occurs when the host issued the SLEEP command to the drive. SLEEP MODE is the same as STANDBY MODE except that interface control is also powered down. To exit the SLEEP MODE, the Host Reset line on the interface must be asserted. The SRST bit in the Digital Output Register is useful for this purpose.
6) Maximum noise allowed (DC to 1 MHZ, with equivalent resistive load): +5V DC: 2%.
7) SPIN UP MODE current draw is for 5 seconds max.
8) The drive has two sets of jumpers E1, E2, E3, near the interface connector of the drive and E1A, E2A, on the same board edge of the drive about midway down.

   E1 jumpered to E2 connects -Host Active to an internal port.

   E2 to E3 jumpers -Host Active to IO Channel Ready on the SH260.

   E1A jumpered selects - Slave Present.
   not jumpered selects single drive only.

   E2A jumpered addresses drive as drive C.
   not jumpered addresses drive as drive D.

OUTLINE DIMENSIONS

Outline Dimensions ± .010"	.75" × 4.00" × 5.15"
Weight	<1 pound

ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	5°C to 55°C
Non Operating	–40°C to 60°C
Thermal Gradient	20°C per hour maximum
Humidity	
Operating	8% to 80% non condensing
Non Operating	8% to 80% non condensing
Maximum Wet Bulb	26°C
Altitude (relative to sea level)	
Operating	–200 to 10,000 feet
Non-operating (maximum)	40,000 feet

RELIABILITY AND MAINTENANCE

MTBF	20,000 hours (POH)**
MTTR	10 minutes typical
Preventative Maintenance	None
Component Design Life	5 years
Data Reliability	<1 non recoverable error in 10^{12} bits read

**population is minimum of 100 units

SHOCK AND VIBRATION

Shock (1/2 sine pulse)
Vibration (swept sine, 1 octave per minute)
(Measured without shock isolation)

Non operating shock	75G's 11 ms (without non recoverable errors)
Non operating vibration	
5-62 HZ	.020" double amplitude
63-500 HZ	4 G's 0-peak
Operating shock	5 G's, 11 ms (without non recoverable errors)
Operating vibration	
5-27 HZ	.010" double amplitude
28-500 HZ	.5 G's 0-peak (without non recoverable errors)

MAGNETIC FIELD

The externally induced magnetic flux density may not exceed 6 gauss as measured at the disk surface.

ACOUSTIC NOISE

40 dBA max. at 1 meter

PIN DESCRIPTIONS

The following table describes all of the pins on the Task File Interface.

PIN	SIGNAL	PIN	SIGNAL
01	–HOST RESET	02	GND
03	+HOST DATA 7	04	+HOST DATA 8
05	+HOST DATA 6	06	+HOST DATA 9
07	+HOST DATA 5	08	+HOST DATA 10
09	+HOST DATA 4	10	+HOST DATA 11
11	+HOST DATA 3	12	+HOST DATA 12
13	+HOST DATA 2	14	+HOST DATA 13
15	+HOST DATA 1	16	+HOST DATA 14
17	+HOST DATA 0	18	+HOST DATA 15
19	GND	20	KEY
21	RESERVED/AEN	22	GND
23	–HOST IOW	24	GND
25	–HOST IOR	26	GND
27	RESERVED/DAK	28	+HOST ALE
29	RESERVED/DRQ	30	GND
31	+HOST IRQ14	32	–HOST IO16
33	+HOST ADDR 1	34	–HOST PDIAG
35	+HOST ADDR 0	36	+HOST ADDR 2
37	–HOST CS0	38	–HOST CS1
39	–HOST SLV/ACT	40	GND
41	+5V LOGIC	42	+5V MOTOR (unregulated)
43	GND	44	–XT/AT

SIGNAL NAME	DIR	PIN	DESCRIPTION
+HOST RESET	O	01	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND	O	0	2Ground between the drive and the Host.
+HOST DATA 0-15	I/O	03-181	6 bit bi-directional data bus between the host and the drive. The lower 8 bits, HD0-HD7, are used for register & ECC access. All 16 bits are used for data transfers. These are tri-state line with 24 mA drive capability. For XT, only bits 0-7 are used.
GND	O	19	Ground between the drive and the Host.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
RESERVED	O	21	AEN Used to Qualify DMA transfers on XT.
GND	O	22	Ground between the drive and the host.
–HOST IOW	O	23	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a register or the data register of the drive.
GND	O	24	Ground between the drive and the host.
–HOST IOR	O	25	Read strobe, which when low enables data from a register or the data register of the drive onto the host data bus, HD0 through HD15. The rising edge of –HOST IOR latches data from the drive at the host.
GND	O	26	Ground between the drive and the host.
RESERVED/DAK	O	27	–DAK DMA Acknowledge. Used for DMA transfers on XT.
+HOST ALE	O	28	Host Address Latch Enable. A signal used to quality the address lines. This signal is presently not used by the drive.
RESERVED/DRQ	O	29	–DRQ DMA Request. Used for DMA transfers on XT.
GND	O	30	Ground between the drive and the host.
+HOST IRQ14	I	31	Interrupt to the Host system, enabled only when the drive is selected, and the host activates the –IEN bit in the Digital Output register. When the –IEN bit is inactive, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. This signal is a tri-state line with 8 ma drive capacity.
–HOST IO16	I	32	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 24 mA drive capacity.
–HOST PDIAG	I	34	Passed diagnostic. Output by the drive if it is strapped in the slave mode. Input to the drive if it is strapped in the master mode. This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is a tri state line with 10 mA drive capability.
+HOST A0, A1, A2	O	35, 33, 36	Bit binary coded address used to select the individual registers in the task file.
–HOST CS0	O	37	Chip select decoded from the host address bus. Used to select some of the Host accessible registers.
–HOST CS1	O	38	Chip select decoded from the Host address bus. Used to select three of the registers in the Task File.
–HOST SLV/ACT	I	39	Signal from the drive used either to drive an active LED whenever the disk is being accessed or as an indication of a second drive present. When –ACTIVE, this signal is active low when the drive is busy and has a drive capability of 20 ma. When –SLAVE PRESENT, it is an indication of the presence of a second drive when low. In this state, it has a drive capability of 10 mA open drain.
GND	O	40	Ground between the drive and the host.
+5V LOGIC	I	41	+5V ±10% regulated DC power
+5V MOTOR	I	42	+5V ±10% DC power (unregulated)
GND	I	43	GND Return
–XT/AT	I	44	Selectable for XT or AT compatible interface.

CHAPTER 7. Floppy disk drive

7-1. SPECIFICATIONS

Items		2M BYTE MODE	1M BYTE MODE	
Recording Capacity	Unformatted	2 Mbytes	1 Mbytes	
	Formatted (Note 1)	1474.6 Kbytes	737.3 Kbytes	
	Per track	12.5 Kbytes	6.25 Kbytes	
Data transfer rate		500 Kbits/sec	250 Kbits/sec	
Recording capacity switching system		Media automatic recognition		
Access time	Track to track	3 msec		
	Seek settling time	15 msec max.		
	Average access time	94 msec		
Disk rotational speed		300 rpm		
Latency		100 msec		
Spindle motor start time (Note 2)		0.5 sec max.		
Recording density at innermost track		17434 bpi	8717 bpi	
Tracks	Track/Side	80 tracks		
	Track/Disk	160 tracks		
Track density		135 tpi		
Number of head		2		
Encoding method		MFM (Note 3)		
Environmental conditions	Conditions	Operating	Non-operating	Storage
	Temperature	5~45°C	−22~55°C	−40~62°C
	Humidity	20~80 %RH	10~90 %RH	5~90 %RH
	Max. wet bulb temp. (Note 4)	29°C	40°C	42°C
Vibration resistance (Note 5)		0.5 G	2 G	2 G
Shock resistance		5 G	60 G for 11 msec	
D.C. voltage requirements (Note 6)		+5V ±10% ripple: 100mVp-p		
Power consumption	Stand by	TYP: 20 mW		
	Operating	TYP: 1.0 W		
External view (*)except front panel		19.5 mm(H) × 101.6 mm(W) × 130.0 mm(D)		
Weight		Less than 270 g		
Panel and Button color		K-63681-30: GRAY 135 (Color No. 100Z-1X32343)		
		K-63681-32: 0A GRAY (Color No. 100Z-4X32154)		
		K-63681-33: NEUTRAL #8 (Color No. 100Z-1X33529)		
Activity LED		Green (Glowing in a drive selected status.)		
Write precompensation		2M mode: ±125 nsec.		
		1M mode: ±250 nsec.		
Acoustic stepping noise (Note 7)		Less than 45 dB(A)		
Media ejection		5 cm ~ without falling		
Reliability	MTBF	30,000 POH		
	MTTR	30 min.		
	Unit Life	5 years		
	Soft read errors	Less than 10^{-9} bits		
	Hard read errors	Less than 10^{-12} bits		
	Seek errors	Less than 10^{-6} seeks		
Security standards		Applying standards of UL, CSA and TÜV		

Note 1: Conformance to IBM, 18 sectors/track (512 bytes/sector): 2 M bytes mode
9 sectors/track (512 bytes/sector): 1 M bytes mode

Note 2: Spindle motor start time is a time period up to reaching the motor rotating speed of 300rpm±1.5% in a disk chucking state.

Note 3: FM system is possible to use. But recording capacity, recording density and data transfer rate become one-half of that of the MFM system.

Note 4: Condensation shall not result.

Note 5: Vibration of 5~500 Hz, except resonance point.

Note 6: The DC power cable used should satisfy the specification at the point of the DC power connector.

Note 7: Measuring condition
Hanging the drive above 1 m from the floor, and setting the measuring equipment 1 m away from the drive with 3 msec seek time.

7-2. INTERFACE

7-2-1. Signal Interface

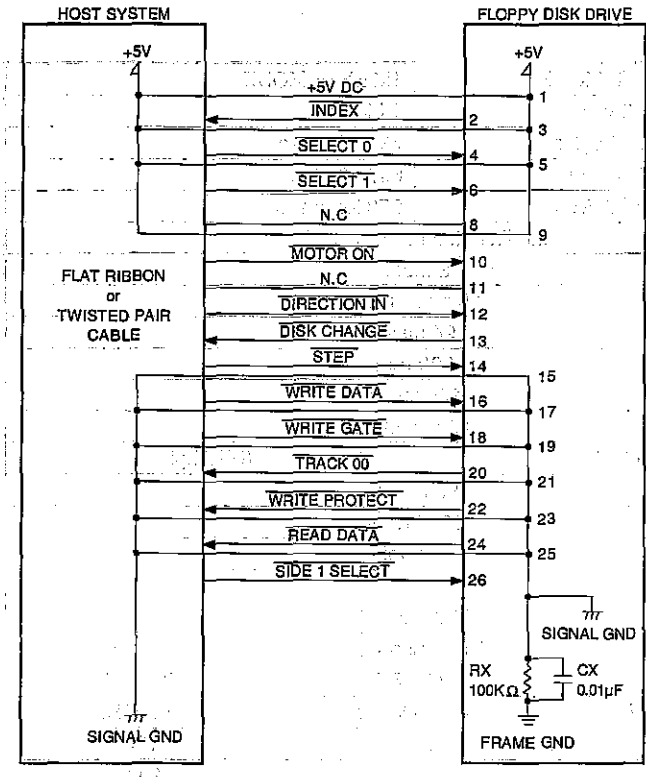


Fig. 7-1 Signal Interface

Pin No.	Signal name	Pin No.	Signal name
1	+5V DC	2	INDEX
3	+5V DC	4	SELECT 0
5	+5V DC	6	SELECT 1
—	—	8	N.C.
9	+5V DC	10	MOTOR ON
11	N.C.	12	DIRECTION IN
13	DISK CHANGE	14	STEP
15	GND	16	WRITE DATA
17	GND	18	WRITE GATE
19	GND	20	TRACK 00
21	GND	22	WRITE PROTECT
23	GND	24	READ DATA
25	GND	26	SIDE 1 SELECT

Connector pins arrangement

7-2-4. Input Signals

SELECT 0~1

Two separate input lines, SELECT 0 (S0) through SELECT 1 (S1) are provided and a specific input line is selected by jumper JJ1. For details, refer to paragraph 4-1 "Jumper function".
When setting this signal to a logical 0 level, the drive goes to active level.

MOTOR ON

This signal controls the spindle motor. When a disk cassette is inserted and this signal is set to a logical 0 level, the spindle motor will turn on.
When this signal is set to logical 1 level or a disk cassette is ejected, the spindle motor will turn off.

DIRECTION IN

This signal defines the direction of motion which the read/write heads will take, a logical 1 level defines the direction as "out", conversely a logical 0 level defines the direction as "in".

STEP

This signal is a control signal which causes the read/write heads to move in the direction of motion defined by the DIRECTION IN signal. The access motion is initiated on the trailing edge (positive going) of each signal pulse.

WRITE GATE

This signal control the write operation. Write operation are valid at a logical 0 level. This signal provides the function which causes tunnel erase operation inside the drive, so switching of SIDE SELECT signal or seek operation must be inhibited, refer to item 3-7 for Write Initiate Timing.

WRITE DATA

This signal provides the data to be written on a disk cassette.
Each transition from a logical 1 level to a logical 0 level will cause the current through the read/write head to reverse, thus causing a flux reversal to be written on a disk cassette. This signal is valid when the WRITE GATE signal is in a logical 0 level.

SIDE 1 SELECT

This signal is a control signal which selects one of the two read/write heads. A logical 0 level on this line selects the side 1 and a logical 1 level selects the side 0.
When switching timing from one head to another, refer to item 3-6 for read initiate timing, and item 3-7 for write initiate timing.

7-2-5. Output Signals

All output signals are issued only when the SELECT line is activated.

TRACK 00

This signal goes to a logical "0" level when the read/write head positioned at track 00 (outermost track) and goes to a logical 1 level when it is positioned at a track except track 00. The head is automatically moved to track 00 by power-on recalibrate function when DC voltage is applied to the drive.

INDEX(NOTE)

This signal is provided by each motor revolution. There is one negative pulse on this signal per revolution of disk. The leading edge (negative-going) of this signal shows the starting point of track.

READ DATA(NOTE)

This signal provides the "raw data" (clock and data together) as detected by the read circuit of the drive.

WRITE PROTECT

This signal informs system that write protected disk is inserted, and on this status, this signal goes to a logical 0 level.
The drive will inhibit writing with the protected disk installed.

DISK CHANGE

This signal informs system that disk cassette is exchanged.
Usually this signal remains a logical 1 level when disk cassette is inserted and goes to a logical 0 level when it is ejected from drive.
The DISK CHANGE signal returns to logical 1 level when disk cassette is inserted, the drive is selected, and a step pulse has been received.

(NOTE) Both of the INDEX and READ DATA signals are issued to drive ready state. Refer to the item 3-5 for Ready gate timing.

CHAPTER 8. SERVICE-MAN DIAGNOSTIC

8-1. Introduction

This diagnostics is used to check the operating state of the system unit, keyboard, and peripheral units, when an option device is interfaced to the PC-4700 or when there is a state of error.

The following four kinds of diagnostics are provided to trace the exact cause.

Individual device diagnostics

Used to test the real time clock, setup RAM, memory module, keyboard, speaker, monochrome adapter, color/graphics adapter, coprocessor printer, serial I/O, modem, and liquid crystal display.

When an error is found, the failure is reported with the error status.

Floppy disk diagnostics

This test program performs tests in more details than the test by the individual device diagnostic and may also be used to perform aging test of the floppy disk.

Hard disk diagnostics

This test program performs tests in more details than the test by the individual device diagnostic and may also be used to perform aging test of the hard disk.

The diagnostic program disk comes supplied on a 3.5" MD-DOS diskette with the above diagnostic programs and the program loader.

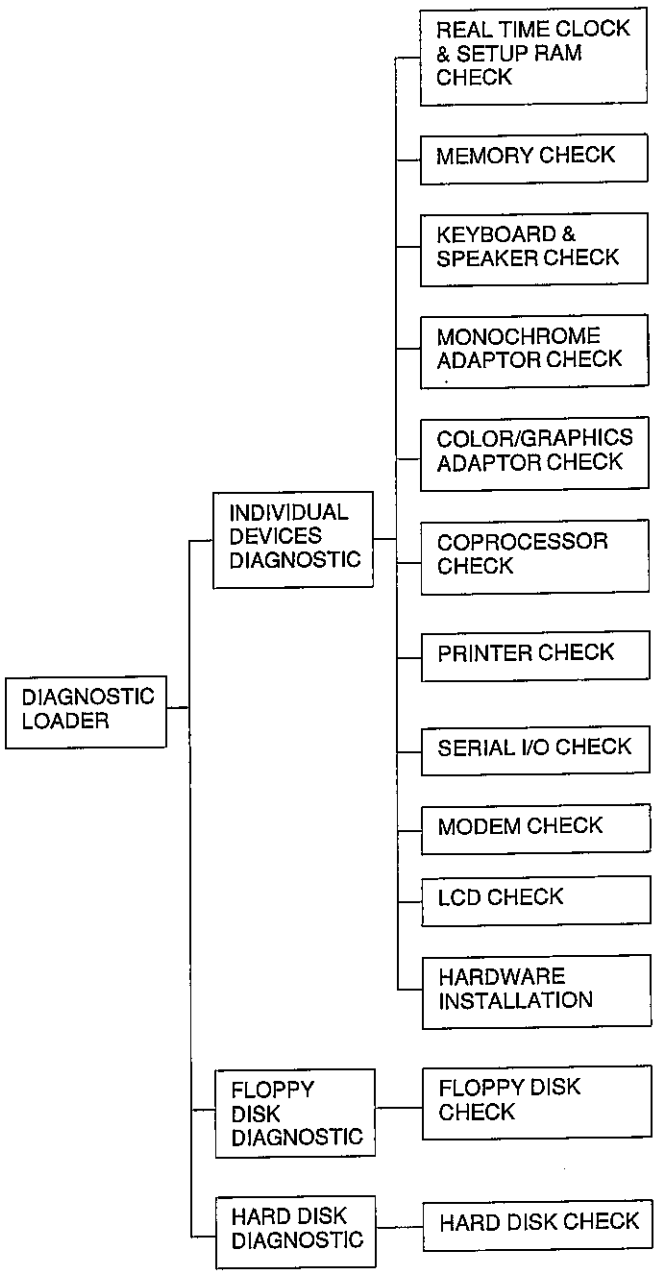
It has been designed to test almost any PC-4700 function and its peripherals.

8-2. Diagnostic program structure

The following figure shows the configuration of the programs stored on the diagnostic program diskette.

Any of three diagnostics can be chosen by typing the number indicated by the diagnostic program.

When an individual device diagnostic is chosen, a sub-menu is displayed to make choice in the same manner.



8-3. Starting up the diagnostic program

The following procedure is required to start the diagnostic program.

1. Insert the diagnostic program disk in the drive A and turn power on to the PC-4700.
2. When the MS-DOS prompt appears, type the command shown below and press the ENTER key.

```
A> DIAG47S [ENTER]
```

3. The diagnostic program menu shown below will appear within a few seconds.

Type a number to choose the program.

```
DIAGNOSTIC PROGRAM MENU
  1. Individual Devices Diagnostic
  2. Floppy Disk Diagnostic
  3. Hard Disk Diagnostic
Enter your selected number:_
```

Diagnostic Program Menu

8-4. Diagnostic program loader

This diagnostic program loader is used to select and execute the individual device diagnostic program, floppy disk diagnostic program and hard disk diagnostic program.

Upon the start of the program loader, the diagnostic program menu is displayed. When one of four choice is typed, the respective diagnostic program is loaded from the floppy disk onto the main memory area. After it has been completed, the control moves to the diagnostic program to execute.

When the ESC key is pushed in the diagnostic program menu, the program terminates and the control returns to the MS-DOS.

8-5. Check program

All check programs are stored on the diagnostic program disk and used to check the state of a device after it has been installed or a specific device is tested when an error is reported.

8-5-1. Individual devices diagnostics

The desired check item must be chosen and typed in the menu followed by the depression of the ENTER key.

To cancel the choice, simply push the ESC key. The control will return to the diagnostic loader.

When changing the setting contents with the set-up menu during each device check, return fromt he device check menu to this individual devices diagnostic menu in advance.

```
Individual Devices Diagnostic V-X.XX
  1 --- Real Time Clock & Setup RAM
  2 --- Memory
  3 --- Keyboard & Speaker
  4 --- Monochrome Adaptor
  5 --- Color/Graphics Adaptor
  6 --- Coprocessor
  7 --- Printer
  8 --- Serial I/O Adaptor
  9 --- Modem Adaptor
 10 --- Liquid Crystal Display
  0 --- Hardware Installation
Enter your selected number: _
```

Individual Devices Diagnostic Menu

• Outline of each device check

* Real time clock & setup RAM
  Tests the real time clock and the setup RAM in the read/write mode.
* Memory
  Tests the main memory, video memory and EMS memory in the read/write mode.
* Keyboard & speaker
  Tests the keyboard and the speaker.
* Monochrome Adapter
  Tests the LCD and CRT functions in the monochrome mode.
* Color/graphics adapter
  Tests the LCD and CRT functions in the color/graphics mode.
* Coprocessor
  Tests the coprocessor by carring out initialize and arithmetic operation.
* Printer
  Tests the printer.
* Serial I/O adapter
  Tests the RS-232C functions using the loopback connector.
* Modem adapter
  Tests the modem functions in the loopback mode.
* Liquid crystal display
  Tests the LCD by means of the display pattern.
* Hardware installation
  Displays the device names interfaced to the PC-4600.

• Setting parameter option

After the real time clock & setup RAM or memory was selected, the program prompts for entry of a parameter option shown below before starting the test.

```
Error stop? (Y/N) (default response is Y)
Loop counter (1-9999) (default response is 1)
```

If the ENTER key was depressed instead of Y, N or a number, the default will be chosen.

After completing the parameter entry, the program starts.

The following is reported in a course of the real time clock & setup RAM or memory check.

```
Success -- xx
Failure -- yy
```

where, xx represents the number of times the program passed successfully, and yy represents how many times the test failed, when any continuous test was specified in the initial setup.

If the ESC key is depressed when the test is being performed, the program execution terminates.

8-5-1-1. Real Time Clock & Setup RAM Check

This program tests the real-time clock and the setup RAM within the sub-CPU.

When this test item is chosen, the sub-menu shown below appears. The desired test item must be chosen by typing the number in the menu. If 0 is typed, the control returns to the individual devices diagnostic menu.

```
Real Time Clock & Setup RAM Check
   1 --- Real time clock check
   2 --- Setup RAM check
   0 --- Exit
Enter your selected number: _
```

Real Time Clock & Setup RAM Check Menu

After a test item was chosen, the control comes asking for a parameter option entry before going into the test. And the test will start after this. If no error was encountered, test repetitions are continued to count.

Depression of the ESC key terminates the test.

When an error was encountered, the error message is produced.

• Real time clock check

This test item tests the real time clock within the sub-CPU for a period of one second while communicating with the sub-CPU by means of the V40 timer interrupt (18.2Hz).

• Setup RAM check

Except for the RAM area within the sub-CPU where the date and time are stored, this test program communicates with the sub-CPU and tests the setup RAM area in the read/write mode in the following manner:

1. Data "5" is written in the setup RAM check area.
2. This data "5" stored in the setup RAM is read one digit at a time, then the data "A" is written in every area until the entire area is written with "A".
3. This test data "A" is read one digit at a time, then the data "5" is written in every area until the entire area is written with "5".

The contents of the setup RAM are saved prior to initiation of the test and restored after completion of the test.

• Error message

* REAL TIME CLOCK ERROR
  The real time clock in the sub-CPU or the V-40 timer is not working properly.
* SETUP RAM READ/WRITE ERROR
  The test data written in the setup RAM within the sub-CPU does not coincide with the data written.
* INTERPROCESSOR COMMUNICATION ERROR
  Communication is not done properly with the sub-CPU.
* SETUP RAM BROKEN ERROR
  The contents of the setup RAM are destroyed as a result of a communication failure with the sub-CPU during the test of the setup RAM.

8-5-2. Memory Check

This program tests the main memory and the video memory on the main board and the EMS memory on the EMS memory card. (CE-471B)

The following menu appears when this test program is selected.

One of three test items must be chosen after typing the desired number.

Typing 0 will cause the control to return to the individual devices diagnostic menu.

```
Memory Check
   1 --- Main memory check
   2 --- Video memory check
   3 --- EMS memory check
   0 --- Exit
Enter your selected number: _
```

Memory Check Menu

After a test item was chosen, the control comes asking for a parameter option entry before going into the test, as discussed in Paragraph 5-1.

And the test will start after this.

If no error was encountered, test repetitions are continued to count.

Depression of the ESC key terminates the test.

When an error was encountered, the error message is produced.

• Main memory check

This program tests for 640KB of the main memory.

1. The main memory area after the address 30000H is read/write tested using the marching test mode in an increment of 64KB.
2. If not error was encountered after checking the area after the address 20000H, the data in the address 00000H through 2FFFFH are copied onto the area after the address 30000H, then the address 00000H through 2FFFFH is tested in the marching test mode in an increment of 64KB.

• Video memory

This program tests for 128KB of the video memory.

The video memory area is read/write tested using the marching test for four video DRAM bank (32KB).

Note that care was taken by the program not to destruct the video memory contents.

• EMS memory check

This program test for 1MB of the EMS memory.

The EMS memory area is read/write tested using the marching test for 64 page frame (16KB).

Note that care was taken by the program to destruct the EMS memory contents.

NOTE: The marching test for the main memory check and the video memory check is carried out in the following manner:
1. Test data 5555H are written in the area to be checked.
2. The test data are read at every word and the test data AAAAH are written. This is done for all the areas.
3. The data AAAAH are read at every word and the test data 5555H are written. This is done for all the areas.
4. The entire area to be tested is written with 0000H.
5. The data 0000H are read at every word and the test data FFFFH are written. This is done for all the areas.
6. The data FFFFH are read at every word and the test data 0000H are written. This is done for all the areas.

• Error message

* 640KB MAIN MEMORY R/W ERROR – address: X000H, data: yyyyH During test of 640KB main memory area, the test data stored in the segment address X000H did not coincide with read data in a yyyyH bit pattern.
* 128KB VIDEO MEMORY R/W ERROR – bank: x, data: yyyyH During test of 128KB video memory area, the test data stored in the bank X did not coincide with read data in a yyyyH bit pattern.
* 1MB EMS MEMORY R/W ERROR – address: 1XX000H, data: YYYYH During test of 1MB EMS memory area, the test data stored in the address from 1XX000H to 1XXFFFH did not coincide with read data in a YYYYH bit pattern.

8-5-3. Keyboard & Speaker Check

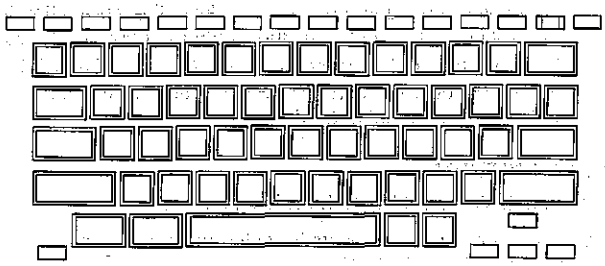
This program test the keyboard and speaker functions. When this test program is chosen, the sub-menu shown below appears. You may choose the desired test item by typing the respective number. Depression of 0 causes the control to return to the individual devices diagnostic menu.

```
Keyboard & Speaker Check
  1 --- US English keyboard check
  2 --- Other keyboards check
  0 --- Exit
Enter selected number: _
```

Keyboard & Speaker Check Menu

• Keyboard check

When this test starts, the keyboard layout appears. Depressing any key makes it emphasized with all toned to indicate that the key has been pressed. Right and left Ctrl key is marked at the same time. Fn key is marked by pressing with cusor key. The test terminates when ESC key is pressed twice consecutively and control return to the keyboard & speaker check manu.



US English keyboard layout screen

The speaker can be tested using the function keys F1 through F10. The F1 key issues the lowest beeping tone and the F10 key the highest tone, while F2 through F9 issues the tone incremental.

8-5-4. Monochrome Adapter Check

This program tests the internal LCD controller, LCD unit, color/monochrome CRT adapter option (CE-471A) and the monochrome CRT interfaced to it.

The following is prompted if the system console was not set up to the MDA when this test program is chosen.

```
Set Display Mode to Monochrome and Console to MDA.
```

In this case, set the display (LCD) or CRT adapter display mode to monochrome with the set-up menu and the system console needs to be updated to MDA with the individual devices diagnostic menu displayed. If the system console has already been set to MDA, the following sub-menu appears. You can now choose the desired item number 1 to 5.

When 0 is chosen, the control returns to the individual devices diagnostic menu.

```
Monochrome Adaptor Check
  1 --- Monochrome display buffer check
  2 --- Attribute check
  3 --- Character set check
  4 --- B/W mode check
  5 --- Run all above checks
  0 --- Exit
Enter your selected number: _
```

Monochrome Adaptor Check Menu

• Monochrome display buffer check

The program tests the video RAM (VRAM) in the monochrome display adapter by writing and reading the test data in the VRAM.

• Attribute check

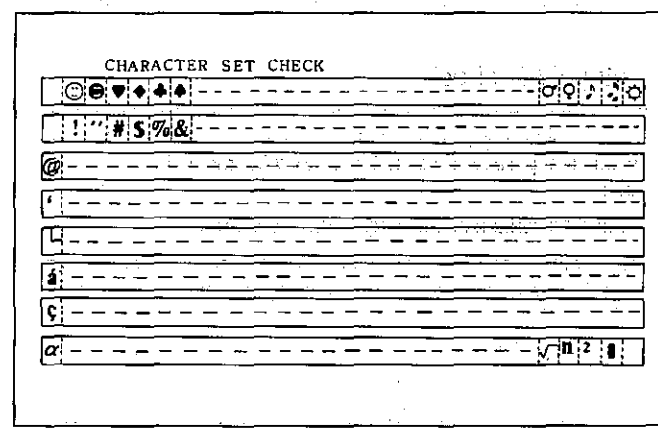
All the attributes of the monochrome display adapter are tested which includes the normal, intensity, reverse video, blinking and underlined characters. Now you can visually check the information appeared in the screen, referring to the following:

```
ATTRIBUTE CHECK
    NORMAL
    INTENSITY
    REVERSE
    BLINK
    UNDERLINE
```

Attribute Check Display

• Character set check

All fonts contained in the character generator are displayed. In the first place, characters of the normal attribute are displayed. When any key is depressed next, characters with intensity attribute are displayed. Now, you can visually check the information appeared in the screen, referring to the following:



Character Set Check Display

* See the Character Format on the upper right of this page.

• B/W mode check

A black and white screen is displayed. Now, you can visually check it while adjusting the LCD or CRT monitor.

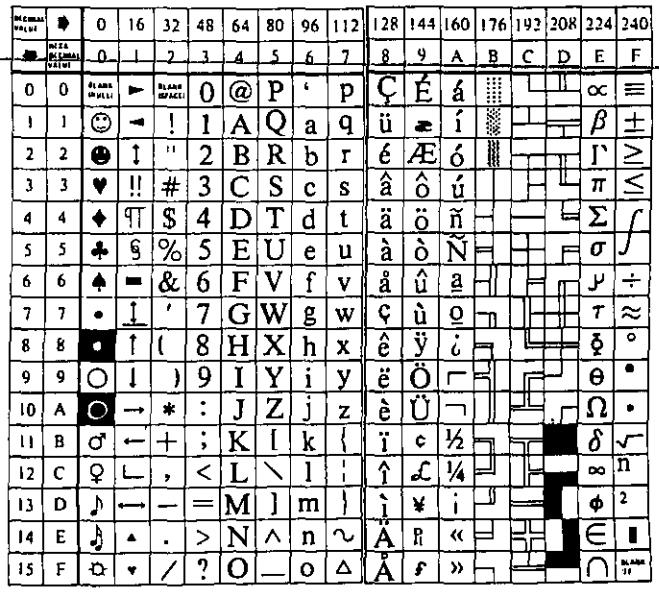
• Run all above checks

You can check items 1 through 4.

• Error message

* VRAM ERROR - data xxH

The test data written in the monochrome display buffer did not coincide with the data read in a bit pattern of xxH (where, the bit 1 is in xxH is an unmatch).



8-5-5. Color Graphics Adapter Check

This program is used to test the internal LCD controller, LD display unit, color/monochrome CRT adapter (CE-471A) and the color CRT monitor interfaced to it.

If the system console was not set up to CGA when this program is chosen, the following message is displayed.

```
Set Display Mode to Color/Graphics and Console to CGA.
```

In this event, the choice must be revised through the setup menu to change the display (LCD) or CRT adapter display mode to graphics and color and the system console to CGA with the individual devices diagnostic menu displayed. The following sub-menu appears if the system console has been set to CGA. You may now choose the item by typing the item number 1 to 9. Depression of 0 causes the control to return to the individual devices diagnostics menu.

```
Color/Graphics Adapter Check
   1 --- Color/graphics display buffer check
   2 --- Attribute check
   3 --- 80 x 25 alphanumeric mode check
   4 --- 40 x 25 alphanumeric mode check
   5 --- 320 x 200 graphics mode check
   6 --- 640 x 200 graphics mode check
   7 --- Screen paging check
   8 --- Color CRT check
   9 --- Run all above checks
   0 --- Exit
Enter your selected number: _
```

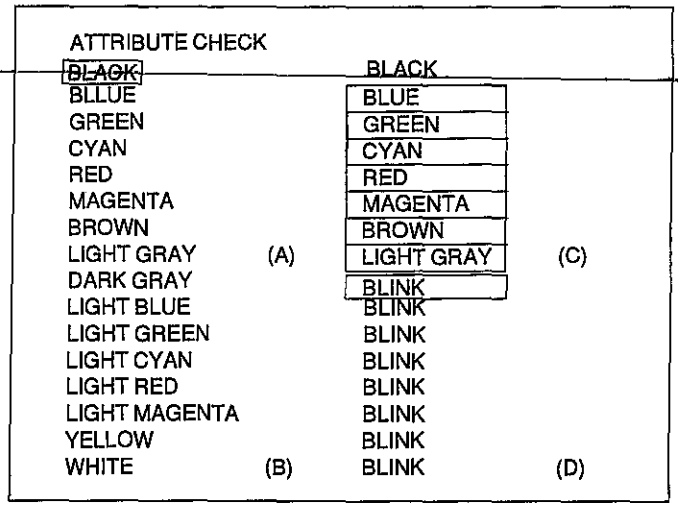
Color/Graphics Adapter Check Menu

• Color/graphics display buffer check

The program checks the viode-RAM (VRAM) on the color/graphics display adapter, writing certain data into the VRAM and reading it back.

• Attribute check

All the attributes modes of the color/graphics display adapter are checked. They are all the intensity, blinking, reverse video, and foreground/background color. Visually check the information displayed on the screen referring to the following.



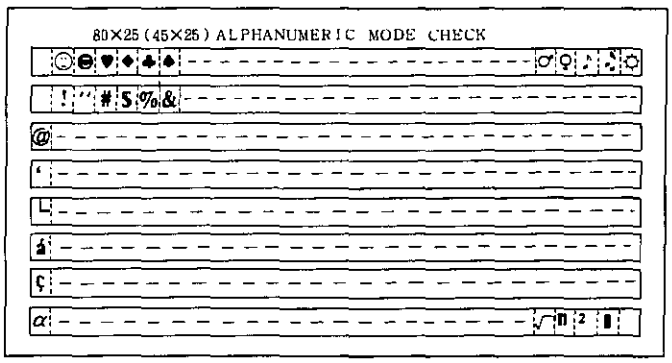
Attribute Check Display

When the color monitor is used, the portions (A) and (B) show the color of display characters and the portion (C) the color of background.

Because it is not possible to display color with the LCD, the portion (A) is displayed by the normal characters (except black which is displayed in reverse video) and the portion (B) is displayed in highlight. The portion (D) is displayed blinking for both the color monitor and the LCD.

• 80 x 25 alphanumeric mode check

All characters are displayed in the 80 x 25, alphanumeric mode. First, the characters of normal attribute are displayed. As any key is depressed next, the characters with the intensity attribute are displayed. Visually check the characters displayed on the screen, referring to the following.



80 x 25 (40 x 25) Alphanumeric Mode Check Display

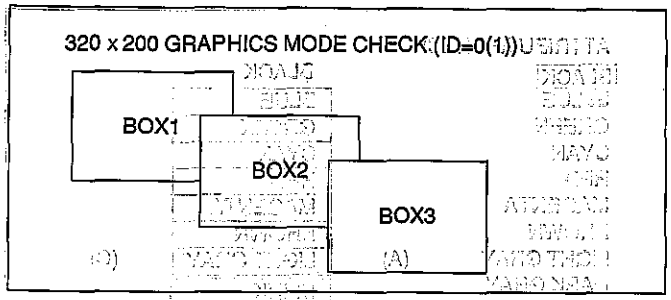
* See the character format on the upper right of page 5.

• 40 x 25 alphanumeric mode check

All characters are displayed in the 40 x 25 alphanumeric mode. First, the characters of normal attribute are displayed. As any key is depressed next, the characters with the intensity attribute are displayed. Visually check the characters displayed on the screen, referring to the above.

• 320 x 200 graphics mode check

Three dialog boxes come displayed in the 320 x 200 graphics mode. First, the color set-1 (ID=0) is displayed in the dialog box. Any key depression displays the color set-2 (ID=1) in the dialog box. Visually check the dialog boxes displayed on the screen, referring to the following.



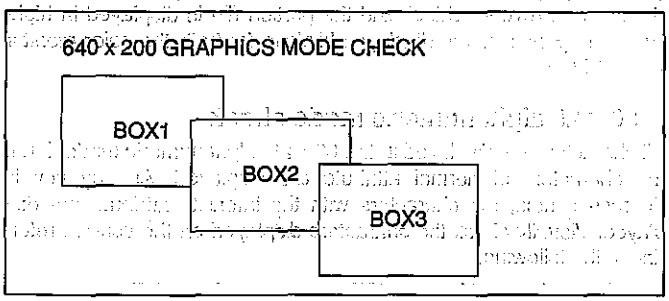
320 x 200 Graphics Mode Check Display

The following applies to the color monitor and LCD display.

	ID = 0 (Color Set 1)				ID = 1 (Color Set 2)			
	BOX1	BOX2	BOX3	Back-ground	BOX1	BOX2	BOX3	Back-ground
Color CRT monitor	Green	Red	Brown	Blue	Cyan	Magenta	White	Red
LCD	Vertical stripes	Vertical stripes	All toned	Null	Vertical stripes	Vertical stripes	All toned	Null

• 640 x 200 graphics mode check

Three dialog boxes are displayed in the 640 x 200, graphics mode. Visually check the boxes displayed on the screen, referring to the following.



640 x 200 Graphics Mode Check Display

The following is displayed for the color monitor and the LCD.

	BOX1	BOX2	BOX3	Background
Color CRT monitor	Horizontal stripes (B/W)	Lightly all toned (B/W)	Darkly all toned (B/W)	Null
LCD	Horizontal stripes	Vertical stripes	All toned	Null

• Screen paging check

The memory in the VRAM can be divided into eight different areas in 40 x 25 alphanumeric mode by the program. These areas are called display pages. Any key depression displays eight display pages numbered from 0 to 7 sequentially. Visually check the display pages on the screen.

• Color CRT check

Sixteen different color screens are displayed sequentially. They are:

1. Black
2. Blue
3. Green
4. Cyan
5. Red
6. Magenta
7. Brown
8. Light gray
9. Dark gray
10. Light blue
11. Light green
12. Light cyan
13. Light red
14. Light magenta
15. Yellow
16. White

Press any key to display the next color screen. Visually check to see if the actually displayed color is correct.

• Run all above checks

Checks all the items from 1 to 9 in sequence.

• Error message

* VRAM ERROR - data xxH

Data written in the color/graphics display buffer do not coincide with the data read in a bit pattern of xxH (where, the bit 1 in xxH is an unmatch).

8-5-6. Coprocessor check

This program tests the co-processor by carring out initialize and arithmetic operation.

When this test item is chosen, the sub-menu shown below appears. The desired test item must be chosen by typing the number in the menu. If 0 is typed, the control returns to the individual devices diagnostic menu.

```
Coprocessor Check
  1 --- Initialize check
  2 --- Arithmetic check
  0 --- Exit
Enter your selected number:_
```

After a test item was chosen, the control comes asking for a parameter option entry before going into the test. And the test will start after this. If no error was encountered, test repetitions are continued to count.

Depression of the ESC key terminates the test.

When an error was encountered, the error message is produced.

• Initialize check

This test item tests the initialize function by issuing the initialize command.

• Arithmetic check

This test item tests the arithmetic function by issuing the arithmetic command.

8-5-7. Printer check

This program tests the printer interface and the printer connected with it.

The following sub-menu is displayed when this test program is selected.

Type the desired test item.

Depression of 0 causes the control to return to the individual device diagnostic menu.

```
Printer Check
  1 --- Printer status check
  2 --- Character set check
  0 --- Exit
Enter your selected number: -
```

Printer Check Menu

• Printer status check

With this test program the printer status is read and displayed as in the figure shown below. If all status are asterisk attached, the test has been normally completed. In this case, it shows that it is ready to printer. The item "Sel" may not change when the CE-700P is in connection.

```
PRINTER STATUS CHECK
Bsy Ack Pe Sel Ioe --- --- Toe
 *   *   *   *   *   *   *   *
```

The signal is OK if the symbol * is displayed.

• Character set check

With this test program code 20H thru 7FH and A0H thru FFH are printed to check with.

Before running the test, the prompt below will appear:

```
Are you ready ? (Y/N)_
```

Enter Y if preparations for this printer are completed.

The result on the paper looks similar to the example shown in the following.

```
 !"#$%&' () *+,-./
0123456789:;<=>?
@ABCDEFGHIJKLMNO
PQRSTUVWXYZ[\] ^_
`abcdefghijklmno
pqrstuvwxyz{|} ~
```

Printout on Paper

* In the case of printed out by CE700P.

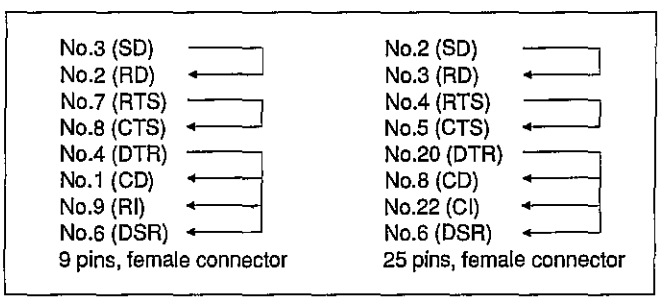
• Error message

* PRINTER NOT AVAILABLE
  Displayed when the printer adapter is in trouble.
* PRINTER STATUS ERROR
  Appears if the printer is not connected, not turned on, or not in the on-line state. At the same time, the printer status at the error is displayed.

8-5-8. Serial I/O Check

This program tests the RS-232C line of the standard serial I/O and the internal serial I/O (CE-451B, CE-451M, CE-462M) with the loop-back connector in use.

The following shows how wires are connected.



Oraganization of Loopback Connector

If the serial port adapter (RS-232C or modem) was not istalled when this test program is chosen, the following message is produced.

```
Serial Port Adapter is not installed.
```

The following is displayed if the mode is not in the SIO mode, even if the modem card (CE-451M, CE-462M) is installed.

```
Set Communication Mode to SIO.
```

In this event, the mode must be set to SIO through the setup menu with the individual devices diagnostic menu displayed.

The sub-menu shown next will appear if the serial I/O adapter (RS-232C) is installed.

Type the desired test item.

Depression of 0 causes the control to return to the individual devices diagnostic menu.

```
Serial I/O Check
  1 --- Parameters check
  2 --- Character transport check
  0 --- Exit
Enter your selected number: _
```

Serial I/O Check Menu

• Parameters check

This program tests the parameters such as the baud rate, parity check, stop bit, and word length.

If the internal serial I/O is connected, the following message appears:

```
  1 --- Standard serial I/O
  2 --- Internal serial I/O
  0 --- Exit
Enter your selected number: _
```

Select a serial I/O which is to be tested.

Parameters are checked automatically in the following order.

1. Checks the baud rate, 110 to 9600 baud, with the parity check set to none, stop bit to 1, and word length to 8 bits.
2. Checks the word length 7 bits and 8 bits with the parity check set to none and the stop bit to 1. Next, the same check is done with the stop bits at two (fixed to the 9600 baud).
3. Checks the word length 7 bits and 8 bits with the parity check set to odd and the stop bit to 1. Next, the same check is done with the stop bits at two (fixed to the 9600 baud).
4. Checks the word length 7 bits and 8 bits with the parity check set to even and the stop bit to 1. Next, the same check is done with the stop bits at two (fixed to the 9600 baud).

NOTE: Test data 0 to 7FH is used for the word length 7 bits and 0 to FFH for the word length 8 bits.

• Character transport check

This program tests the character data entered on the keyboard are sent and received via the loopback connector and the received data are displayed on the screen.

If the serial I/O is connected, the following message appears:

```
  1 --- Standard serial I/O
  2 --- Internal serial I/O
  0 --- Exit
Enter your selected number:_
```

Select a serial I/O which is to be tested.

Communication parameter must be entered first in the setup menu.

As entry of characters to be transmitted will be prompted after the program started, you may enter 60 strokes of any character at a maximum. Depression of the ENTER key starts the test and transmission takes place according to the parameter programmed in the setup menu. The received data are displayed.

The test terminates when the ESC key is depressed and the control returns to the serial I/O check menu.

• Error message

* COMMUNICATION MODE ERROR
SIO test is made with the modem card (CE-451M) communication mode set to Modem mode.

* COM1 (or 2): BAUD RATE = xxx0bps - <Error kind>
During COM1 (or 2) baud rate parameter check, the error displayed in <Error kind> occurs.

* COM1 (or 2): PARITY, STOP BIT, WORD LENGTH = x, y, z - <Error kind>
During COM1 (or 2) parameter check, when parity, stop bit, and word length are respectively x (= none, odd, or even), y (= 0 or 1), z (= 7 or 8), the error displayed in <Error kind> occurs.

* COM1 (or 2): CHARACTER TRANSPORT - <Error kind>
During COM1 (or 2) character transport check, the error displayed in <Error kind> occurs.

<Error kind>

- SD TIMEOUT
Response to the transmit data is not found within the prescribed time.
- RD TIMEOUT
Response to the receive data is not found within the prescribed time.
- TRANS REG NOT EMPTY
The transmitter shift register failed to go empty.
- OVERRUN ERROR
Character is received when the receive buffer is fully occupied with characters.
- FRAMING ERROR
0 is found for the stop bit.
- PARITY ERROR
A parity error is met.
- DATA COMPARE ERROR
Received data did not match with the transmit data.

8-5-9. Modem Check

With this test program the modem (CE-451M, CE-462M) is tested after setting the modem interface to the loopback test mode.

If the serial port adapter (RC-232C or modem) was not installed when this program is chosen, the following message is displayed.

```
Serial Port Adapter is not installed.
```

If the serial I/O card (CE-451B) was installed, the following message is displayed.

```
Modem Adapter is not installed.
```

If the mode is not for the modem even though the modem card (CE-451M, CE-462M) was installed, the following message is displayed.

```
Set Communication Mode to Modem.
```

In this event, the mode must be set to the modem at the setup menu with the individual devices diagnostic menu displayed.

The following sub-menu is displayed when the modem adapter is installed. Depression of 1 starts to test the modem. Depression of 0 causes the control to return to the individual devices diagnostic menu.

```
Modem Check
   1 --- Loop back check
   0 --- Exit
Enter your selected number:_
```

Modem Check Menu

• Loopback check

This program is used to test the modem by sending and receiving the data with the modem interface set in the loopback test mode.

First, the communication parameter must be set at the setup menu.

The modem is tested in the following order after the test is started.

1. The modem interface is set in the loopback test mode.
2. Using the parameter chosen in the setup menu, the test data 0 thru 7FH are sent and received to verify.
3. The control returns to the command mode to be ready for the initial setup.

• Error message

- COMMUNICATION MODE ERROR
Modem test is made with the modem card (CE-451M) communication mode set to Modem mode.
- COM1 (or 2): LOOP BACK - <Error kind>

<Error kind>

- SD TIMEOUT
Response to the transmit data is not found within the prescribed time.
- RD TIMEOUT
Response to the receive data is not found within the prescribed time.
- TRANS REG NOT EMPTY
The transmitter shift register failed to go empty.
- OVERRUN ERROR
Character is received when the receive buffer is fully occupied with characters.
- FRAMING ERROR
0 is found for the stop bit.
- PARITY ERROR
A parity error is met.
- DATA COMPARE ERROR
Received data did not match with the transmit data.

8-5-10. Liquid Crystal Display Check

This program tests the LC display function by displaying the LCD test pattern on the screen. If the display mode and the system console are not set up to CGA, the following message is displayed.

```
Set Display Mode to Graphics and Console to CGA.
```

In this event, set the display mode to graphics and the system console to CGA at the setup menu with the individual devices diagnostic menu displayed. If the display mode has been set to graphics and the system console to CGA, the following sub-menu is displayed.

Choose and type the desired item number.

Depression of 0 causes the control to return to the individual devices diagnostic menu.

```
Liquid Crystal Display Check
   1 --- Check pattern
   2 --- Line move
   3 --- Stripe
   0 --- Exit
Enter your selected number: _
```

Liquid Crystal Display Check Menu

• Check pattern

This program displays the check pattern on the display.

First, all display dots are displayed. Next, the test patterns of single dot, two dots, four dots, and eight dots intervals are displayed and their reverse videos. The above procedure is repeated again.

Visually check the pattern displayed on the screen.

When the SPACE bar is pushed in a middle of the test, the test execution suspends. With the depression of the SPACE bar again, the test resumes. The test terminates by the depression of the ESC key and the control returns to the liquid crystal display check menu.

• Stripe

With this test program stripe is displayed vertical and horizontal stripes are displayed including reverse video (four patterns).

Visually check the pattern displayed on the screen.

When the SPACE bar is pushed in a middle of the test, the test execution suspends. With the depression of the SPACE bar again, the test resumes. The test terminates by the depression of the ESC key and the control returns to the liquid crystal display check menu.

8-5-11. Hardware Installation

With this program the devices connected to the PC-4700 are checked for installation.

When this item is selected, all the installed devices appear on the screen.

The following are the names of possible devices:

```
Hardware installation
System Board
Real Time Clock & Setup RAM
Main Memory (indicated by kilobytes)
Keyboard
Liquid Crystal Display
Monochrome CRT Adapter
Color/Graphics CRT Adapter
1 or 2 Floppy Disk Drive(s), Adapter
Printer Adapter
Serial I/O Card
Modem Card
Co-processor
Hard Disk Drive, Adapter
EMS Card
```

Hardware Installation Display

8-5-12. Floppy disk drive diagnostics

This program tests the internal 3-1/2" floppy disk drive and the external 5-1/4" floppy disk drive.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

```
Floppy Disk Drive Diagnostics
Read drive status
Write, read & compare check
Read only check
00 track sensor adjustment
Target sector read check
Error table display
```

8-5-12-1. Read drive status

This item displays the current status of the floppy disk drive(s). While this program is executing, the system periodically detect some status change, it causes the buzzer to sound and displays the new status on the screen.

- **Operation**

Pressing any key, the test terminates.

8-5-12-2. Write, read & compare check

This test checks the write/read operation.

The system writes the specified data to the floppy disk, reads the same data from the floppy disk, and then compares them.
The specified data to be written is 00H to FFH increment pattern when the pass count is 0, otherwise the data is 2bytes repetitive pattern of "B6DBH".

- **Caution**

When this test is executed, all the contents stored in the floppy disk are destroyed. So be very careful with this test. In addition, it is necessary to release "Write Protect".

- **Operation**

When this test is selected, the following message is displayed.

```
Please insert the formatted scratch disk in the drive.
```

At the time, insert the test disk in the drive to be checked and press ENTER. If the drive is not ready or the test disk isn't inserted in the drive, the following message is displayed and the test terminates.

```
Drive not ready.
```

Specify whether to check the drive or not in the following message.

```
Drive_A (1.44MB) test ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. The string in the parenthesis represents the capacity of the disk.
Specify the range of cylinders to be checked in the following message.

```
Cylinder range ?
Drive_A [01 ↔ 79] = ■■-■■
```

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.

Specify the number of sector accessed by one instruction in the following message.

```
Sector count ?
Drive_A [1, 3, 9] = ■
```

Type the sector count in the displayed count and press ENTER. Specify the number of retrial in the following message, when an error has occurred.

```
Retry count ? [0 ↔ 4] = ■
```

Type the retry count in the displayed range and press ENTER.

Specify whether to stop or continue the test, when an error has occurred.

```
Error stop ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER.
Specify whether to execute the test or not.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the checked drive". On the other hand, when entering "Yes", starts the test.

While the system executes the test, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test.
The lower left screen shows pass count and test point represented by physical address as follows:

```
Pass count = ■■■■■
Test point = TT.H.SS
```

"TT" means the track, "H" means the head and "SS" means the sector.
In addition, the lower right screen shows the test mode and the test drive.

```
Test mode: Write Test drive: Drive_A
```

• **Error processing**
If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on the lower right screen and increments the right-hand error counter.
If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER the system continues the test. On the other hand, by pressing ESC, the test terminates. For details of error message, see "8-5-12-7. Error message".

8-5-12-3. Read only check

This test checks that data is properly read from the floppy disk drive.

• **Operation**
When this test is selected, the following message is displayed.

```
Please insert the formatted scratch disk in the drive.
```

At the time, insert the test disk in the drive to be checked and press ENTER. If the drive is not ready or the test disk isn't inserted in the drive, the following message is displayed and the test terminates.

```
Drive not ready.
```

Specify whether to check the drive or not in the following message.

```
Drive_A (1.44MB) test ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. The string in the parenthesis represents the capacity of the disk.
Specify the range of cylinders to be checked in the following message.

```
Cylinder range ?
Drive_A [00 ↔ 79] = ■■-■■
```

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.
Specify the number of sector accessed by one instruction, in the following message.

```
Sector count ?
Drive-A [1, 3, 9] = ■
```

Type the sector count in the displayed count and press ENTER.
Specify the number of retrial in the following message, when an error has occurred.

```
Retry count ? [0 ↔ 4] = ■
```

Type the retry count in the displayed range and press ENTER.
Specify whether to stop or continue the test, when an error has occurred.

```
Error stop ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER.
Specify whether to execute the test or not.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When selecting "No", control exits to "specification of the checked drive". On the other hand, when selecting "Yes", starts the test.
While the system executes the test, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test.
The lower left screen shows pass count and test point represented by physical address.

```
Pass count = ■■■■■
Test point = TT.H.SS
```

"TT" means the track, "H" means the head and "SS" means the sector.
In addition, the lower right screen shows the test mode and the test drive.

```
Test mode: Read Test drive: Drive_A
```

• **Error processing**
If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on the lower right screen and increments the right-hand error counter.
If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER the system continues the test. On the other hand, by pressing ESC, the test terminates. For details of error message, see "8-5-12-7. Error message".

8-5-12-4.00 Track sensor adjustment

This program checks the 00 track sensor which detects the cylinder 0. The system moves the head from the cylinder 0 to cylinder 4 and returns the head to the cylinder 0. With such an operation, the system can observe a signal from the 00 track sensor as a pulse.

• **Operation**
Specify the drive to be checked in the following message.

```
Test drive ? [Drive_A]
```

Move the highlighting to the drive you want to select, and press ENTER.
Specify whether to repeat or do only once the test in the following message.

```
Aging mode ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When selecting "Yes", the test will be repeated. On the other hand, when selection "No", the test will be done only once.
Specify whether to execute the test or not.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When selecting "No", control exits to "specification of the checked drive". On the other hand, when selecting "Yes", starts the test.
In the aging mode, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test.
Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test. Otherwise, by pressing ESC, the test terminates. However, by pressing ENTER, the test is repeated again.

- **Error processing**

While the system executes the test, if an error occurs, the system displays the kind of error at the lower screen. In this state, by pressing any key, the test terminates. For details of error message, see "8-5-12-7. Error message".

8-5-12-5. Target sector read

This test is used to continue reading the specific sector.

- **Operation**

Specify the disk to be checked in the following message.

```
Please insert the alignment or formatted disk in the drive.
What kind of the test disk do you use ?
[Alignment_disk Formatted_disk]
```

At the time, insert the test disk in the drive to be checked and move the highlighting to the disk you inserted, and press ENTER. If the drive is not ready or the test disk isn't inserted in the drive, the following message is displayed and the test terminates.

```
Drive not ready.
```

Specify the drive to be checked in the following message.

```
Test drive ? [Drive_A]
```

Move the highlighting to the drive you want to select, and press ENTER.
Specify the cylinder number to be checked in the following message.

```
Cylinder number ? [00 ↔ 79] = ■■
```

Type the cylinder number to be checked in the displayed range and press ENTER.
Specify the head number to be checked in the following message.

```
Head number ? [0 ↔ 1]
```

Type the head number to be checked in the displayed range and press ENTER.
Specify the sector range to be checked in the following message.

```
Sector range ? [1 ↔ 9, 9 ↔ 18] = ■■-■■
```

Type the first sector number and the last sector number of the cylinder range to be checked and press ENTER. Also do not specify sectors which extend from 9 sector to 0 sector.

NOTE: When the alignment disk is selected, this specification of sector range is not displayed.

Specify whether to stop or continue the test if an error occurs while executing test.

```
Error stop ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. If the alignment disk is selected, select "No".
Specify whether to execute the test or not.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. when selecting "No", control exits to "specification of the checked drive". On the other hand, when selecting "Yes", starts the test.
While the system executes the test, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test.
The lower left screen shows pass count and test point represented by physical address.

```
Pass count = ■■■■■
Test point = TT.H.SS
```

"TT" means the track, "H" means the head and "SS" means the sector In addition, the lower right screen shows the test mode and the test drive.

```
Test mode: Read Test drive: Drive_A
```

- **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on the lower right screen and increments the right-hand error counter. If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information at the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER the system continues the test. On the other hand, by pressing ESC, the test terminates. For details of error message, see "8-5-12-7. Error message".

8-5-12-6. Error table display

All error kinds, locations and counts are displayed for "Write-read check" and "Read only check". However, this error information is limited to 40 locations.

- **Operation**

By pressing any key, the test terminates.

8-5-12-7. Error messages

- **FDC busy**

A read or write command is in process.

- **FDC seek error**

The system received a FAULT signal from the device or the seek operation was abnormally completed.

- **Communication error**

Handshake error occurred between the CPU and FDC.

- **Equipment check**

The system received a FAULT signal from a device or did not detect a track 00 signal in the specified time period while the recalibrate operated.

- **Missing address mark**

The address mark in the ID section was not detected.

- **FDC no data**

The ID without CRC error was not detected.

- **FDC invalid command**

A command written to the FDC was invalid.

• **Drive not ready**
The device being specified was in the not ready state.

• **Record not found**
The sector specified in the ID field could not be detected in the track

• **DMA boundary error**
DMA error across 64KB boundary.

• **Write protected error**
The system detected write protection.

• **Seek error**
Shows the occurrence of a error during seek.

• **Bad controller**
Shows the occurrence of any abnormality in the controller.

• **Bad address mark**
Shows the occurrence of an address mark read error.

• **Bad CRC error**
Shows the occurrence of a CRC error during data error.

• **Bad command error**
A command was specified which was not in BIOS.

• **Compare error**
Data being written did not accord with data being read.

• **Others error**
Shows the occurrence of other errors not described above.

8-5-13. Hard disk drive diagnostics

This program tests the hard disk drive.
The following menu appears when this test program is selected.
Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

```
Hard Disk Drive Diagnostics
Drive type check
Write, read & compare check
Read only check
Random seek check
Dump and Patch
Disk controller check
Error table display
```

8-5-13-1. Drive type check

This test item checks the specification of the drive if the drive is ready. The capacity, cylinder numbers, head numbers and sector numbers are displayed.

• **Operation**
Depression of any key terminates the test.

8-5-13-2. Write, read & compare check

This item checks the write/read operation.
The system writes the specified data to the hard disk, reads the same data from the floppy disk, and then compares them.
The specified data to be written is 00H to FFH increment pattern when the pass count is 0, otherwise the data is 2bytes repetitive pattern of "CB33".

• **Caution**
When this test is executed, all the contents stored in the disk are destroyed. So be very careful with this test.

• **Operation**
Specify the range of cylinders to be checked in the following message.

```
Cylinder range ?
[000 ↔ 964] = ■■■ - ■■■
```

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.
Specify the number of sector accessed by one instruction in the following message.

```
Sector count ?
[01 ↔ 17] = ■■
```

Type the sector count in the displayed range and press ENTER.
Specify the number of retrial in the following message, when an error has occurred.

```
Retry count ?
[0 ↔ 4] = ■
```

Type the retry count in the displayed range and press ENTER.
Specify whether to stop or continue the test in the following message, when an error has occurred.

```
Error stop ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER.
Specify whether to execute the test or not in the following message.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the cylinder range". On the other hand, when entering "Yes", starts the test.
While executing the test, by pressing SPACE, the system stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depressing of ESC is always effective during this test.
the lower left screen shows the pass count and the test point represented by physical address as follows:

```
Pass count =  ■■■■■
Test point =  CCC.HH.SS
```

"CCC" means the cylinder, "HH" means the head and "SS" means the sector.
In addition, the lower right screen shows the test mode.

```
Test mode: Write
```

• **Error processing**
If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen and increments the right-hand error counter.
If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER, the system continues the test and by pressing ESC, the test terminates.
For details of error message, see "8-5-13-8. Error message".

8-5-13-3. Read only check

The test checks if the read operation is normal by reading the data on the hard disk.

• **Operation**
Specify the range of cylinders to be checked in the following message.

```
Cylinder range ?
[000 ↔ 964] = ■■■ - ■■■
```

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.
Specify the number of sector accessed by one instruction in the following message.

```
Sector count ?
[01 ↔ 17] = ■■
```

Type the sector count in the displayed range and press ENTER.
Specify the number of retrial in the following message, when an error has occurred.

```
Retry count ?
[0 ↔ 4] = ■
```

Type the retry count in the displayed range and press ENTER.
Specify whether to stop or continue the test in the following message, when an error has occurred.

```
Error stop ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER.
Specify whether to execute the test or not in the following message.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. when entering "No", control exits to "specification of the cylinder range". On the other hand, when entering "Yes", starts the test.
While executing the test, by pressing SPACE, the system stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depressing of ESC is always effective during this test.
The lower left screen shows the pass count and the test point represented by physical address as follows:

```
Pass count =  ■■■■■
Test point =  CCC.HH.SS
```

"CCC" means the cylinder, "HH" means the head and "SS" means the sector.
In addition, the lower right screen shows the test mode.

```
Test mode: Read
```

- **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen and increments the right-hand error counter.
If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER, the system continues the test and by pressing ESC, the test terminates.
For details of error message, see "8-5-13-8. Error message".

8-5-13-4. Random seek check

The test checks if the seek operation is normal by accessing the hard disk at random.

- **Operation**

Specify whether to stop or continue the test in the following message, when an error has occurred.

```
Error stop ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER.
Specify whether to execute the test or not in the following message.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the cylinder range". On the other hand, when entering "Yes", starts the test.
While executing the test, by pressing SPACE, the system stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depressing of ESC is always effective during this test.
The lower left screen shows the pass count and the test point represented by physical address as follows:

```
Pass count =  ■■■■■
Test point =  CCC.HH.SS
```

"CCC" means the cylinder, "HH" means the head and "SS" means the sector.
In addition, the lower right screen shows the test mode.

```
Test mode: Read
```

- **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen and increments the right-hand error counter.
If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER, the system continues the test and by pressing ESC, the test terminates.
For details of error message, see "8-5-13-8. Error message".

8-5-13-5. Dump and Patch

The contents of the disk, the hexadecimal figure with the ASCII character, are displayed on the screen and are patched up. The contents of a sector (512KB) is displayed in two parts: the first half (256KB) and the second half (256KB).

- **Operation**

Specify the physical address to be dumped and patched.

```
Physical address = CCC.HH.SS
```

Type the cylinder number displayed by "CCC" and press ENTER. Type the head number displayed by "HH" and press ENTER. Type the sector number displayed by "SS".
When the entrys have been complete, the screen appears with the data of the specified sector on the screen.
At this time, by pressing PGDN, a next sector or a second half of the sector is displayed and by pressing PGUP, a previous sector or a first half of the sector is displayed on the screen.
Moreover, by pressing SPACE, control exits "specify the physical address" and by pressing ESC, the test terminates.
To patch up, move the highlighting to the location you want to patch and type the figure with hexadecimal and press ENTER. The following message display on the lower screen. At this time, specify whether to update or not.

```
Update data ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER.

• **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen.
For details of error message, see "8-5-13-8. Error message".

8-5-13-6. Disk controller check

The test checks the disk controller.

• **Operation**

Specify whether to repeat or do only once the test in the following message.

```
Aging mode ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When selection "Yes", the test will be repeated. On the other hand, when selecting "No", the test will be done only once.
Specify whether to execute the test or not in the following message.

```
Test start ? [Yes No]
```

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the aging mode". On the other hand, when entering "Yes", starts the test. Depression of ESC terminates the aging.

• **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen.
For details of error message, see "8-5-13-8. Error message".

8-5-13-7. Error table display

All error kinds, locations and counts are displayed for "Write, read & compare check", "Read only check" and "Random seek check". However, this error information is limited to 40 locations.

• **Operation**

By pressing any key, the test terminates.

8-5-13-8. Error message

• **Bad command**

Shows that an invalid command is received.

• **Bad address mark**

Shows that the occurrence of an address mark read error.

• **Record not found**

Shows that the specified record is not found.

• **DMA boundary error**

Shows that the DMA error across 64Kb boundary.

• **Bad track**

Shows that a bad track is found.

• **Bad ECC on disk read**

Shows that the occurrence of an ECC error during data read.

• **Data corrected**

A error occurred but shows that the error was corrected by ECC.

• **Seek error**

Shows that the occurrence of an error during seek.

• **Bad controller**

Shows that the occurrence of any abnormality in the controller.

• **Time out error**

Shows that an interrupt responses from the controller was not received in the prescribed time.

• **Compare error**

Shows that an unmatch of the write data with the read data.

• **Others error**

Shows that the occurrence of other errors not described above.

CHAPTER 9. APPENDICES

9-1. μPD70208G Main CPU (V-40)

1. Features

1-1. High-performance 8-bit CPU

- 1M-byte memory space and 64K-byte I/O space
- Abundant memory addressing modes
- Fourteen 16-bit register sets
- Instruction set with 101 types of powerful instructions
- Bit field manipulation instructions
- Packed BDC arithmetic operation instructions
- Memory-memory high-speed block transfer instructions
- High-speed multiplication and division instructions by exclusive hardware
- High-speed effective address calculation by exclusive hardware
- A wealth of interrupt process functions
- μPD8080AF emulation mode
- Standby mode

1-2. Internal clock generator

1-3. Programmable wait function

1-4. Dynamic RAM refresh function

1-5. Timer/counter unit

- Three 16-bit counters
- Six programmable count modes
- binary/BCD count
- Multiple-latch commands

1-6. Serial control unit

- Asynchronous serial communication
- Clock rate: Baud rate x16, x64
- Baud rate: DC to 48.4k bits/sec.
- Character length: 7/8 bits
- Transfer stop bit: 1/2 bits

1-10. IEEE-796 bus compatible interface

1-11. CMOS

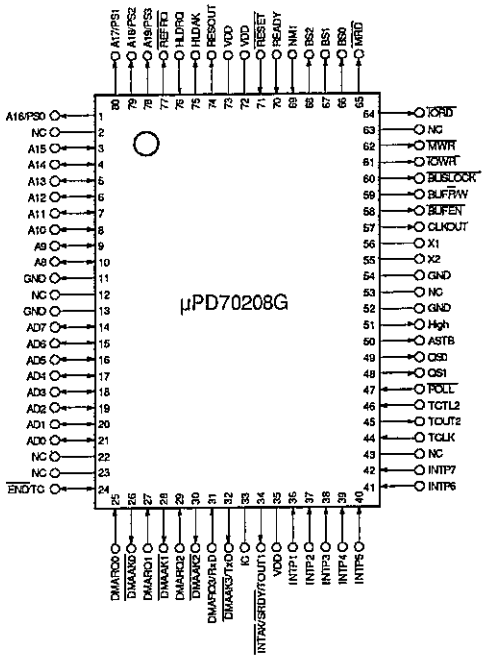
1-12. Low power consumption

1-13. Single power supply

1-14. 10-MHz clock

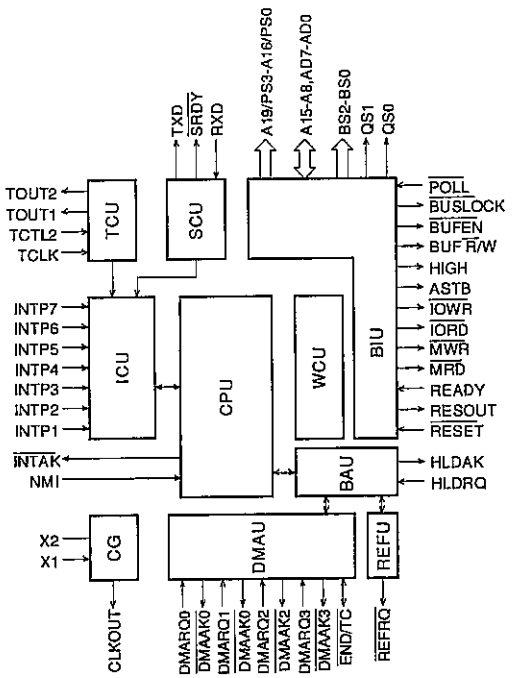
2. μPD70208G Pin Configurations

- 80-pin Plastic Flat Package (Top View)



NOTE: For μPD70208G, pins 3 to 10 are output only.

3. μPD70208G Block Diagram



4. Pin Function

4-1. AD7 to AD0 (address/data bus) ... 3-state input/output

These pins constitute a maltiplexed address/data bus that outputs the lower 8 bits of 20-bit address information and inputs/outputs 8-bit data on a time-division basis. These pins function as the address bus during T1 state of the bus cycle, and as the data bus during T2, T3, TW, and T4 states.
These pins become high impedance during hold acknowledge.

4-2. A15 to A8 (address bus) ... 3-state output

These pins output the middle 8 bits of 20-bit address information.
These pins become high impedance during hold acknowledge.

4-3. A19/PS3 to A16/PS0 (address bus/processor status) ... 3-state output

These are time-multiplexed output pins that output addresses and processor status signals.
These pins function as an address bus during T1 state of the bus cycle. They output processor status signals during T2, T3, TW, and T4 states.
When functioning as an address bus, these pins output the higher 4 bits of address information. All these pins output 0 during I/O access.
The processor status signal is output during both the memory and I/O accesses. The PS3 pin outputs 0 in native mode and when the cycle is neither DMA nor refresh; otherwise, it outputs 1. The PS2 pin outputs the content of the interrupt enable flag (IE).
The PS1 and PS0 pins indicate which segment is used by the current bus cycle.

Processor Status

A17/PS1	A16/PS0	Segment
0	0	Data segment 1 (DS1)
0	1	Stack segment (SS)
1	0	Program segment (PS)
1	1	Data segment 0 (DS0)

These pins become high impedance during hold acknowledge.

4-4. $\overline{\text{REFRQ}}$ (refresh request) ... Output

This is an output pin that outputs an active-low signal during T2, T3 and TW states of the refresh cycle.

4-5. HLDRQ (hold request) ... Input

This pin inputs a high-level signal when an external device requests that the address bus, address/data bus, and control bus be released. The priority of this signal is as follows: REFU (highest priority) > DMAU > HLDRQ > CPU > REFU (lowest priority).

4-6. HLDAK (hold acknowledge) ... Output

This signal indicates that the μPD70208/70216 has acknowledged the hold request signal (HLDRQ) and set the buses to the high-impedance state. When this signal is at the high level, therefore, the address bus, address/data bus, and control bus of 3-state output system become high-impedance state.
If a refresh request or DMA request with higher priority than the HLDAK signal occurs during hold acknowledge, HLDAK becomes inactive. Then the μPD70208G requests that the bus control be returned to it provided that the HLDRQ signal becomes inactive at the same time.

4-7. $\overline{\text{RESET}}$ (reset) ... Input

This is an active-low reset input pin and takes the precedence over all the other operations. The reset operation affects not only the CPU but also the on-chip peripherals. After the reset input is released, the CPU starts executing the program from address FFFF0H. The $\overline{\text{RESET}}$ input is also used to release the standby mode of the CPU.

4-8. RESOUT (reset output) ... Output

This pin synchronizes the asynchronous signal input to the $\overline{\text{RESET}}$ pin with the internal clock and then outputs it as an active-high signal. This signal can also be used as a system reset signal.

4-9. READY (ready) ... Input

The basic bus cycle of the μPD70208G requires four clocks. However, when the READY signal goes low (inactive) a wait state (TW) is inserted between T3 and T4 states and thus the bus cycle is extended. This function is used for memory or I/O whose access time is slow.
This signal is internally synchronized with the clock and supplied to each block. Then it is checked during T3 and TW states.
Other than by this signal, TW state can be also inserted by programmable wait function.

4-10. NMI (nonmaskable interrupt) ... Input

This pin inputs an interrupt request signal that cannot be masked by software.
This input signal is rising-edge triggered and is sampled in each clock cycle. When the current instruction has been executed, an interrupt assigned with No.2 vector is generated.
This interrupt is also used to release the standby mode of the CPU.

4-11. $\overline{\text{MRD}}$ (memory read) ... 3-state output

This signal becomes active (low level) when data is read from the memory. This signal also becomes active when the memory is refreshed by the on-chip refresh control unit or when data are transferred from the memory to I/O by the on-chip DMA control unit.
The $\overline{\text{MRD}}$ signal becomes active during T2, T3, and TW states of the bus cycle.
This pin becomes high impedance during hold acknowledge.

4-12. $\overline{\text{MWR}}$ (memory write) ... 3-state output

This signal becomes active (low level) when data are written to the memory. This signal also becomes active when data are transferred from the I/O to memory by the on-chip DMA control unit. When data are processed by the CPU, the $\overline{\text{MWR}}$ signal becomes active during T2, T3, and TW states. However, when data are processed by the DMA unit, the $\overline{\text{MWR}}$ signal becomes active during T3 and TW states.
This pin becomes high impedance during hold acknowledge.

4-13. $\overline{\text{IORD}}$ (I/O read) ... 3-state output

This signal becomes active (low level) when data are read from the I/O. However, if the I/O to be accessed is on the chip, it will not become active. The $\overline{\text{IORD}}$ signal also becomes active when data are transferred from the I/O to the memory by the on-chip DMA control unit. This signal becomes active during T2, T3 and TW states of the bus cycle.
This pin becomes high impedance during hold acknowledge.

4-14. $\overline{\text{IOWR}}$ (I/O write) ... 3-state output

This signal becomes active (low level) when data are written to the I/O. However, if the I/O to be accessed is on the chip, it will not become active. The $\overline{\text{IOWR}}$ signal also becomes active when data are transferred from the memory to I/O by the on-chip DMA control unit.
This signal becomes active during T2, T3, and TW states when data are processed by the CPU. However, when data are processed by the DMAU, the $\overline{\text{IOWR}}$ signal becomes active during T3 and TW states for normal write timing; T2, T3, and TW states for extended write timing.
This pin becomes high impedance during hold acknowledge.

4-15. ASTB (address strobe) ... Output

This signal is an active-high strobe signal that externally latches address information. This signal becomes active while the clock (CLKOUT) in T1 state of the bus cycle is at low level.
This pin outputs low-level signal during hold acknowledge.

4-16. $\overline{\text{BUSLOCK}}$ (bus lock) ... 3-state output

This signal is used to request the other master CPUs in the multiprocessor system not to use the system bus while the instruction following the BUSLOCK prefix is being executed or during interrupt acknowledge cycles.
During bus lock (i.e. $\overline{\text{BUSLOCK}}$ is active), hold request and DMA request are ignored, while refresh request is hold off.
This pin becomes high impedance during hold acknowledge.

4-17. $\overline{\text{POLL}}$ (poll) ... Input

The signal input to the $\overline{\text{POLL}}$ pin is checked by the POLL instruction. If the signal is at the low level, the program execution proceeds to the next instruction. If the $\overline{\text{POLL}}$ pin is at the high level, it is checked every five clocks until the $\overline{\text{POLL}}$ input goes low. These functions are used to synchronize the CPU program with the operations of external devices.

4-18. BUF$\overline{\text{R}}$/W (buffer read/write) ... 3-state output

This signal is output to determine the data transfer direction of an external bidirectional data buffer. If it is high level, data are output from the μPD70208G to the external device. If the signal is low level, data are input from the external device to the μPD70208G.
This pin becomes high impedance during hold acknowledge.

4-19. $\overline{\text{BUFEN}}$ (buffer enable) ... 3-state output

This signal is active low signal and is used as an output enable signal for the external bidirectional data buffer.
During T2 through T4 states of the read cycle and interrupt acknowledge cycle, it becomes active (low level). This signal also becomes active during T1 through T4 states of the write cycle.
However, the $\overline{\text{BUFEN}}$ pin will not become active when the internal I/O on the chip is accessed.
This pin becomes high impedance during hold acknowledge.

4-20. X2 and X1 (clock) ... Input

To use the internal clock generator, a crystal must be connected across the X2 and X1 pins. The oscillation frequency of the crystal to be connected should be 2 times the operating frequency.
If an external clock generator is to be used, the square wave of 2 times the operating frequency must be input to the X1 pin and the inverted signal of the X1 to the X2 pin.

4-21. CLKOUT (clock out) ... Output

This pin outputs the square wave clock that has one half the frequency of crystal frequency or X1 input frequency.

4-22. BS2 to BS0 (bus status) ... 3-state output

These pins output status signals that inform the external bus controller of the current bus cycle.
These signals become active during T1 and T2 states and are encoded as indicated in the table below. By decoding these encoded signals, the external bus controller can generate control signals by which to access the memory or I/O.
Only when CPU enters halt state, BS2 to BS0 indicates the CPU passive state one clock earlier than normal states.

BS2	BS1	BS0	Bus cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Program prefetch
1	0	1	Memory read*
1	1	0	Memory write (including DMA cycle)
1	1	1	CPU passive state

* In addition to the CPU read cycle, the "memory read cycle" includes the DMA cycle, DMA verify, and refresh cycle.

These pins become high impedance during hold acknowledge.

4-23. QS1 to QS0 (queue status) ... Output

These signals inform an external device (floating-point operation chip) of the CPU's internal instruction queue status.
The "queue status" means a status in which the execution unit (EXU) in the CPU accesses an instruction queue. The contents output to the QS1 and QS0 pins are valid only during one clock cycle immediately after the EXU has accessed the instruction queue.

QS1	QS0	Instruction queue status
0	0	No operation (no changing queue)
0	1	The first byte of an instruction is fetched.
1	0	The queue is empty.
1	1	The second or latter byte of the instruction is fetched.

The status signals are provided so that the floating-point operation chip can monitor the program execution status of the CPU and performs processing in synchronization with the CPU when the control is given to the chip by the FPO (floating point operation) instruction.

4-24. TOUT2 (timer output) ... Output

This is the output pin of the internal timer/counter unit (TCU). Of the three counters of the TCU, the result of the TCT#2 is output to this pin.

4-25. TCTL2 (timer control) ... Input

This is the control input pin of the internal timer/counter unit (TCU). Of the three counters, the TCT#2 is controlled by this input.

4-26. TCLK (timer clock) ... Input

This is the clock input pin of the internal timer/counter unit. However, the clock actually input to each counter is selected by software from either the clock input to this pin or the operating clock of the μPD70208G on which frequency division has been performed.

4-27. INTP7 to INTP1 (interrupt request from peripheral) ... Input

These seven pins input asynchronous interrupt requests to the internal interrupt control unit (ICU). Either edge-triggering (at the rising edge) or level-triggering (high level) of these input signals can be selected. These interrupt request inputs can be also used to release the standby mode of the CPU.
These pins have internal pull-up resistors.

4-28. $\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1 (interrupt acknowledge/serial ready/timer output) ... Output

This is a shared output pin for interrupt acknowledge signal, serial ready signal, and timer output (TCT#1). The interrupt acknowledge signal $\overline{\text{INTAK}}$ becomes active (low level) during T2, T3, and TW states of the interrupt acknowledge cycle of the CPU. The $\overline{\text{SRDY}}$ signal is output from the internal serial control unit (SCU) and becomes active (low level) when the receiver is enabled to receive data.
The TOUT1 signal is output from the internal timer/counter unit (TCU). Of the three counters, a result of the TCT#1 is output to this pin. The functions of this pin is selected by controlling the OPCN (on-chip peripheral connection) register in the μPD70208G by software.

4-29. $\overline{\text{DMAAK3}}$/TxD (DMA acknowledge/transmit data) ... Output

This is a shared pin and outputs the acknowledge signal for channel 3 of the DMA unit and serial data from the serial control unit (SCU).

The $\overline{\text{DMAAK3}}$ signal is active-low.

When this pin functions as the TxD pin, it becomes high level (marking) if there is no transmit data. When transmit data is set, the start bit (low level) is automatically output and then the set data is serially output. A parity bit and a stop bit (high level) are appended to the end of the each data. Whether to append the parity bit can be specified by program.

The μPD70208G's internal OPCN (on-chip peripheral connection) register controls the function of this pin (refer to 12.1, System I/O Area).

4-30. DMARQ3/RxD (DAM request/receive data) ... Input

This is a shared pin that inputs the request signal for channel 3 of the DMA unit and the serial data of the SCU.
The DMARQ3 signal is active-high.
When this pin functions as the RxD pin, a high-level (marking) signal is input to it when no data is transmitted. The RxD pin starts receiving data at the falling edge of the start bit.

Pin election	$\overline{\text{DMAAK3}}$/TxD	DMARQ3/RxD	$\overline{\text{INTAK}}$/SRDY/TOUT1
1	$\overline{\text{DMAAK3}}$	DMARQ3	$\overline{\text{INTAK}}$
2	$\overline{\text{DMAAK3}}$	DMARQ3	TOUT1
3	TxD	RxD	$\overline{\text{INTAK}}$
4	TxD	RxD	$\overline{\text{SRDY}}$

The three pins described in Sections 4-28 through 4-30 can be specified in the following four ways by controlling register OPCN (on-chip peripheral connection) of the μPD70208G by software.

4-31. $\overline{\text{DMAAK2}}$ to $\overline{\text{DMAAK0}}$ (DMA acknowledge) ... Output

These pins output the DMA acknowledge signals from channels 2 through 1 of the DMA unit.
These signals are active-low.

4-32. DMARQ2 to DMARQ0 (DMA request) ... Input

These pins input the DMA request signals to channels 2 through 0 of the DMA unit.
These signals are active-high.

4-33. $\overline{\text{END}}$/$\overline{\text{TC}}$ (end/terminal count) ... Input/output

This active-low pin controls termination of data transfer by DMA when the data transfer is performed by the DMA unit. When a low-level pulse ($\overline{\text{END}}$) is input to this pin during the DMA transfer, the DMA unit will terminate the ongoing DMA servicing. Also, when the number of DMA ransfers specified for each channel is complete, this pin outputs a low-level pulse ($\overline{\text{TC}}$).
Because this pin is an open-drain, a pull-up resistor must be externally connected.

4-34. V_{DD} (power supply)

This is a positive power supply pin.

4-35. GND (ground)

This is a ground pin (0V).

4-36. IC (internally connected)

Don't connect any signal with this pin and must be left open.

5. Functional Blocks

5-1. CPU (central processing unit)

The CPU consists of two independent processing units: BCU (bus control unit) and EXU (execution unit). Each of these two units performs the following function.

BCU ..... Prefetches instructions using instruction queues (the instruction queue is 4-byte for the μPD70208G.
EXU..... Processes data (executes microprograms).

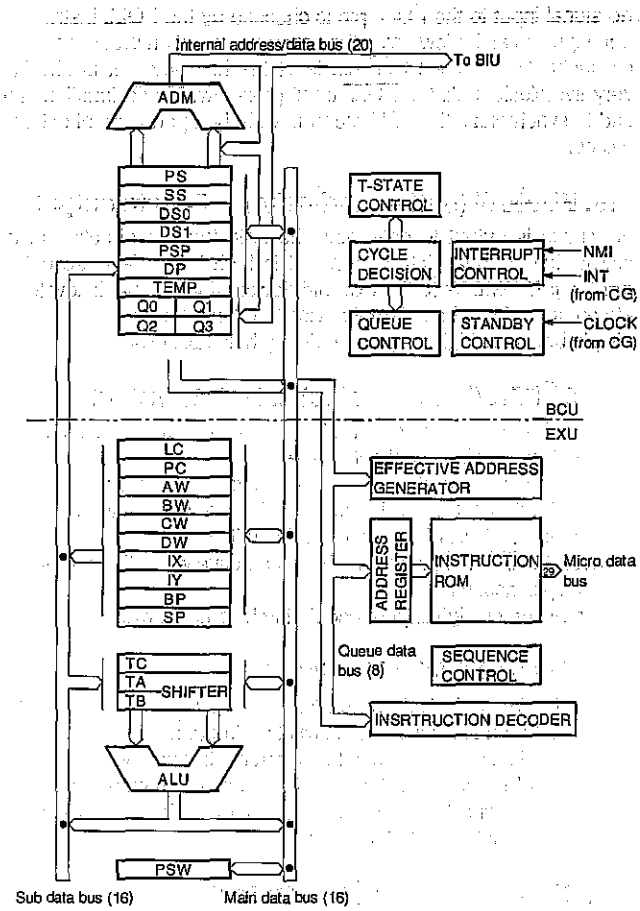


Fig. 5-1 μPD70208G CPU block diagram

5-2. BIU (bus interface unit)

The BIU controls the pins constituting the data bus, address bus, and control bus. These buses are used by three functional blocks: the CPU, DMAU (DMA control unit), and REFU (refresh control unit). The BIU synchronizes the $\overline{\text{RESET}}$ and READY inputs using the clock signal generated by the clock generator. The synchronized reset signal is active-high that is used in the μPD70208G as well as supplied to an external device via the RESOUT pin. The synchronized READY signal is supplied to the internal CPU, DMAU, and REFU.

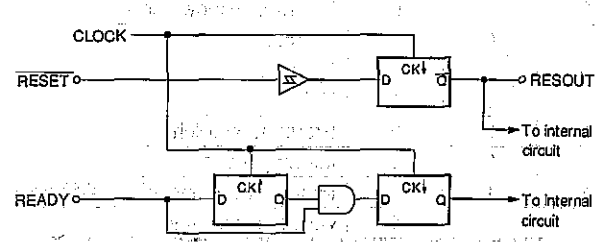


Fig. 5-2 Synchronization of $\overline{\text{RESET}}$ and READY

5-3. BAU (bus arbitration unit)

The BAU performs the bus control arbitration. The bus control priority is as follows:

REFU (highest priority) > DMAU > HLDRQ > CPU > REFU (lowest priority)

The REFU can take either the highest or lowest priority depending on the pending status of the refresh request. Even when a bus is used by a bus master, if another bus master with the higher priority requests the bus control, the BAU requests the current bus master to return the bus control by inactivating the acknowledge signal (i.e., bus acknowledge signal to the CPU, DMAU, or REFU, or the HLDAK signal to an external device). When the bus request signal (i.e., bus request signal from the CPU, DMAU, or REFU, or the HLDRQ signal from an external device) becomes inactive in response to this bus relinquish request, the BAU gives the bus control to the bus master with the higher priority.

When the bus control is sent between the internal bus masters, bus control request, acknowledge, relinquish request, and relinquish are efficiently performed.

5-4. CG (clock generator)

The CG generates clock signal one half the frequency of the crystal connected across the X1 and X2 pins and provides the clock to the CLKOUT pin and each functional block of the μ70208G. The duty cycle of the generated clock signal is 50%.

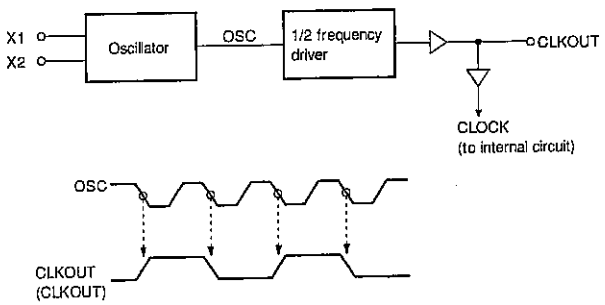


Fig. 5-3 Clock generator

5-5. REFU (refresh control unit)

The REFU generates refresh addresses and refresh request signals. By using these, the memory, if it is a dynamic RAM, can be refreshed.

5-6. WCU (programmable wait control unit)

The WCU has a function to insert up to three clocks of wait states TW to compensate for the process speeds of low-speed memories or I/O's. The number of clocks per wait state TW can be independently specified for CPU access, DMA access, and refresh access. Especially, when accessing the CPU, the memory space can be divided into three areas. These three areas and I/O can be independently specified.

5-7. TCU (timer/counter unit)

the TCU is a timer/counter unit. Three independent counters are provided in the TCU. The output signal of one of the counters is supplied to internal blocks whereas that of another one is supplied to external devices. The output of the last counter can be supplied to both internal and external devices.

5-8. SCU (serial control unit)

The SCU performs asynchronous serial communication.

5-9. ICU (interrupt control unit)

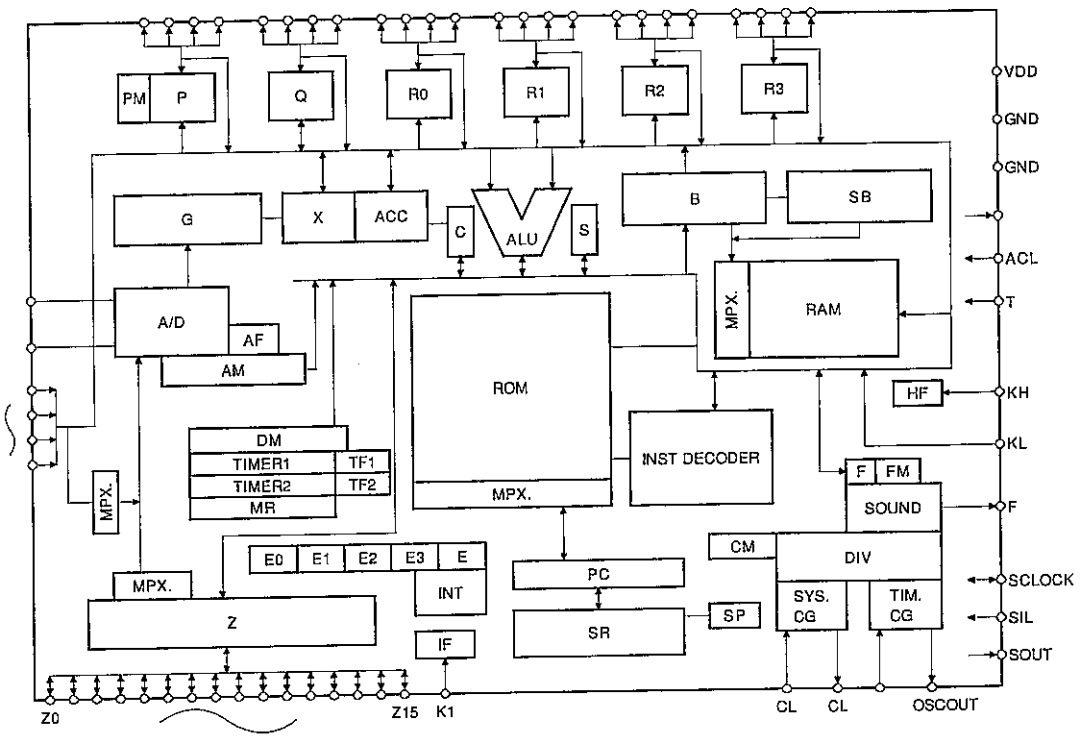
The ICU is an interrupt control unit, and arbitrates eight interrupt requests, generates an interrupt request that is to be sent to the CPU, and sends the interrupt vector number to the CPU. One of the eight interrupt request lines is not externally connected but it is connected to an output of the internal timer/counter.

5-10. DMAU (DMA control unit)

The DMAU is a DMA control unit and controls data transfer performed by using DMA (Direct Memory Access) between the memory and I/O.

9-2. LU57844P SUB CPU (SCM)

1) Block diagram



2) Sub CPU (SCM) pin description

Signal name	Pin	In/Out	Function
IPC0	P0	In/Out	Bi-directions: Host I/F port
IPC1	P1	In/Out	
IPC2	P2	In/Out	
IPC3	P3	In/Out	
PVCRT	Q00	Out	CRT Power switch
PVMDM	Q01	Out	Not used
PON (PVCC)	Q02	Out	VCC Power switch
KSTRA	Q03	Out	Key strobe line
KSEN0	R00	In	Key sense line (0 thru 7)
KSEN1	R01	In	
KSEN2	R02	In	
KSEN3	R03	In	
KSEN4	R10	In	
KSEN5	R11	In	
KSEN6	R12	In	
KSEN7	R13	In	
LED1	R20	Out	Caps Lock LED
LED2	R21	Out	Num Lock LED
LED3	R22	Out	Scrl Lock LED
*RESET	R23	Out	System Reset (active low)
FDN0 (SW7)	R30	Out	Not used
FDN1 (SW8)	R31	Out	Not used
COM1/2	R32	Out	COM1/*COM2 select
TKPDEW	R33	In	Ten-key-pad select switch (High)
KSTR0	Z0	Out	Key strobe line (0 thru 10)
KSTR1	Z1	Out	(KSTROBE0=SLP/RES key strobe)
KSTR2	Z2	Out	(KSTROBE1=ON SW strobe)
KSTR3	Z3	Out	
KSTR4	Z4	Out	
KSTR5	Z5	Out	
KSTR6	Z6	Out	
KSTR7	Z7	Out	
KSTR8	Z8	Out	
KSTR9	Z9	Out	(KSTROBE8, 9=Low Batt LED)
KSTR10	Z10	Out	(KSTROBE10=V-reference)
CPUHS	Z11	In	Host hand shake signal
SCMHS	Z12	Out	SCM hand shake signal
BKLIGHT	Z13	Out	Back-light control
KCLKOUT	Z14	Out	KEY I/F clock out
LB	Z15	Out	Low Battery Signal for HDD
KCLKIN	KI	In	KEY I/F clock in
ON/OFF	KH	In	ON SW sense
KDATAIN	KL	In	KEY I/F data in
LOWBAT0	KC0	An: Out/In	Low battery FATAL Level
LOWBAT1	KC1	An: Out/In	Low battery WARNING level
ACPOWER	KC2	An: Out/In	AC adaptor
*RI	KC3	In	Ring indicator
KDATAOUT	SOUT	Out	KEY I/F data out
SSPKR	F	Out	Low Battery Beep.
VCCHK	SIN	In	V_{CC} check

* means active low signal.

9-3. 8087
NUMERIC DATA COPROCESSOR
8087-1

- **High Performance Numeric Data Coprocessor**
- **Adds Arithmetic, Trigonometric, Exponential, and Logarithmic Instructions to the Standard 8086/8088 and 80186/80188 Instruction Set for All Data Types**
- **CPU/8087 Supports 7 Data Types: 16-, 32-, 64-Bit Integers, 32-, 64-, 80-Bit Floating Point, and 18-Digit BCD Operands**
- **Compatible with IEEE Floating Point Standard 754**
- **Adds 8 x 80-Bit Individually Addressable Register Stack to the 8086/8088 and 80186/80188 Architecture**
- **7 Built-In Exception Handling Functions**
- **MULTIBUS® System Compatible Interface**

The 8087 Numeric Data Coprocessor provides the instructions and data types needed for high performance numeric applications, providing up to 100 times the performance of a CPU alone. The 8087 is implemented in N-channel, depletion load, silicon gate technology (HMOS III), housed in a 40-pin package. sixty-eight numeric processing instructions are added to the 8086/8088, 80186/80188 instruction sets and eight 80-bit registers are added to the register set. The 8087 is compatible with the IEEE Floating Point Standard 754.

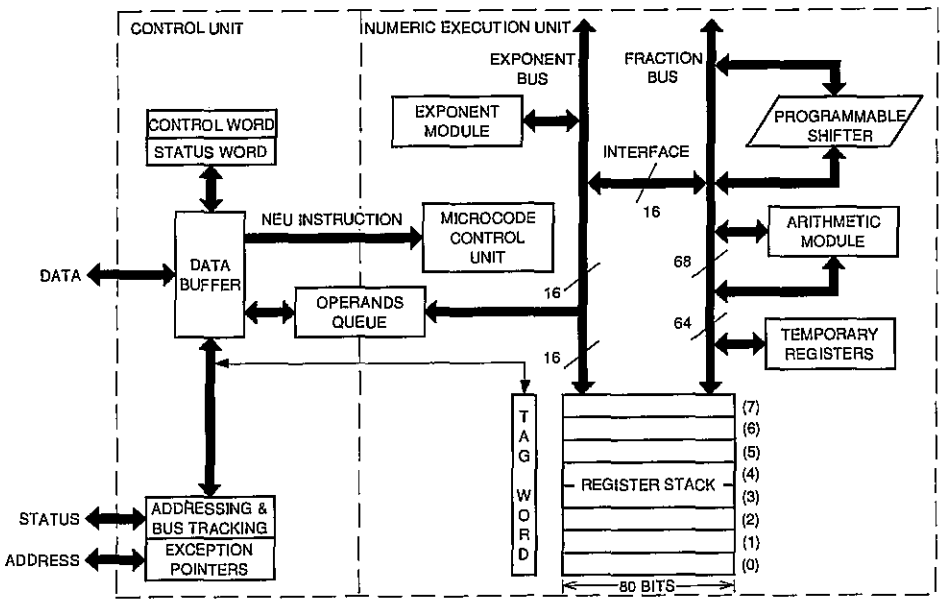


Figure 1. 8087 Block Diagram

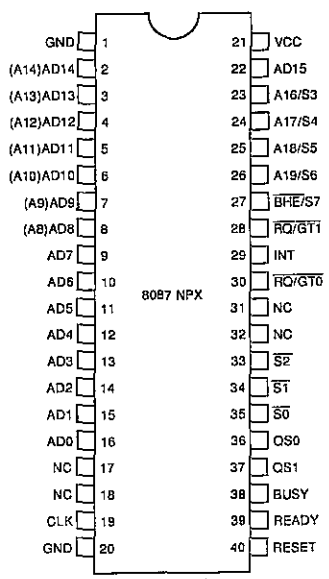


Figure 2. 8087 Pin Configuration

Table 1. 8087 Pin Description

Symbol	Type	Name and Function
AD15 – AD0	I/O	**ADDRESS DATA:** These lines constitute the time multiplexed memory address (T_1) and data (T_2, T_3, T_W, T_4) bus. A0 is analogous to the $\overline{BHE}$ for the lower byte of the data bus, pins D7 – D0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory operations. Eight-bit oriented devices tied to the lower half of the bus would normally use A0 to condition chip select functions. These lines are active HIGH; they are input/output lines for 8087-driven bus cycles and are inputs which the 8087 monitors when the CPU is in control of the bus. A15 – A8 do not require an address latch in an 8088/8087 or 80188/8087; the 8087 will supply an address for the T_1 – T_4 period.
A19/S6, A18/S5, A17/S4, A16/S3	I/O	**ADDRESS MEMORY:** During T_1 these are the four most significant address lines for memory operations. During memory operations, status information is available on these lines during T_2, T_3, T_W, and T_4. For 8087-controlled bus cycles, S6, S4, and S3 are reserved and currently one (HIGH), while S5 is always LOW. These lines are inputs which the 8087 monitors when the CPU is in control of the bus.
BHE/S7	I/O	**BUS HIGH ENABLE:** During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15 – D8. Eight-bit-oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read and write cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T_2, T_3, T_W, and T_4. The signal is active LOW. S7 is an input which the 8087 monitors during the CPU-controlled bus cycles.
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	I/O	**STATUS:** For 8087-driven, these status lines are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ 0 (LOW) X X Unused 1 (HIGH) 0 0 Unused 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive Status is driven active during T_4, remains valid during T_1 and T_2, and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller (or the 82188 Integrated Bus Controller with an 80186/80188 CPU) to generate all memory access control signals. Any change in $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These signals are monitored by the 8087 when the CPU is in control of the bus.
$\overline{RQ}/GT0$	I/O	**REQUEST/GRANT:** This request/grant pin is used by the 8087 to gain control of the local bus from the CPU for operand transfers or on behalf of another bus master. It must be connected to one of the two processor request/grant pins. The request/grant sequence on this pin is as follows: 1. A pulse one clock wide is passed to the CPU to indicate a local bus request by either the 8087 or the master connected to the 8087 $\overline{RQ}/GT1$ pin. 2. The 8087 waits for the grant pulse and when it is received will either initiate bus transfer activity in the clock cycle following the grant or pass the grant out on the $\overline{RQ}/GT1$ pin in this clock if the initial request was for another bus master. 3. The 8087 will generate a release pulse to the CPU one clock cycle after the completion of the last 8087 bus cycle or on receipt of the release pulse from the bus master on $\overline{RQ}/GT1$. For 80186/80188 systems the same sequence applies except $\overline{RQ}/GT$ signals are converted to appropriate HOLD, HLDA signals by the 82188 Integrated Bus Controller. This is to conform with 80186/80188's HOLD, HLDA bus exchange protocol. Refer to the 82188 data sheet for further information.

Table 1. 8087 Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{RQ}/\overline{GT}1$	I/O	**REQUEST/GRANT:** This request/grant pin is used by another local bus master to force the 8087 to request the local bus. If the 8087 is not in control of the bus when the request is made the request/grant sequence is passed through the 8087 on the $\overline{RQ}/\overline{GT}0$ pin one cycle later. Subsequent grant and release pulses are also passed through the 8087 with a two and one clock delay, respectively, for resynchronization. $\overline{RQ}/\overline{GT}1$ has an internal pullup resistor, and so may be left unconnected. If the 8087 has control of the bus the request/grant sequence is as follows: 1. A pulse 1 CLK wide from another local bus master indicates a local bus request to the 8087 (pulse 1). 2. During the 8087's next T_4 or T_1 a pulse 1 CLK wide from the 8087 to the requesting master (pulse 2) indicates that the 8087 has allowed the local bus to float and that it will enter the "RQ/GT acknowledge" state at the next CLK. The 8087's control unit is disconnected logically from the local bus during "RQ/GT acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 8087 (pulse 3) that the "RQ/GT" request is about to end and that the 8087 can reclaim the local bus at the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW. For 80186/80188 system, the $\overline{RQ}/\overline{GT}1$ line may be connected to the 82188 Integrated Bus Controller. In this case, a third processor with a HOLD, HLDA bus exchange system may acquire the bus from the 8087. For this configuration, $\overline{RQ}/\overline{GT}1$ will only be used if the 8087 is the bus master. Refer to 82188 data sheet for further information.
QS1, QS0	I	**QS1, QS0:** QS1 and QS0 provide the 8087 with status to allow tracking of the CPU instruction queue. **QS1** **QS0** 0 (LOW) 0 No Operation 0 1 First Byte of Op Code from Queue 1 (HIGH) 0 Empty the Queue 1 1 Subsequent byte from Queue
INT	O	**INTERRUPT:** This line is used to indicate that an unmasked exception has occurred during numeric instruction execution when 8087 interrupts are enabled. This signal is typically routed to an 8259A for 8086/8088 systems and to INT0 for 80186/80188 systems. INT is active HIGH.
BUSY	O	**BUSY:** This signal indicates that the 8087 NEU is executing a numeric instruction. It is connected to the CPU's $\overline{TEST}$ pin to provide synchronization. In the case of an unmasked exception BUSY remains active until the exception is cleared. BUSY is active HIGH.
READY	I	**READY:** READY is the acknowledgement from the addressed memory device that it will complete the data transfer. The RDY signal from memory is synchronized by the 8284A Clock Generator to form READY for 8086 systems. For 80186/80188 systems, RDY is synchronized by the 82188 Integrated Bus Controller to form READY. This signal is active HIGH.
RESET	I	**RESET:** RESET causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. RESET is internally synchronized.
CLK	I	**CLOCK:** The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}		**POWER:** V_{CC} is the +5V power supply pin.
GND		**GROUND:** GND are the ground pins.

NOTE: For the pin descriptions of the 8086, 8088, 80186 and 80188 CPUs, reference the respective data sheets (8086, 8088, 80186, 80188).

9-4. TC8566F Floppy Disk Controller II

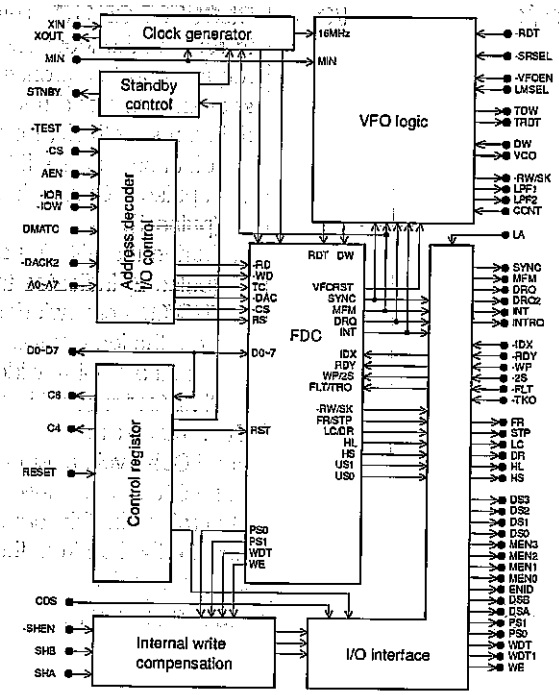
1) General

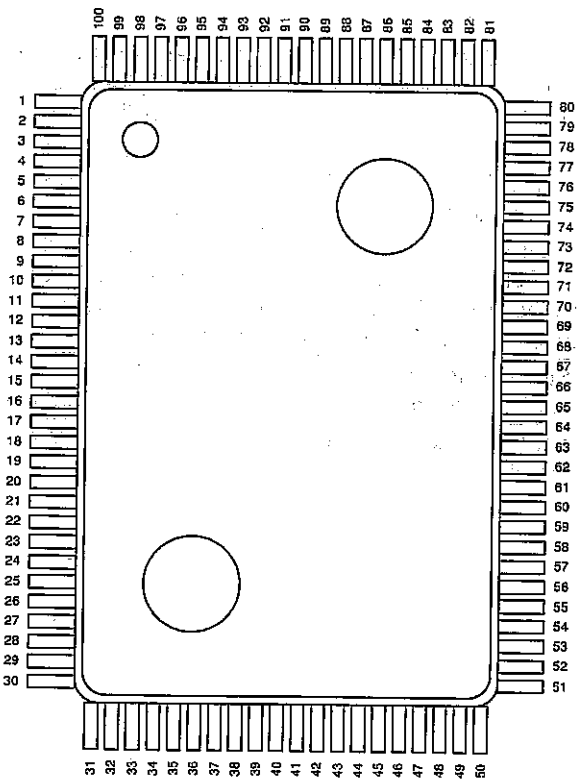
The TC8586F is a floppy disk control microchip designed to interface four floppy disk unit with the CPU. In this chip is implemented a high performance VFO circuitry and peripheral logic circuitry.

2) Features

- ❑ Silicon gate CMOS
- ❑ Single 5V supply
- ❑ 100-pin flat package
- ❑ Internal oscillator
- ❑ Internal VFO
- ❑ Internal standby circuit
- ❑ FD/MFD selection
- ❑ FM/MFM recording mode
- ❑ Internal write compensation
- ❑ Motor enable output control
- ❑ Internal I/O address decoder
- ❑ Multi-sector, multi-track
- ❑ Simultaneous seek, 4 drives
- ❑ Drive interface Schmitt trigger input
- ❑ Programmable step rate
- ❑ IBM compatible track format
- ❑ Internal CRC generation and check (X16+X12+X5+1)
- ❑ Programmable head load and unload time
- ❑ Data scan function
- ❑ DMA/non-DMA data transfer

3) TC8566F block diagram





4) Signal description

Pin No.	Signal name	In/Out	Description
1	C6	Out	Control register C6 output
2	$\overline{IOR}$	In	Signal used to transfer data onto the data bus from the FDC.
4	$\overline{IOW}$	In	Control signal to transfer data from the data bus to FDC.
5	A0	In	Address signal
6	A1	In	
7	A2	In	
8	A3	In	
9	A4	In	
10	A5	In	
11	A6	In	
12	A7	In	
13	$\overline{CS}$	In	FDC chip select
14	AEN	In	Address enable from the CPU
15	D0	In/Out	Bidirectional 8-bit data bus
16	D1	In/Out	
17	D2	In/Out	
18	D3	In/Out	
19	D4	In/Out	
20	D5	In/Out	
21	D6	In/Out	
22	D7	In/Out	
23	DRQ2	Out	DMA request. Output to delay DRQ. The signal is at a low level when the control register ENID bit is 0.
24	INTRQ	Out	Interrupt request issued by the FDC. The signal is at a low level when the control register ENID bit is 0. This signal stays low.
25	INT	Out	Interrupt request issued from the FDC.
26	DRQ	Out	DMA request
27	[VSS]	G	FDC digital ground
28	AG	G	VCO analog ground
32	$\overline{DACK2}$	In	DMA cycle becomes valid with a low state of this as input at DMA transfer.
33	DMATC	In	Indicates end of DMA during DMA transfer.
34	CONT	In	VCO control voltage input
35	$\overline{TEST}$	In	Test input with a pullup resistance. Normally, not to be connected or fixed high.
36	VCO	In/Out	Test input in the test mode, but normally output. To be connected with the low gain side filter.
37	LPF2	Out	Output connected to LPF of the PLL circuit. Selected after leading frequency. To be connected with the low gain side filter.
38	LPF1	Out	Output connected to LPF of the PLL circuit. Selected after leading frequency. To be connected with the high gain side filter.
39	CW	Out	Test input. Not to be connected.
40	DW	In	Data window input signal required when using external VFO circuit. Normally, low or high fixed.
41	FLT1	Out	Test input used to indicate filter switching. Not to be connected.
42	DOS	Out	Test input. Not to be connected.
43	LOCK	In	Test input with a pullup resistance. Normally, not to be connected or fixed high.
44	$\overline{RDT}$ (RDT)	In	Data read signal from the floppy disk drive. When the external VFO circuit is used, it is a data read signal (RDT) input from the external VFO circuit.
45	XOUT	Out	Crystal oscillator inverter amp output pin.
46	XIN	In	Crystal oscillator inverter amp input pin which is used for the 16MHz external clock.
47	$\overline{VFOEN}$	In	Internal VFO select signal. Internal VFO is selected with a low state of signal and the external VFO is chosen with a high state of signal.
48	MIN	In	Used to select the standard floppy disk and mini-floppy disk. Low: Standard floppy disk High: Mini-floppy disk
49	MFM	Out	High: MFM mode Low: FM mode
53	$\overline{CL}$	In	This pin incorporates a pullup resistance and is used to reset the internal clock generator and VFO flip-flop with a low state of signal. Normally, not to be connected or fixed high.
54	[VSS]	G	FDC digital ground
55	SYNC	Out	Indicates that the FDC is in reading action.

9-6. LZ95H12 (Gate array)

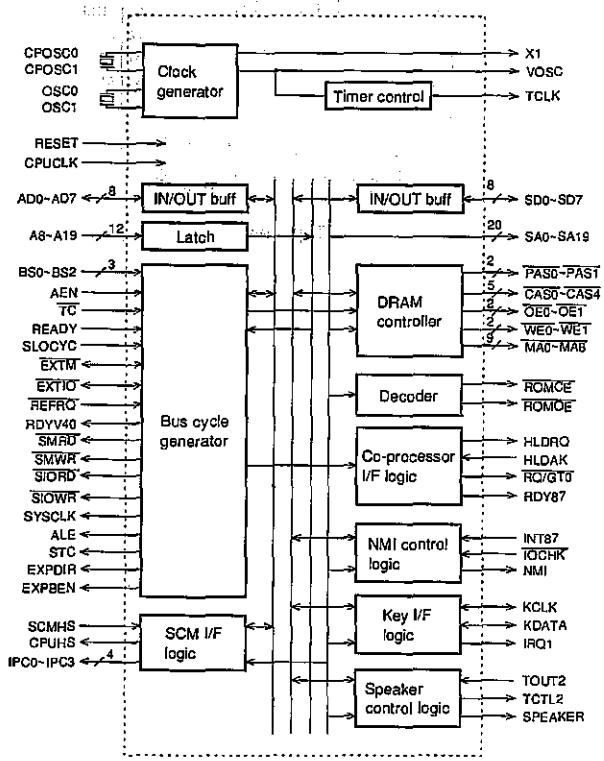
General

The LZ95H12 may be used together with a LZ93J21, a V40 and optionally, a 8087.

The LZ95H12 incorporates the following functions:

1. V40/system address bus interfacing;
2. V40/system data bus interfacing;
3. V40 oscillator selection;
4. bus cycle generator and IO channel interface;
5. 8087 interface;
6. system ROM interface;
7. DRAM control signal generation;
8. system timer clock generation;
9. speaker control;
10. keyboard interface;
11. configuration switch port;
12. NMI control and IO trapping;
13. SCM interface; and
14. internal I/O register interface.

LZ95H12 Block Diagram



LZ95H12

No.	Signal name	I/O	Description
1	$\overline{WE1}$	O	Not used
2	$\overline{OE0}$	O	DRAM output enable
3	$\overline{OE1}$	O	Not used
4	RESET	I	System reset signal inut
5	$\overline{ROMCE}$	O	ROM chip enable
6	$\overline{ROMOE}$	O	ROM output enable
7	BS0	I	Bus status 0
8	BS1	I	Bus status 1
9	BS2	I	Bus status 2
10	AD0	I/O	AD bus 0
11	AD1	I/O	AD bus 1
12	AD2	I/O	AD bus 2
13	AD3	I/O	AD bus 3
14	AD4	I/O	AD bus 4
15	AD5	I/O	AD bus 5
16	Vcc		
17	GND		
18	AD6	I/O	AD bus 6
19	AD7	I/O	AD bus 7
20	A8	I	CPU address 8
21	A9	I	CPU address 9
22	A10	I	CPU address 10
23	A11	I	CPU address 11
24	A12	I	CPU address 12
25	A13	I	CPU address 13
26	A14	I	CPU address 14
27	A15	I	CPU address 15
28	A16	I	CPU address 16
29	A17	I	CPU address 17
30	A18	I	CPU address 18
31	A19	I	CPU address 19
32	RDY87	O	Ready signal for 8087
33	RDYV40	O	Ready signal for V40
34	$\overline{REFRQ}$	I	Refresh request
35	$\overline{RQ/GT0}$	I/O	Request/Grant 0
36	IRQ87	I	Interrupt request from 8087
37	HLDAK	I	Bus hold acknowledge
38	HLDRQ	O	Bus hold request
39	TCLK	O	Timer clock
40	TCTL2	O	Timer 2 control
41	TOUT2	I	Timer 2 output
42	IRQ1	O	Interrupt 1
43	NMI	O	Non-maskable interrupt
44	$\overline{TC}$	I	Terminal count
45	CPUCLK	I	CPU clock
46	X1	O	Connected with X1 pin of V40
47	CPOSC0	O	Connected with 20MHz crystal
48	CPOSC1	I	
49	GND		
50	Vcc		
51	VOSC	O	Clock output for LZ93J21
52	OSC0	O	Connected with 14.31818MHz crystal
53	OSC1	I	
54	AEN	I	DMA or refresh active signal
55	$\overline{EXTM}$	I/O	External memory active signal

Pin No.	Signal name	In/Out	Description
56	WDT1	Out	FDD write data compensation output signal. Active low when LA is high.
57	WE	Out	Used to direct the FDD to write data. Active low when LA is high.
58	HS	Out	Head 0 is selected with a low state of this signal when LA is at a low level. Head 1 is selected with a low state of this signal when LA is at a low level.
59	HL	Out	Used to direct the FDD to load the read/write head on the disk. Active low when LA is at a low level.
60	MEN3	Out	Number 3 unit drive motor enable, active low when LA is at a high level.
61	MEN2	Out	Number 2 unit drive motor enable, active low when LA is at a high level.
62	MEN1	Out	Number 1 unit drive motor enable, active low when LA is at a high level.
63	MEN0	Out	Number 0 unit drive motor enable, active low when LA is at a high level.
64	[VSS]	G	FDC digital ground
65	[VDD]	V	Single 5V supply. All VDD lines connected to +5V.
66	DS3	Out	Indicates that the number 3 unit is selected, active low when LA is at a high level.
67	DS2	Out	Indicates that the number 2 unit is selected, active low when LA is at a high level.
68	DS1	Out	Indicates that the number 1 unit is selected, active low when LA is at a high level.
69	DS0	Out	Indicates that the number 0 unit is selected, active low when LA is at a high level.
70	STP	Out	Used to deliver step pulse to move the head to another cylinder, active low when LA is at a high level.
71	FR	Out	Used to reset a fault of the FDD, active low when LA is at a high level.
72	LC	Out	Indicates that the read/write head is on the cylinder position after the 43rd cylinder, active low when LA is at a high level.
73	DR	Out	Indicates the direction of the head in the seek mode. Seeks towards disk periphery with a low state of this signal and disk center with a high state of this signal when LA is at a low level. Seeks towards the disk periphery with a high state of this signal and disk center with a low state of this signal when LA is at a high level.
74	[VSS]	G	FDC digital ground
75	[VDD]	V	Single +5V supply. All VDD lines are connected to +5V.
76	$\overline{IDX}$	In	Indicates the start point of track on the disk.
77	$\overline{RDY}$	In	Indicates that the FDD is ready.
80	$\overline{WP}$	In	Indicates that the disk is write protected.
81	$\overline{2S}$	In	Indicates the use of two-sided floppy disk.
82	$\overline{FLT}$	In	Indicates that the FDD is at a fault.
83	$\overline{TK0}$	In	Indicates that the head is on track 0.
84	PS1	Out	Indicates write compensation information in the MFM mode.
85	PS0	Out	Late if PS0 is at a low and PS1 at a high. Early if PS0 is at a high and PS1 at a low. Normal if PS0 is at a low and PS1 at a low.
86	DSB	Out	FDD select signal. #0 drive: DSB=low, DSA=low #1 drive: DSB=low, DSA=high #2 drive: DSB=high, DSA=low #3 drive: DSB=high, DSA=high
87	DSA	Out	
88	LA	In	Determines logic of the drive side output. WDT1, WE, HG, HL, MEN0 ~ MEN3, DS0 ~ D53, STP, FR, LC, DR are active low with a high state of this signal.
90	[VDD]	V	Single +5V supply. All VDD lines are connected to +5V.
92	CDS	In	Control register DSB and DSA are selected as drive select signal with a high state of this signal. Internal FDC block US1 and US0 are selected as drive select signal with a low state of this signal.
93	RESET	In	Resets the contents of control register.
94	SHB	In	Used to indicate rate of shift for the write.
95	SHA	In	Compensation circuit. 125ns when SHB is low and SHA low. 250ns when SHB is low and SHA high. 375ns when SHB is high and SHA low. 500ns when SHB is high and SHA high. One half of the above values is used for the standard floppy disk.
96	$\overline{SHEN}$	In	Used to set SHB and SHA valid. Rate of shift becomes 0 for the write compensation circuit when the signal is at a high level.
97	STNBY	Out	Indicates that the FDC is at standby. WDT1, WE, HG, HL, MEN0 ~ MEN3, DS0 ~ DS3, STP, FR, LC, DR are active low when in the standby mode.
98	WDT	Out	FDD write data composed of clock bits and data bits.
99	ENID	Out	Control register ENID bit output.
100	C4	Out	Control register C4 output.

9-5. INS82C50A asynchronous communication element

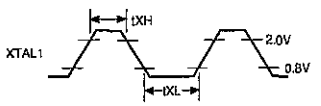
1. General description and features

- Enhances interface with almost any microprocessor
- Add/delete of suffixed bit(s) (START, STOP, PARITY) for async communication
- Full double buffer method that does not require precise synchronization
- Independently controlled transmit, receive, line status, data set interrupts
- 1 – (216 – 1) divided programmable buad rate generator (Internal 16 x clock generation)
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI, DCD)
- Serial interface format full compatible
  - 5, 6, 7, 8 bits character size
  - Even, off, non parity
  - 1, 1-2/1, stop bits
  - Baud rate generation (DC ~ 56K bauds)
- Illogical start bit detection
- Variety of status information
- Bidirectional data bus, control bus directly controlled tri-state TTL driver
- Start and detect of line break
- Internal self-diagnostics
  - Device internal loopback control
  - Break, parity, overrun, framing error simulation
- Interrupt controlled with priority

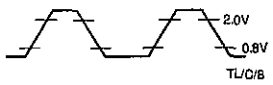
Timing waveforms

All waveforms are explained in reference to bit 0 and 1.

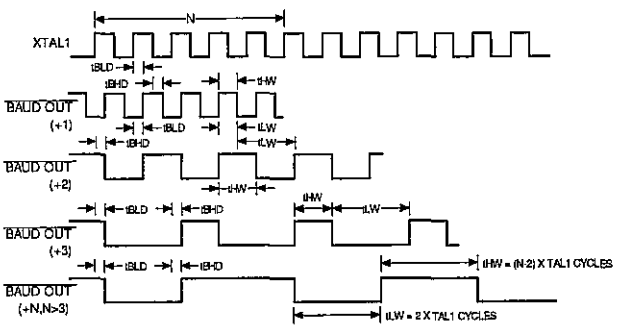
Internal clock (3.1MHz,max.)



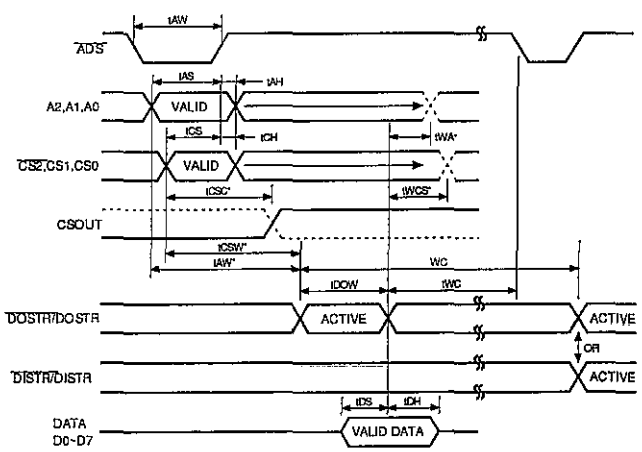
AC test point



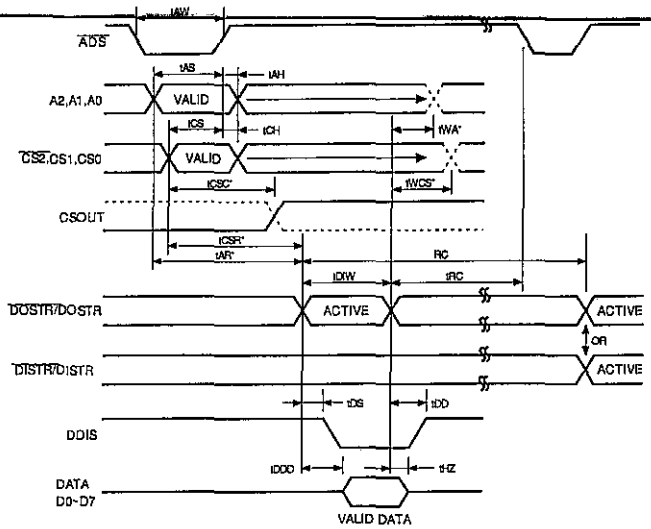
BAUDOUT timing



Write cycle

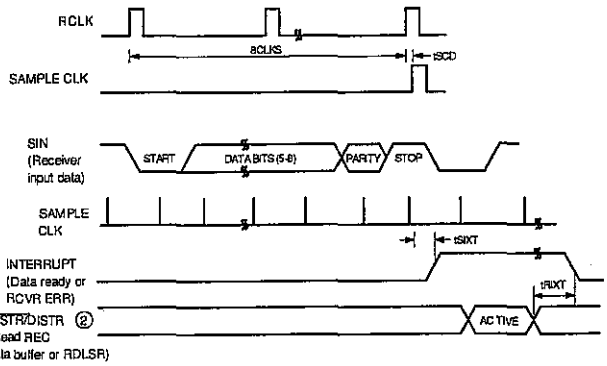


Read cycle

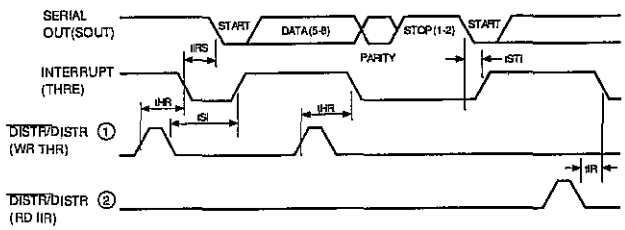


ADS fixed to low level for measurement

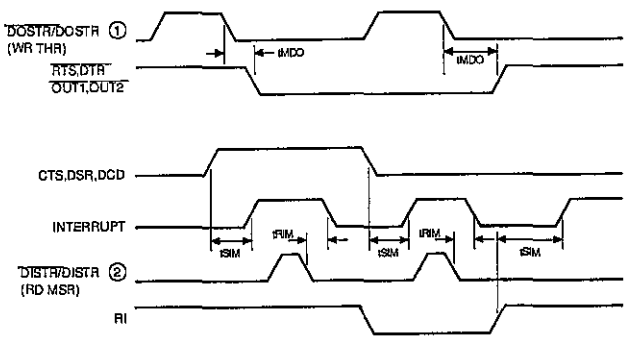
Receiver timing



Transmitter timing

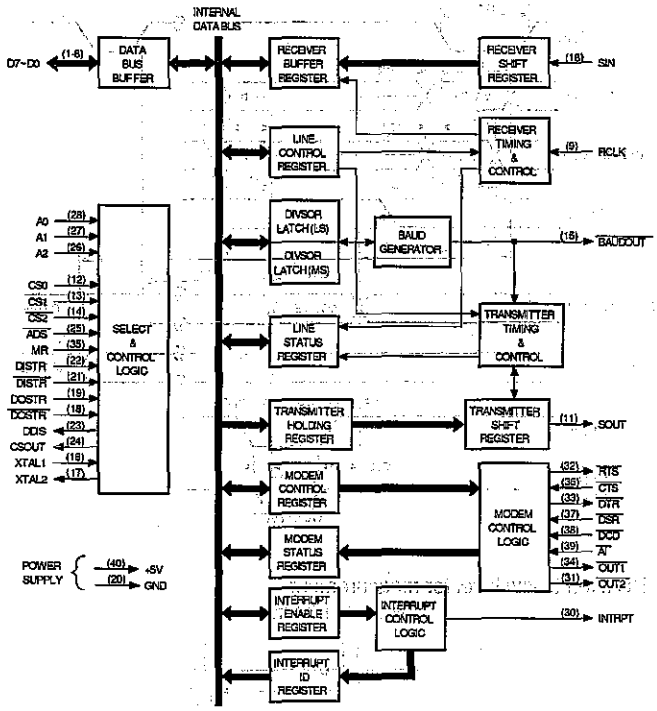


Modem control timing



① : Refer to write cycle.
② : Refer to read cycle.

2. Block diagram



3. Pin description

Discussed below are functions of I/O signal lines. Some of those relate to the internal circuitry.

NOTE: In the discussion, low level signal means logic 0 and high level signal logic 1.

INPUT SIGNALS

Chip select (CS0, CS1, $\overline{CS2}$, pin-12 to pin-14)

The chip is selected with a high state of CS0 and CS1 and low state of $\overline{SC2}$. Chip is selected by latching the decoded chip select signal at a trail edge of the address strobe signal $\overline{ADS}$. When the chip is selected, communication is enabled between the ACE and the CPU.

Data input strobe (DISTR, $\overline{DISTR}$, pin-22 and 21)

When DISTR input is at a high or $\overline{DISTR}$ is at a low after the chip was selected, status information from the ACE selected register and data are read by the CPU.

NOTE: When either $\overline{DISTR}$ or DISTR is set active, the data will be read from the ACE to the CPU. Therefore, $\overline{DISTR}$ must be set low or DISTR low when the line is not used.

Data output strobe (DOSTR, $\overline{DOSTR}$, pin-19 and 18)

When DOSTR is at a high or $\overline{DOSTR}$ is at a low after the chip was selected, data or control word are written to thee ACE selected register.

NOTE: Either $\overline{DOSTR}$ or DOSTR must be set active to write to ACE. Therefore, DOSTR must be set low or $\overline{DOSTR}$ high when the line is not used.

Address strobe ($\overline{ADS}$, pin-25)

When this line is low, the register select signals (A0, A1, A2) and chip select signals (CS0, CS1, $\overline{CS2}$) are latched.

NOTE: The ADS input is used when register select signals (A0, A1, A2) and chip select signals (CS0, CS1, $\overline{CS2}$) are not stable. The signal must be set low for such this that this input is not required.

DLAB	A2	A1	A0		Register
0	0	0	0	R	Receive buffer (holding register)
0	0	0	0	W	Trensmit buffer (holding register)
0	0	0	1		Interrupt mask
X	0	1	0		Interrupt ID
X	0	1	1		Line control
X	1	0	0		Modem control
X	1	0	1	R	Line status
X	1	1	0	R	Modem status
X	1	1	1		Scratch pad
1	0	0	0		Baud rate divide register, LSB
1	0	0	1		Baud rate divide register, MSB

R: Read only register
W: Write only register

Register select (A0, A1, A1, pin-26 to pin-28)

Used to select the register during read or write.

As shown in the table, the divisor latch access bit (DLAB) which is the most significant bit of the line control register relates to register selection. In order to access the baud rate generator divisor latch, the DLAB bit must be set 1 by the system software.

Master reset (MR, pin-35)

A TTL compatible schmitt trigger buffer that has a 0.5 (standard) hysteresis is implemented in this input line. When the line is at a high level, all registers and control logics are cleared, except for the receiver buffer, transmit holding, and divisor latch. Also, the output signals (SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) change as in Table-1.

Receiver clock (RCLK, pin-9)

A 16 x clock input line that has a receiver circuit.

Serial input (SIN, pin-10)

Serial data input line from the communication link (peripheral device, modem, data terminal).

Clear to send ($\overline{CTS}$, pin-36)

CTS is a modem control signal whose state is tested by referring to the bit 4 (CTS) of the modem status register. The bit 0 (DCTS) of the modem status register is set 1 when there was a change in the state of the $\overline{CTS}$ input in the period that this register is read after the modem status register was read. The $\overline{CTS}$ input does not affect the transmitter at all.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the CTS bit of the modem status register.

Data set ready ($\overline{DSR}$, pin-37)

A low on this line indicates that the modem or the data set is ready to receive and send. For $\overline{DSR}$ is a modem control input, its state can be tested by referring to the bit 5 (DSR) of the modem status register. The bit 1 (DDSR) of the modem status register is set 1 when there was a change in the state of the $\overline{DSR}$ input in the period that this register is read after the modem status register was read.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the DSR bit of the modem status register.

Data carrier detect ($\overline{DCD}$, pin-38)

A low on this line indicates that data carrier is detected by the modem or data set. For $\overline{CD}$ is a modem control input, its state can be tested by referring to the bit 7 (DCD) of the modem status register. The bit 3 (DDCD) of the modem status register is set 1 when there was a change in the state of the $\overline{DCD}$ input in the period that this register is read after the modem status register was read.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the $\overline{DCD}$ bit of the modem status register.

Ring indicator 8-$\overline{RI}$, pin-39)

A low on this line indicates that ring is detected by the modem or data set. For $\overline{RI}$ is a modem control input, its state can be tested by referring to the bit 6 (RI) of the modem status register. The bit 2 (TERI) of the modem status register is set 1 when there was a change in the state of the $\overline{RI}$ input in the period that this register is read after the modem status register was read.

NOTE: An interrupt is caused when the modem status interrupt is enabled and that there was a change in the RI bit of the modem status register.

VCC: pin-40
+5V supply
VSS: pin-20
GND (0V), reference voltage ground

OUTPUT SIGNAL DESCRIPTION

Data terminal ready ($\overline{DTR}$, pin-33)

A low on this line indicates that the ACE is enabled to communicate with the modem or the data set. $\overline{DTR}$ turns active when the bit 0 (DTR) of the modem control register is set by the program. This output is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Request to send ($\overline{RTS}$, pin-32)

A low on this line indicates that the ACE is enabled to send data to the modem or the data set. $\overline{RTS}$ turns active when the bit 1 (RTS) of the modem control register is set by the program. This output is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Output-1 ($\overline{OUT1}$, pin-34)

A general purpose output line which goes active low when the bit 2 (OUT1) of the modem control register is set by the program. $\overline{OUT1}$ is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Output-2 ($\overline{OUT2}$, pin-31)

A general purpose output line which goes active low when the bit 3 (OUT2) of the modem control register is set by the program. $\overline{OUT2}$ is set high level after the master reset is conducted. During the loopback mode, the signal is held high level.

Chip select out (CSOUT, pin-24)

A high level signal is issued on this line when CS0, CS1, and $\overline{SC2}$ are set high to select chip. Data are not sent out until CSOUT goes high.

Driver select out (DDIS, pin-23)

Goes low when ACE data are read by the CPU. When the CPU is reading other than data, the line is kept high. Used to disable an external data transceiver which is established on the data bus D7 ~ D0 between the CPU and the ACE.

Baud out ($\overline{BAUDOUT}$, pin-15)

The 16 x clock used in the ACE transmitter circuitry is sent out. The clock frequency is the value the basic clock input is divided by the value set in the baud rate divisor latch. When the $\overline{BAUDOUT}$ output is connected to the RCLK input, it can also be used for the receiver clock.

Interrupt (INTRPT, pin-30)

Goes active when one of receiver error flag, receive data available, transmitter holding register empty, and modem status interrupts is requested. If the corresponding IER bit was set, the line goes high. The INTR output is reset low after the master reset is conducted or an adequate interrupt service is done.

Serial output (SOUT, pin-11)

Through this line is sent out the serial data to the communication link (modem or data set). The line is set high (MARK) when the master reset is conducted.

INPUT/OUTPUT PIN DESCRIPTION

Data bus (D7 ~ D0, Pin-1 to -8)

An eight line tri-state input/output used to carry bidirectional data communication between the ACE and the CPU. Data, control word, and status information are transferred via this data bus.

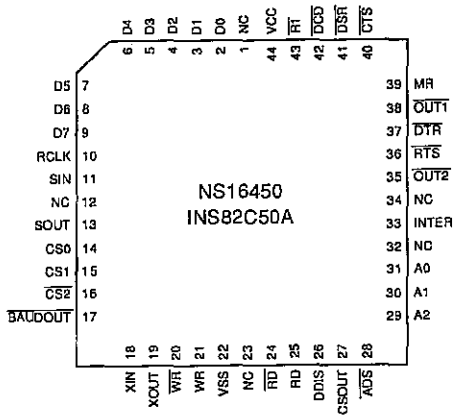
External clock input/output (XTAL1, XTAL2, pin-16 and 17)

Connected to the basic clock input (crystal oscillator or external clock).

NOTE: Pin numbers described are for the dual in-line package.

Pin Configuration

PLCC package



Top view

No.	Signal name	I/O	Description
56	$\overline{\text{EXTIO}}$	I/O	External I/O active signal
57	SLOCYC	I	Signal to decide bus cycle
58	EXPDIR	O	Not used
59	$\overline{\text{EXPBEN}}$	O	Not used
60	$\overline{\text{IOCHK}}$	I	Not used
61	READY	I	Ready
62	STC	O	Terminal count output
63	SYSCLK	O	System clock
64	ALE	O	Address latch enable
65	SD0	I/O	System data bus 0
66	SD1	I/O	System data bus 1
67	SD2	I/O	System data bus 2
68	SD3	I/O	System data bus 3
69	SD4	I/O	System data bus 4
70	SD5	I/O	System data bus 5
71	SD6	I/O	System data bus 6
72	SD7	I/O	System data bus 7
73	SA0	O	System address bus 0
74	SA1	O	System address bus 1
75	SA2	O	System address bus 2
76	SA3	O	System address bus 3
77	SA4	O	System address bus 4
78	SA5	O	System address bus 5
79	SA6	O	System address bus 6
80	Vcc		
81	GND		
82	SA7	O	System address bus 7
83	SA8	O	System address bus 8
84	SA9	O	System address bus 9
85	SA10	O	System address bus 10
86	SA11	O	System address bus 11
87	SA12	O	System address bus 12
88	SA13	O	System address bus 13
89	GND		
90	SA14	O	System address bus 14
91	SA15	O	System address bus 15
92	SA16	O	System address bus 16
93	SA17	O	System address bus 17
94	SA18	O	System address bus 18
95	SA19	O	System address bus 19
96	$\overline{\text{SMRD}}$	O	System memory read
97	$\overline{\text{SMWR}}$	O	System memory write
98	$\overline{\text{SIORD}}$	O	System I/O rend
99	$\overline{\text{SIOWR}}$	O	System I/O write
100	SPEAKR	O	Speaker signal
101	KCLK	I/O	Key clock
102	KDATA	I/O	Key data
103	CPUHS	O	Signal for handshake CPU-SCM
104	SCMHS	I	Signal for handshake CPU-SCM
105	IPC0	I/O	IPC bus 0
106	IPC1	I/O	IPC bus 1
107	IPC2	I/O	IPC bus 2
108	IPC3	I/O	IPC bus 3
109	MA0	O	Multiplexed DRAM address 0
110	MA1	O	Multiplexed DRAM address 1
111	MA2	O	Multiplexed DRAM address 2
112	Vcc		

No.	Signal name	I/O	Description
113	GND		
114	MA3	O	Multiplexed DRAM address 3
115	MA4	O	Multiplexed DRAM address 4
116	MA5	O	Multiplexed DRAM address 5
117	MA6	O	Multiplexed DRAM address 6
118	MA7	O	Multiplexed DRAM address 7
119	MA8	O	Multiplexed DRAM address 8
120	GND		
121	$\overline{\text{RAS0}}$	O	DRAM-RAS output
122	$\overline{\text{RAS1}}$	O	DRAM-RAS output
123	$\overline{\text{CAS0}}$	O	DRAM-CAS output
124	$\overline{\text{CAS1}}$	O	DRAM-CAS output
125	$\overline{\text{CAS2}}$	O	DRAM-CAS output
126	$\overline{\text{CAS3}}$	O	DRAM-CAS output
127	$\overline{\text{CAS4}}$	O	DRAM-CAS output
128	$\overline{\text{WE0}}$	O	DRAM write enable

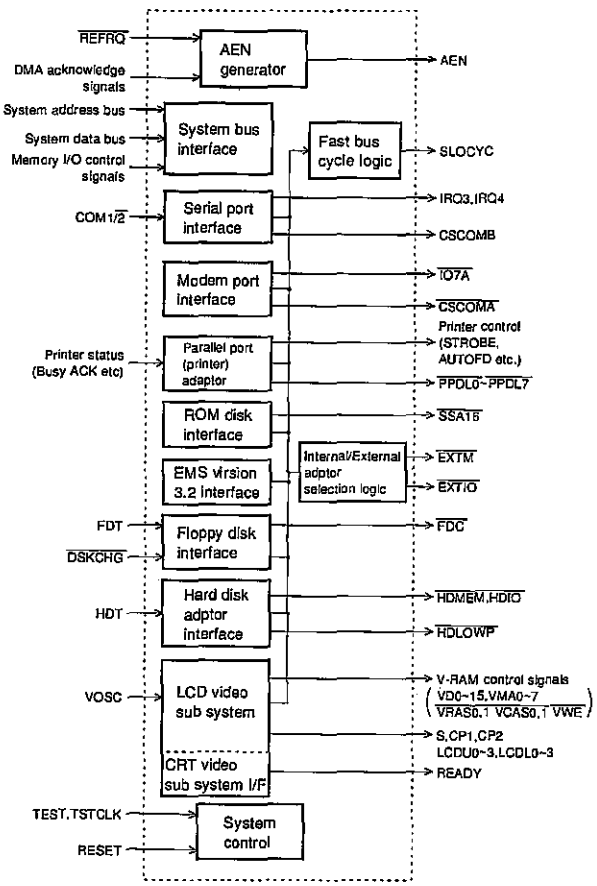
9-7. LZ93J21 (Gate array)

General

The LZ93J21 may be used together with a LZ95H12, a V40 and optionally. The LZ93J21 incorporates the following functions:

1. system bus interface;
2. AEN generation;
3. serial port interface;
4. modem port interface;
5. parallel port adapter;
6. ROM disk interface;
7. EMS Version 3.2 interface;
8. floppy disk adapter extension;
9. hard disk adapter interface;
10. CRT video subsystem interface;
11. LCD video subsystem;
12. fast bus cycle logic; and
13. internal/external adapter selection logic.

LZ93J21 Block Diagram



LZ93J21 signal description

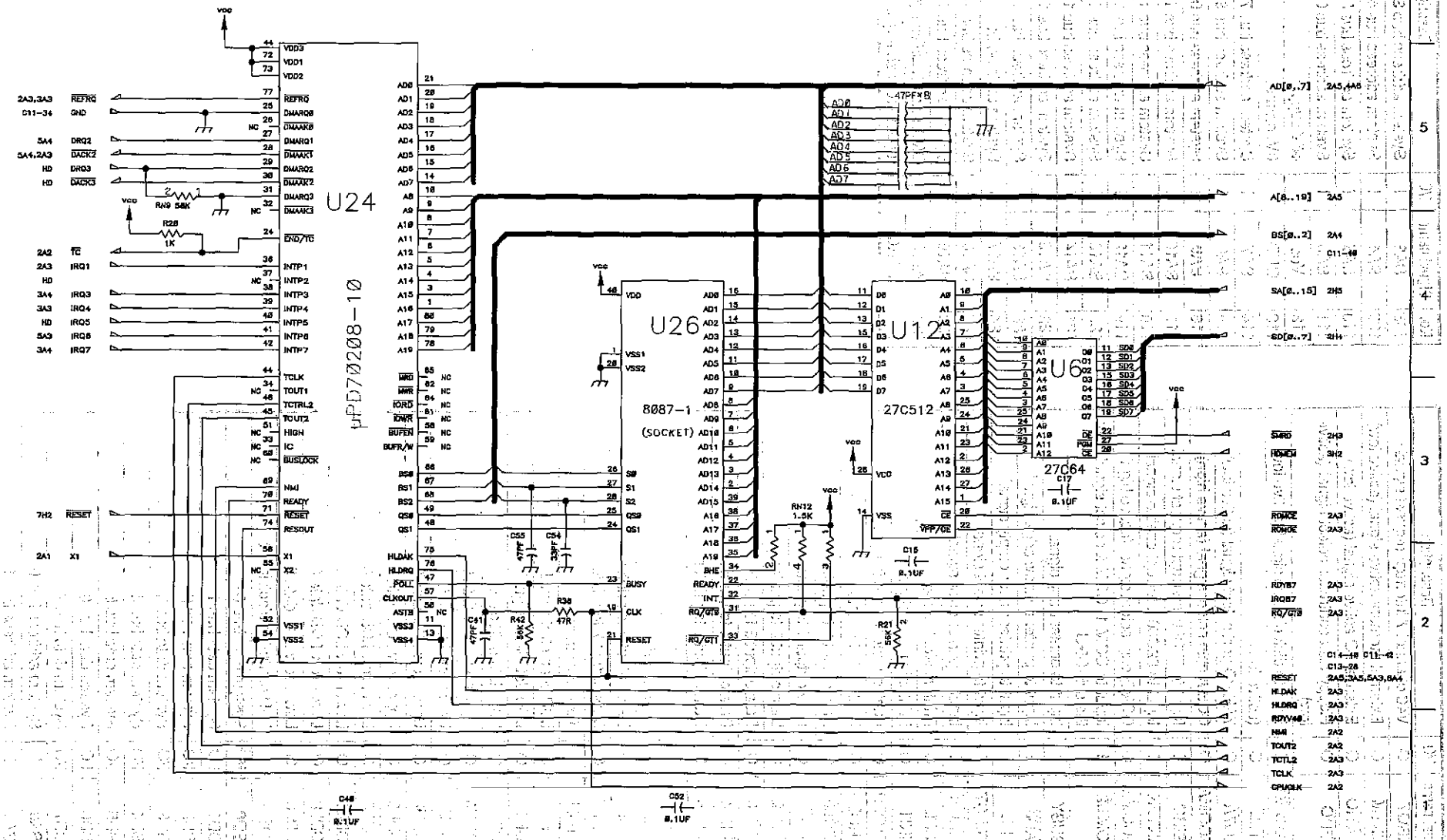
No.	Signal name	I/O	Description
1	$\overline{\text{DACK1}}$	I	Input to V40 channel 0 DMA acknowledge
2	$\overline{\text{DACK2}}$	I	Input to V40 channel 1 DMA acknowledge
3	$\overline{\text{DACK3}}$	I	Input to V40 channel 2 DMA acknowledge
4	$\overline{\text{SMRD}}$	I	Input to active low memory read signal
5	$\overline{\text{SMWR}}$	I	Input to active low memory write signal
6	$\overline{\text{SIORD}}$	I	Input to active low I/O read signal
7	$\overline{\text{SIOWR}}$	I	Input to active low I/O write signal
8	VD0	I/O	LCD VRAM data bus 0
9	VD1	I/O	LCD VRAM data bus 1
10	VD2	I/O	LCD VRAM data bus 2
11	VD3	I/O	LCD VRAM data bus 3
12	VD4	I/O	LCD VRAM data bus 4
13	VD5	I/O	LCD VRAM data bus 5
14	VD6	I/O	LCD VRAM data bus 6
15	VD7	I/O	LCD VRAM data bus 7
16	Vcc		+5V supply
17	GND		0V, ground
18	VD8	I/O	LCD VRAM data bus 8
19	VD9	I/O	LCD VRAM data bus 9
20	VD10	I/O	LCD VRAM data bus 10
21	VD11	I/O	LCD VRAM data bus 11
22	VD12	I/O	LCD VRAM data bus 12
23	VD13	I/O	LCD VRAM data bus 13
24	VD14	I/O	LCD VRAM data bus 14
25	VD15	I/O	LCD VRAM data bus 15
26	VMA0	O	LCD VRAM address bus 0
27	VMA1	O	LCD VRAM address bus 1
28	VMA2	O	LCD VRAM address bus 2
29	VMA3	O	LCD VRAM address bus 3
30	VMA4	O	LCD VRAM address bus 4
31	VMA5	O	LCD VRAM address bus 5
32	VMA6	O	LCD VRAM address bus 6
33	VMA7	O	LCD VRAM address bus 7
34	TEST	I	Test pin
35	$\overline{\text{VRAS0}}$	O	LCD VRAM 0 row address select signal (active low)
36	$\overline{\text{VRAS1}}$	O	LCD VRAM 1 row address select signal (active low)
37	$\overline{\text{VCAS0}}$	O	LCD VRAM 0 column address select signal (active low)
38	$\overline{\text{VCAS1}}$	O	LCD VRAM 1 column address select signal (active low)
39	$\overline{\text{VWE}}$	O	LCD VRAM write enable signal (active low)
40	$\overline{\text{HDMEM}}$	O	Hard disk memory select signal (active low)
41	$\overline{\text{HDIO}}$	O	Hard disk I/O select signal (active low)
42	$\overline{\text{SSA16}}$	O	EMS memory card system address bus 16
43	HDLOWP	O	Not used
44	HDT	I	1: HD 0: FD
45	FDT	I	LOW.
46	READY	O	Bus cycle ready signal
47	SLOCYC	O	Slow bus cycle select signal
48	RESET	I	Reset signal input (active high)
49	GND		
50	Vcc		
51	IRQ3	O	V40 channel 3 interrupt request signal
52	IRQ4	O	V40 channel 4 interrupt request signal

No.	Signal name	I/O	Description
53	IRQ7	O	V40 channel 7 interrupt request signal
54	$\overline{EXTM}$	O	External memory active signal (active low)
55	$\overline{EXTIO}$	O	External I/O active signal (active low)
56	$\overline{FDC}$	O	Floppy disk controller select signal (active low)
57	$\overline{DSKCHG}$	I	Input to disk change signal (active low)
58	$\overline{HID}$	O	(active low)
59	$\overline{IO7A}$	O	7AH I/O port select signal (active low)
60	CSCOMA	O	COMA chip select signal (active high)
61	SIRQ	I	Input to 82C50 interrupt request signal
62	$\overline{SINTEN}$	I	Input to 82C50 interrupt enable signal
63	CSCOMB	O	COMB chip select signal (active high)
64	COM1/$\overline{2}$	I	Input to COM 1, COM 2 select signal from the sub-CPU
65	BUSY	I	Input to printer busy signal
66	$\overline{ACK}$	I	Input to printer acknowledge signal
67	PE	I	Input to printer paper empty signal
68	SELECT	I	Input to printer select signal
69	$\overline{ERROR}$	I	Input to printer error signal
70	SEL	O	Printer select signal
71	INIT	O	Printer initialize signal
72	AUTOFD	O	Printer linefeed enable signal
73	STROBE	O	Printer strobe signal
74	$\overline{PPDL0}$	O	Data output 0 to printer
75	$\overline{PPDL1}$	O	Data output 1 to printer
76	$\overline{PPDL2}$	O	Data output 2 to printer
77	$\overline{PPDL3}$	O	Data output 3 to printer
78	$\overline{PPDL4}$	O	Data output 4 to printer
79	$\overline{PPDL5}$	O	Data output 5 to printer
80	Vcc		+5V supply
81	GND		0V, ground
82	$\overline{PPDL6}$	O	Data output 6 to printer
83	$\overline{PPDL7}$	O	Data output 7 to printer
84	TSTCLK	I	Test clock input
85	S	O	LCD scan start signal
86	CP1	O	LCD data latch signal
87	CP2	O	LCD data shift clock
88	LCDU0	O	Upper row LCD data 0
89	LCDU1	O	Upper row LCD data 1
90	LCDU2	O	Upper row LCD data 2
91	LCDU3	O	Upper row LCD data 3
92	LCDL0	O	Lower row LCD data 0
93	LCDL1	O	Lower row LCD data 1
94	LCDL2	O	Lower row LCD data 2
95	LCDL3	O	Lower row LCD data 3
96	VOSC	I	LCD controller clock input
97	SD0	I/O	System data bus 0
98	SD1	I/O	System data bus 1
99	SD2	I/O	System data bus 2
100	SD3	I/O	System data bus 3
101	SD4	I/O	System data bus 4
102	SD5	I/O	System data bus 5
103	SD6	I/O	System data bus 6
104	SD7	I/O	System data bus 7
105	SA0	I	System address bus 0
106	SA1	I	System address bus 1
107	SA2	I	System address bus 2

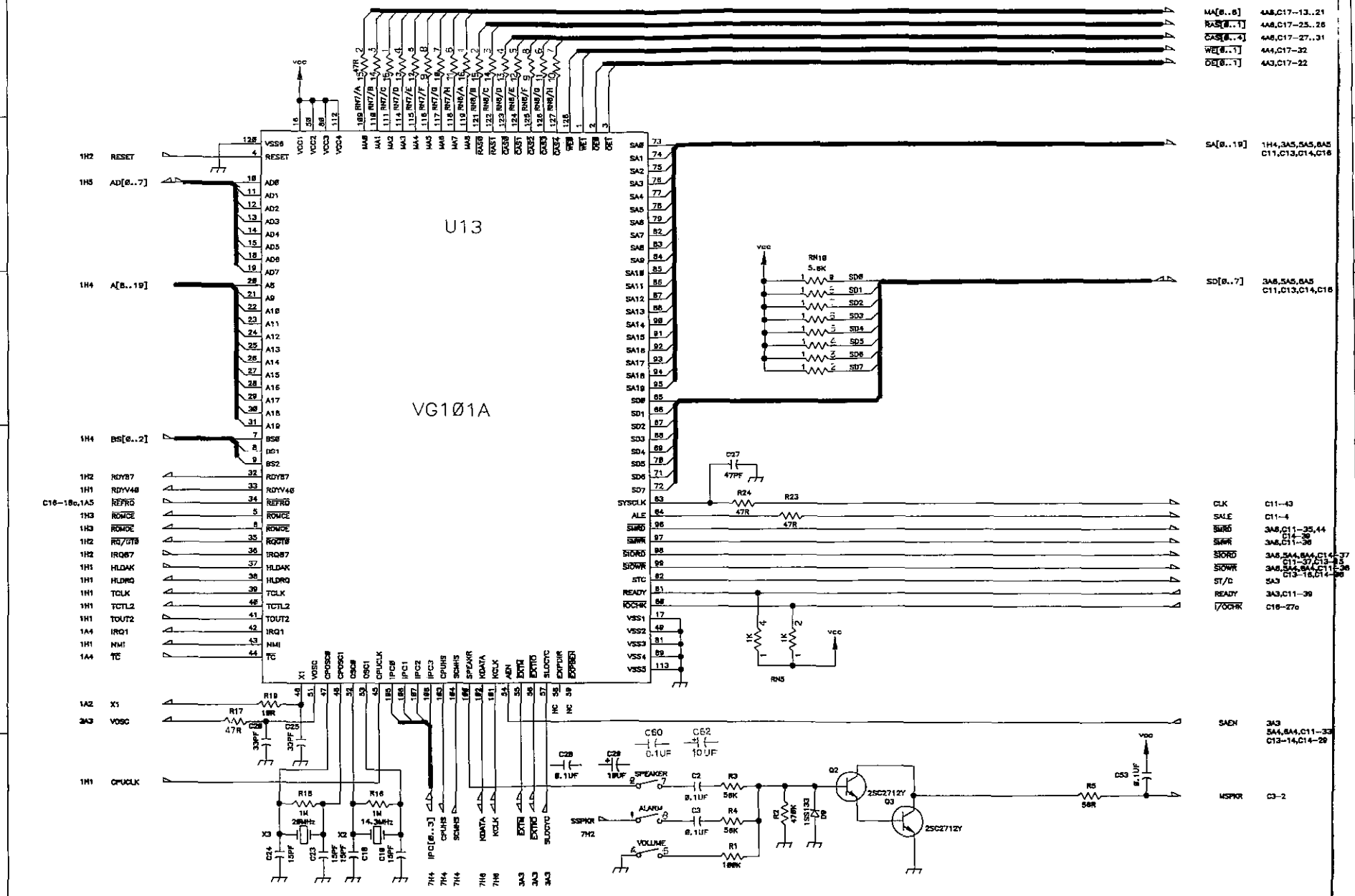
No.	Signal name	I/O	Description
108	SA3	I	System address bus 3
109	SA4	I	System address bus 4
110	SA5	I	System address bus 5
111	SA6	I	System address bus 6
112	Vcc		+5V supply
113	GND		0V, ground
114	SA7	I	System address bus 7
115	SA8	I	System address bus 8
116	SA9	I	System address bus 9
117	SA10	I	System address bus 10
118	SA11	I	System address bus 11
119	SA12	I	System address bus 12
120	SA13	I	System address bus 13
121	SA14	I	System address bus 14
122	SA15	I	System address bus 15
123	SA16	I	System address bus 16
124	SA17	I	System address bus 17
125	SA18	I	System address bus 18
126	SA19	I	System address bus 19
127	AEN	O	DMA refresh active signal
128	$\overline{REFRQ}$	I	Input to refresh request signal from V40

CHAPTER 10. CIRCUIT DIAGRAM & PARTS POSITION

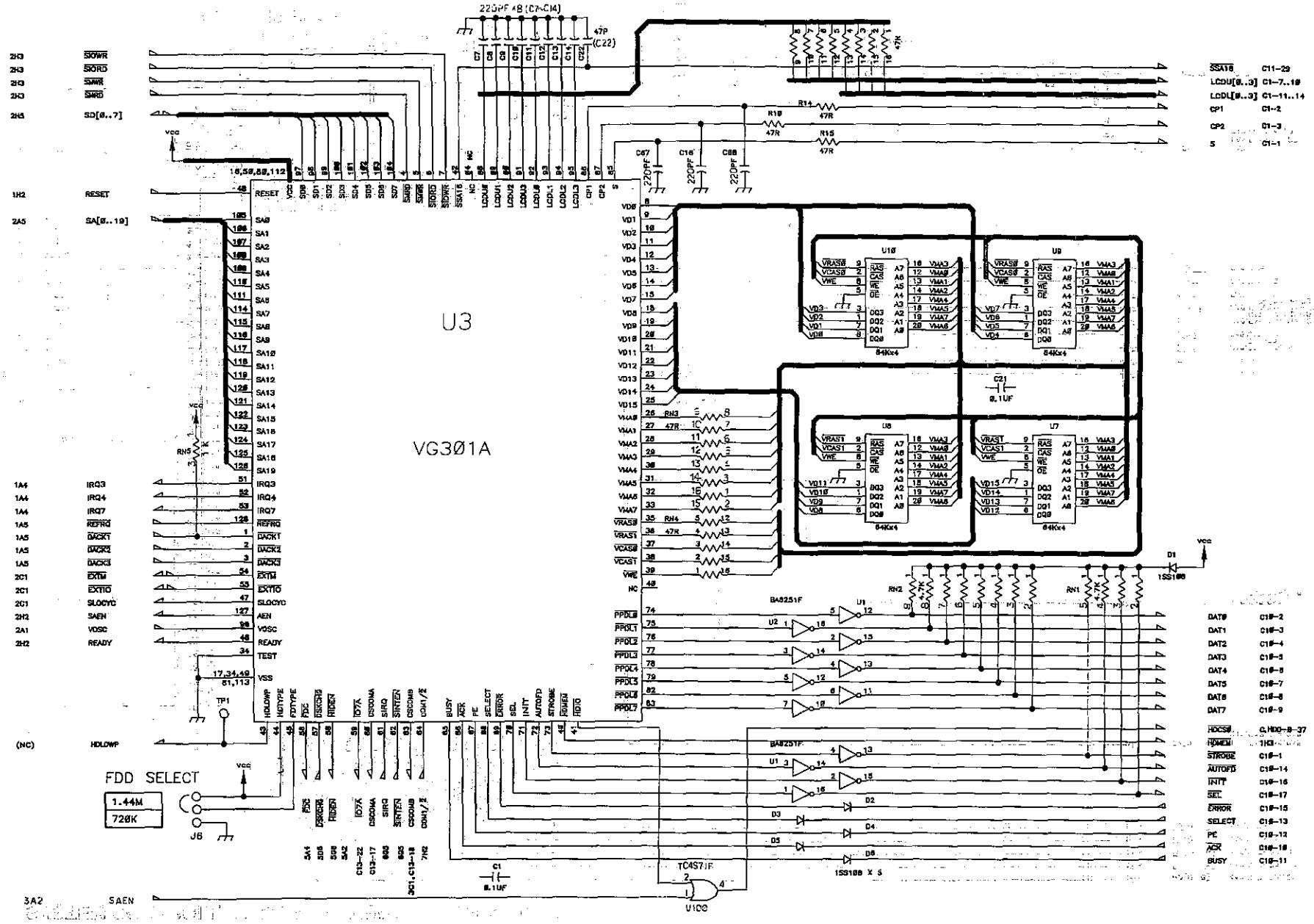
PROCESSOR & ROM



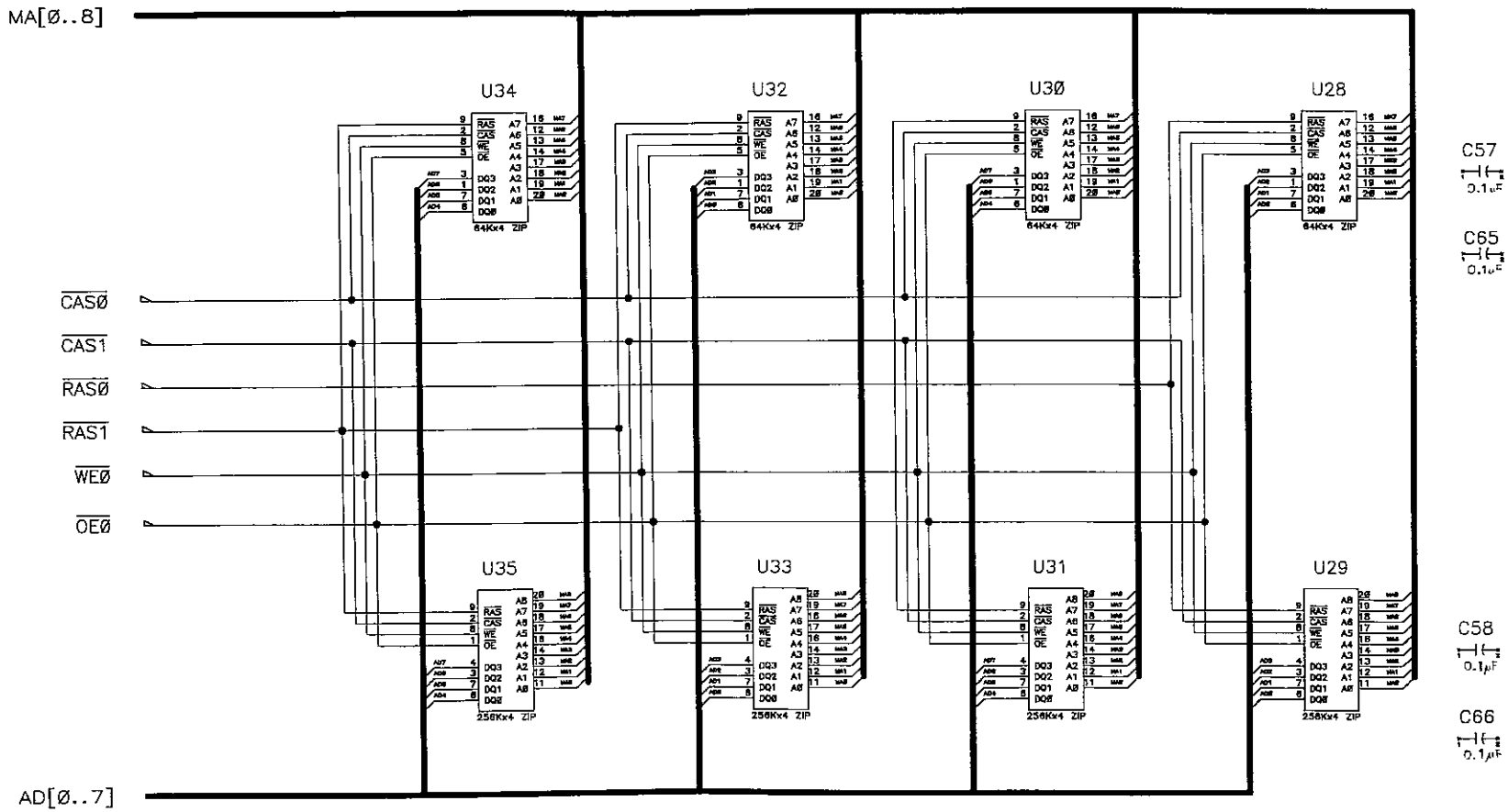
SYSTEM CONTROLLER (BUS I/F, MEMORY I/F, SPEAKER I/F)



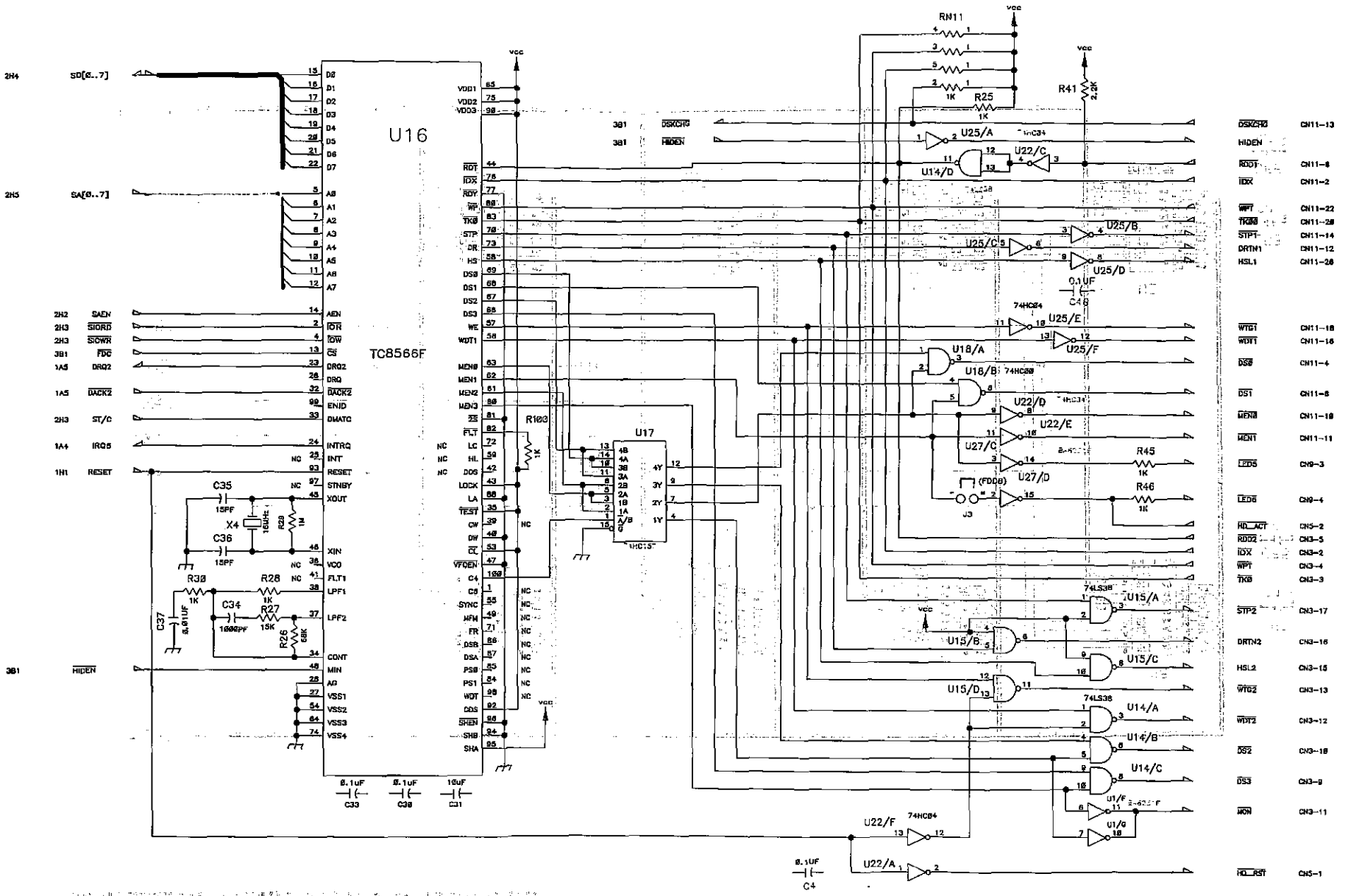
PERIPHERAL/LCD CONTROLLER (LCD, PARALLEL I/F)



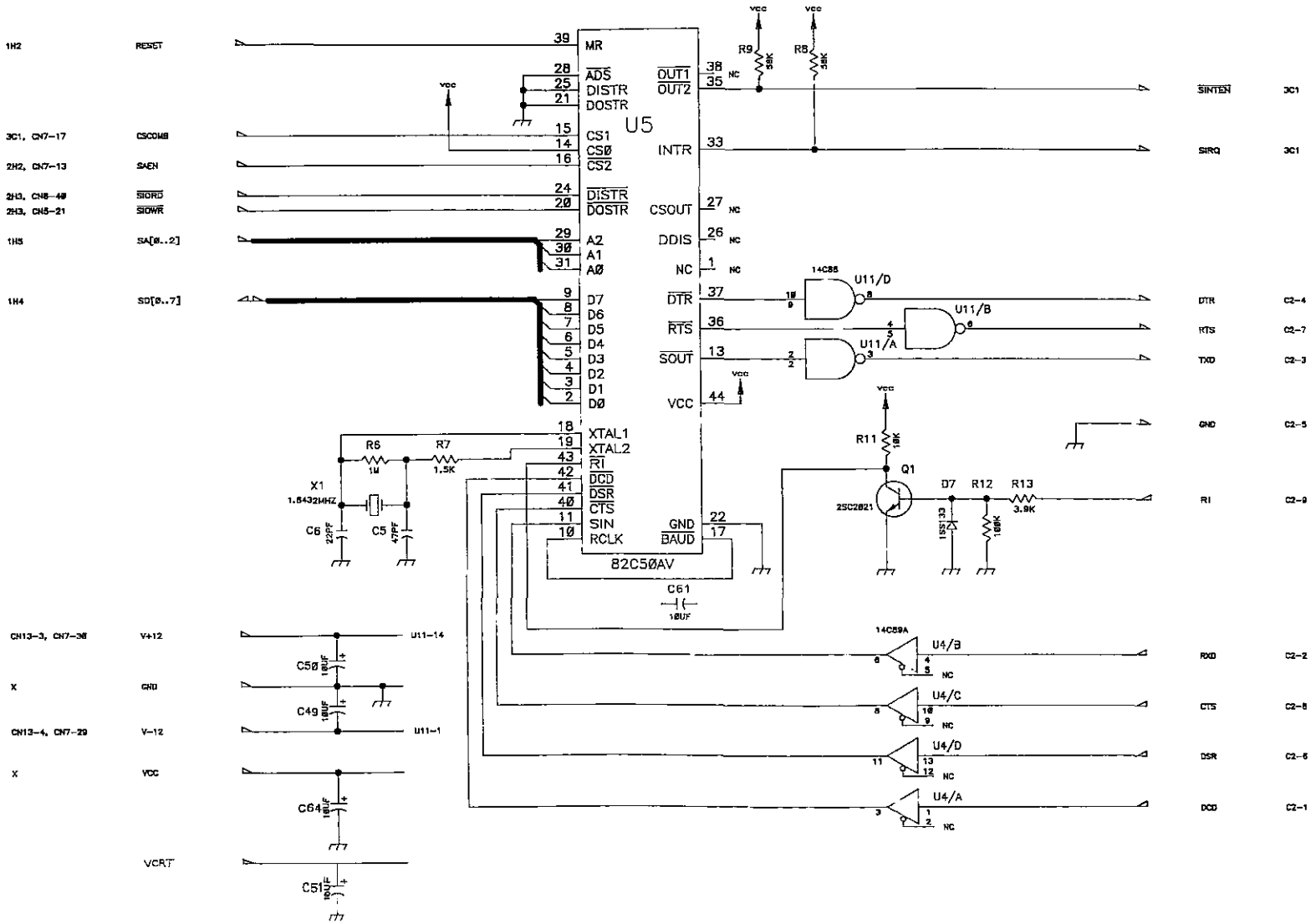
MAIN MEMORY (640K) PCB REV.4 CONFIGURATION



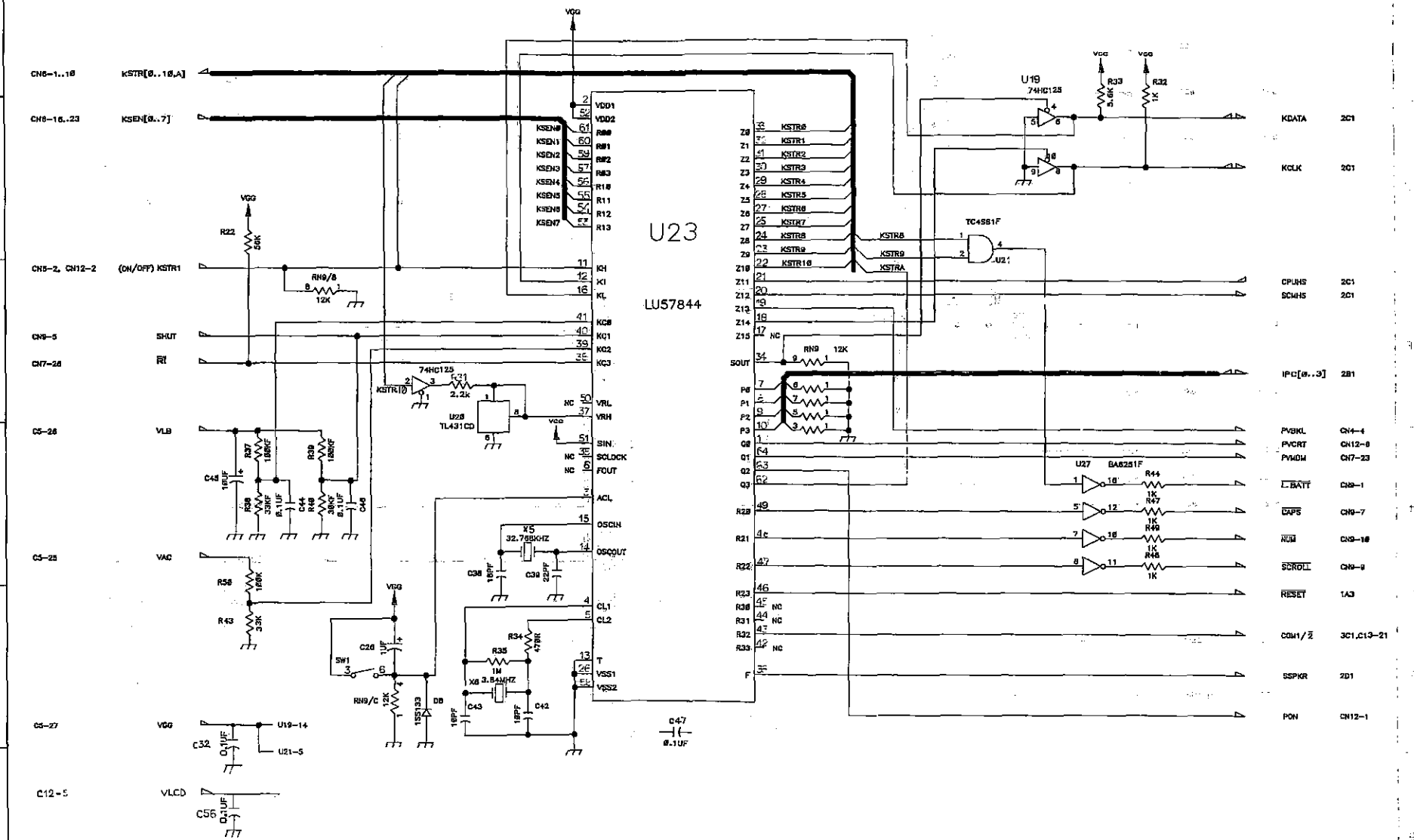
FLOPPY DISK CONTROLLER & I/F



SERIAL I/F


1H2 RESET
3C1, CN7-17 CSCOMB
2H2, CN7-13 SAEN
2H3, CN8-40 SIORD
2H3, CN8-21 SIOWR
1H5 SA[0..2]
1H4 SD[0..7]
U5
82C50AV
MR
ADS
DISTR
DOSTR
CS1
CS0
CS2
INTR
CSOUT
DDIS
NC
D7
D6
D5
D4
D3
D2
D1
D0
VCC
GND
XTAL1
XTAL2
RI
DCD
DSR
CTS
SIN
RCLK
BAUD
OUT1
OUT2
R9
R8
U11/D
U11/B
U11/A
U4/B
U4/C
U4/D
U4/A
Q1
2SC2821
X1
1.8432MHZ
C6
C5
C61
R6
R7
R11
R12
R13
SINTEN 3C1
SIRQ 3C1
DTR C2-4
RTS C2-7
TXD C2-3
GND C2-5
RI C2-9
RXD C2-2
CTS C2-8
DSR C2-6
DCD C2-1
CN13-3, CN7-38 V+12
CN13-4, CN7-29 V-12
VCRT
C50
C49
C64
C51

SUB-CPU (KEYBOARD, SYSTEM POWER, RTC)



CONNECTORS

CN4
LCD

1	S		
2	CP1		
3	CP2		
4	PVEKL		
5	VCC		
6	GND		
7	VLCD		
8	LCDU0		
9	LCDU1		
10	LCDU2		
11	LCDU3		
12	LCDL0		
13	LCDL1		
14	LCDL2		
15	LCDL3		

CN6
KEYBD

KSTR0	1	2	KSTR1
2	3	4	3
4	5	6	5
6	7	8	7
8	9	10	9
10	11	12	(NC)
(NC)	13	14	(NC)
(NC)	15	16	KSEN0
KSEN1	17	18	2
3	19	20	4
5	21	22	6
7	23		

CN11
FDD

VCC	1	2	IDX
VCC	3	4	DSB
VCC	5	6	DSKCHG
VCC	7	8	DS1
VCC	9	10	MDAB
MDNT	11	12	DRTN1
DSKCHG	13	14	STP1
GND	15	16	WDT1
GND	17	18	WTG1
GND	19	20	TKB0
GND	21	22	WPT
GND	23	24	RDD1
GND	25	26	HSL1

C59 ⊣| |⊢ 10UF

CN8
CRT

SD0	1	2	SA1
SD2	3	4	SA3
SD4	5	6	SA5
SD6	7	8	SD7
SA0	9	10	SA1
SA2	11	12	SAEN
SIORD	13	14	SIOWR
GND	15	16	SA3
SA4	17	18	SA5
SA6	19	20	SA7
SA8	21	22	SA9
SA10	23	24	SA11
SA12	25	26	SA13
SA14	27	28	SA15
SSA16	29	30	SA17
SA18	31	32	SA19
SMWR	33	34	SMRD
VDD	35	36	READY
VDD	37	38	CLK
VCRT	39	40	SALE
VCRT	41	42	GND
PVCRT	43	44	GND
VCC	45	46	VCC
BS2	47	48	VCC
RESET	49	50	REFRQ

CN7
MODEM

GND	1	2	GND
SD0	3	4	SD1
SD2	5	6	SD3
SD4	7	8	SD5
SD6	9	10	SD7
SA0	11	12	SA1
SA2	13	14	SAEN
SIORD	15	16	SIOWR
CSCOMA	17	18	CSCOMB
IRQ3	19	20	IRQ4
COM1/2	21	22	307A
(NC)	23	24	PVMDM
RI	25	26	MSPKR
V-5	27	28	RESET
V+12	29	30	V-12
VCC	31	32	VDD
VCC	33	34	VCC

CN3
MFD

(NC)	1	14	(NC)
IDX	2	15	HSL2
TKB0	3	16	DRTN2
WPT	4	17	STP2
RDD2	5	18	GND
(NC)	6	19	GND
(NC)	7	20	GND
(NC)	8	21	GND
DS3	9	22	GND
DS2	10	23	GND
MON	11	24	GND
WDT2	12	25	GND
WTG2	13		

CN9
LED

1	L.BATT
2	GND
3	FDDA
4	FDDB/HD
5	SHUT
6	VCC
7	CAPS
8	SPK
9	SCROLL
10	NUM

CN5
HDD

HD_RST	1	2	GND
SD7	3	4	NC
SD8	5	6	NC
SD5	7	8	NC
SD4	9	10	NC
SD3	11	12	NC
SD2	13	14	NC
SD1	15	16	NC
SD0	17	18	NC
GND	19	20	NC
SAEN	21	22	GND
SIOWR	23	24	GND
SIORD	25	26	GND
DACK3	27	28	NC
DRQ3	29	30	GND
IRQ5	31	32	GND
SA1	33	34	GND
SA0	35	36	GND
HDCS0	37	38	GND
HDACT	39	40	GND
VCC	41	42	MVCC
MGND	43	44	AT/-XT

C63 ⊣| |⊢ 10UF

CN1
PRINTER

STROBE	1	14	AUTOFD
DAT0	2	15	ERROR
DAT1	3	16	INIT
DAT2	4	17	SEL
DAT3	5	18	GND
DAT4	6	19	GND
DAT5	7	20	GND
DAT6	8	21	GND
DAT7	9	22	GND
ACK	10	23	GND
BUSY	11	24	GND
PE	12	25	GND
SELECT	13		

CN12
PS1

VCC	1
VCC	2
V+12	3
V-12	4
VLCD	5
VCRT	6
GND	7
GND	8

CN13
PS2

1	PON
2	KSTR1
3	KSTR0
4	VAC
5	VDD
6	PVCRT
7	VLB
8	GND
9	V-5
10	GND

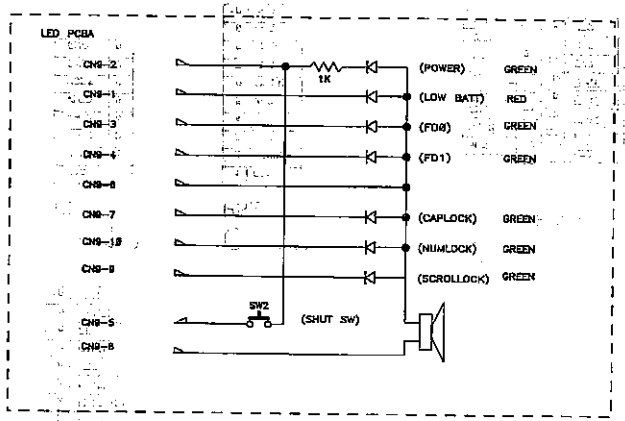
CN10
EMS MEMORY

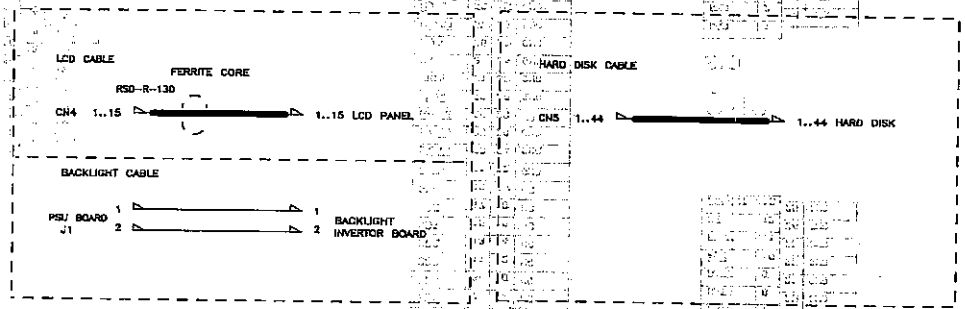
WE1	33	31	AD2	OE1	34	32	AD6
AD0	29	27	AD4	AD7	30	28	AD3
CAS2	25	23	CAS4	AD1	26	24	AD5
GND	21	19	CAS1	CAS3	22	20	CAS0
GND	17	15	RAS1	RAS0	18	16	MA8
MA1	13	11	GND	MA3	14	12	MA2
VCC	9	7	MA9	MA4	10	8	MA5
VCC	5	3	VCC	MA7	6	4	GND
VCC	1			MA6	2		

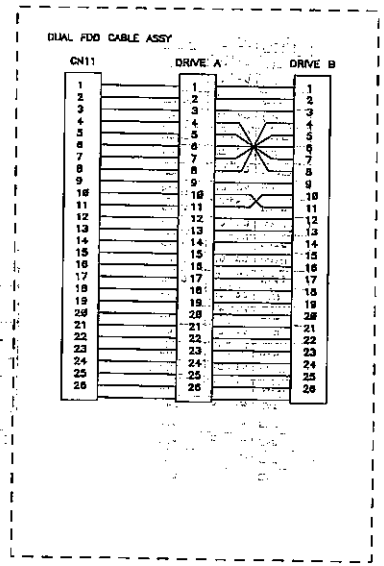
CN2
SIO

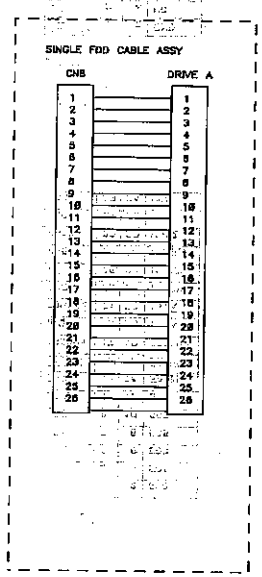
DCD	1	6	DSR
RXD	2	7	RTS
TXD	3	8	CTS
DTR	4	9	RI
GND	5		

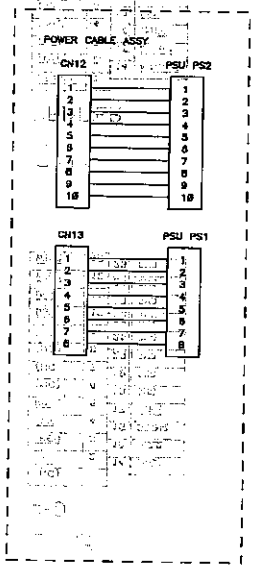
SUB ASSEMBLIES





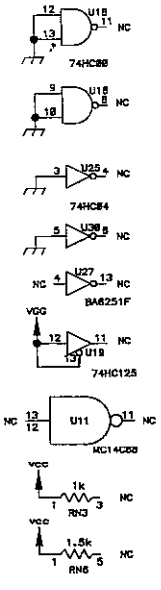






SERIAL I/F

SPARE GATES



DESIGNATORS	
LAST USE	NOT USED
C60	
U35	
X6	
D9	
J3	
R49	
RN13	
Q3	

RAM CHIPS LOCATOR FOR REV.3 PCB			
START	LAST ADDRESS	BIT 7–4	BIT 3–0
000K	00FFFF	U5	U15
64K	01FFFF	U21	U19
128K	02FFFF	U4	U14
192K	03FFFF	U20	U9
256K	04FFFF	U3	U13
320K	05FFFF	U19	U8
384K	06FFFF	U2	U12
448K	07FFFF	U18	U7
512K	08FFFF	U1	U11
576K	09FFFF	U17	U6

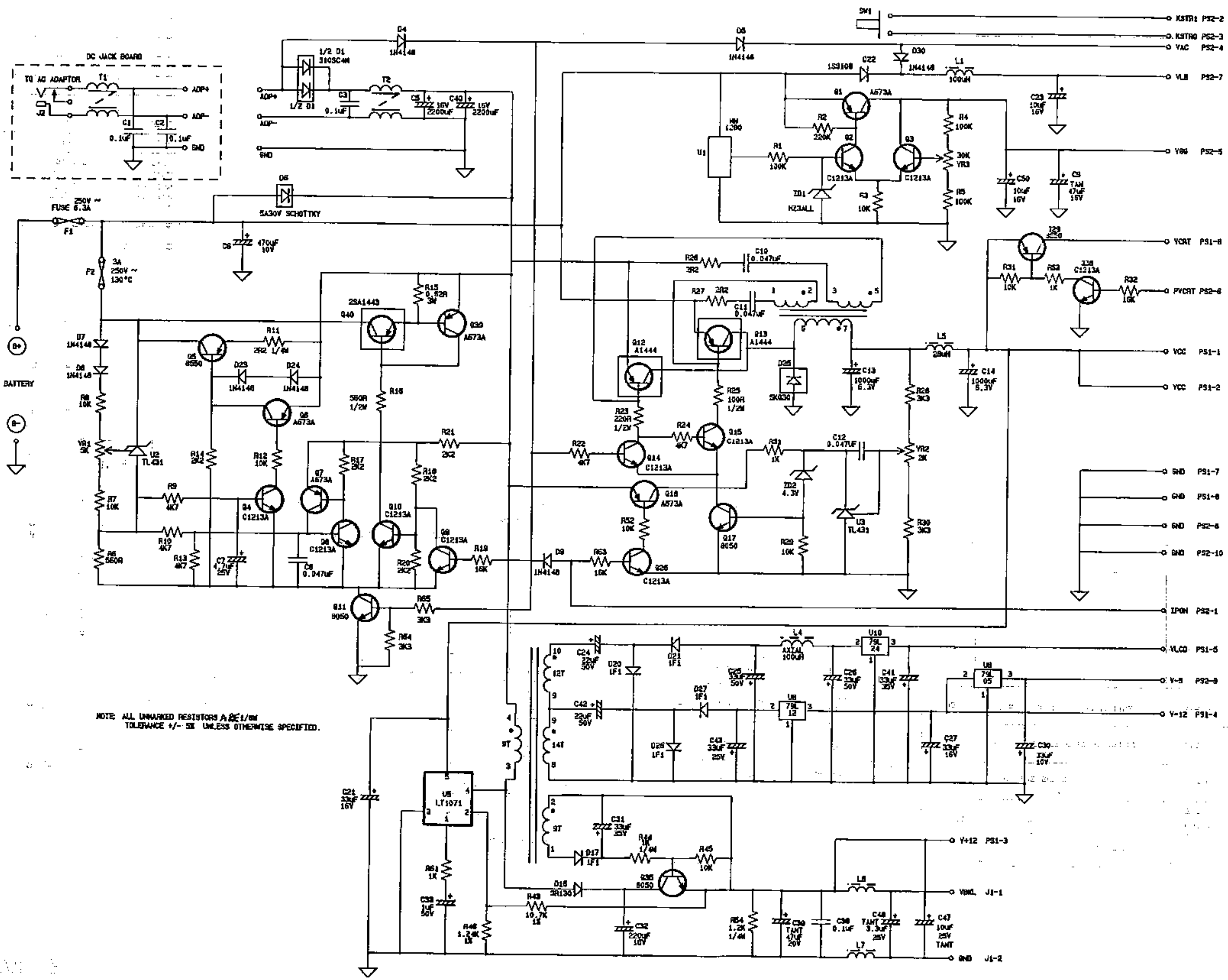
DIP SWITCH		
SW1	ON	OFF
1	NORMAL	LOW BATT/SHUT ALARM OFF
2	NORMAL	PC SPEAKER OFF
3	RESET SUB-CPU	NORMAL OPERATION
4	SPEAKER LOW VOLUME	NORMAL

JUMPER			
LOCATION	FUNCTION	NORMAL SETTING	SPECIAL SETTING
J1	FDD TYPE SELECT	1.44M	(CUT & JMP) 720K
J2	FDD WRITE PRE-COMP PERIOD(720K)	250nS	(CUT & JMP) 125NS
J3	SELECT LED INDICATOR SOURCE	FDD-B	(JUMP) HDD

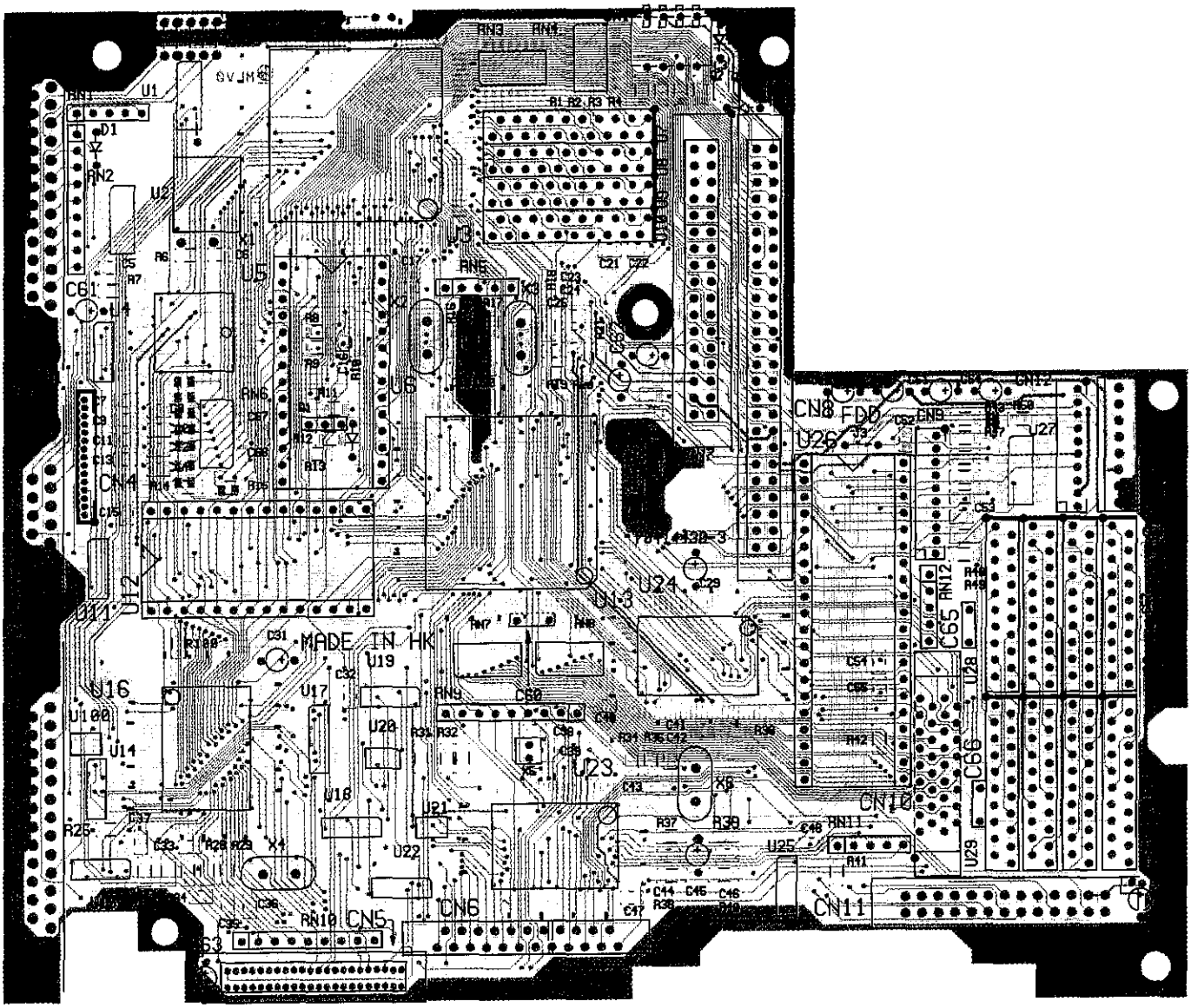
DUAL FDD PCBA VS SINGLE FDD/HDD PCBA		
ITEM	DUAL FDD VERSION	HDD/FDD VERSION
R39	97.6KF	196KF
J3	INSTALL	NIL
CN5	NIL	INSTALL

ECN FOR REV2 PCB

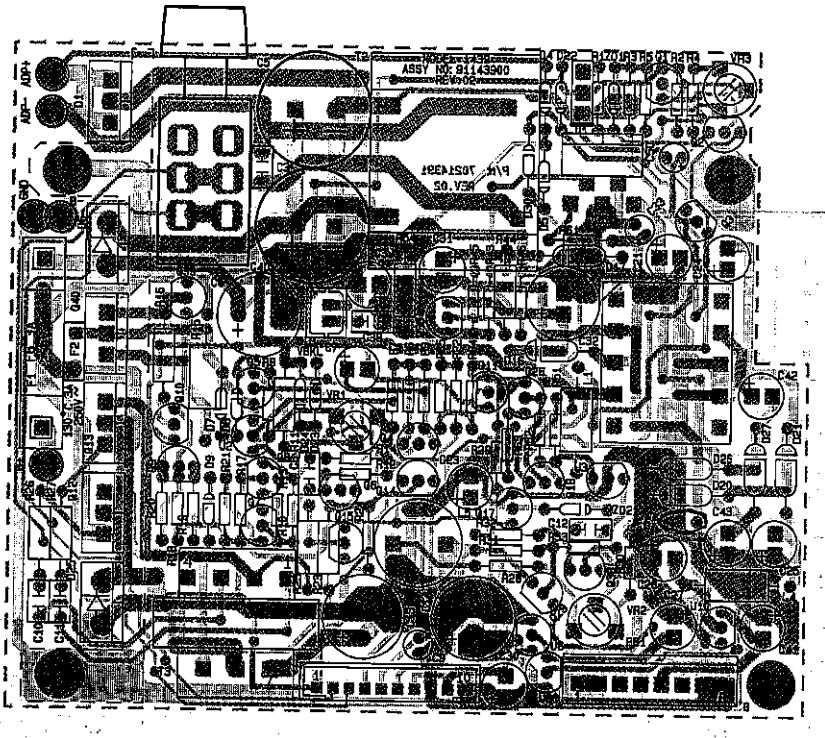
P.S UNIT


DC JACK BOARD
TO AC ADAPTOR
ADP+
ADP-
GND
FUSE 6.3A
250V ~
BATTERY
1N4148
5A30V SCHOTTKY
310SC4M
2SA1443
A673A
C1213A
8550
8050
A1444
TL431
LT1071
HZ3ALL
1SS108
SK030
79L 24
79L 12
79L 05
KSTR1 PS2-2
KSTRO PS2-3
VAC PS2-4
VLB PS2-7
VBB PS2-5
VCRT PS1-8
PVCRT PS2-6
VCC PS1-1
VCC PS1-2
GND PS1-7
GND PS1-6
GND PS2-8
GND PS2-10
IPON PS2-1
VLCD PS1-5
V-5 PS2-9
V-12 PS1-4
V+12 PS1-3
VBKL J1-1
GND J1-2
NOTE: ALL UNMARKED RESISTORS ARE 1/8W
TOLERANCE +/- 5% UNLESS OTHERWISE SPECIFIED.

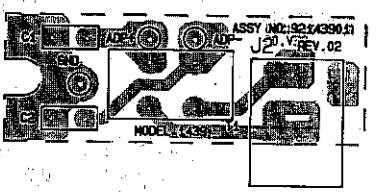
MAIN PWB



POWER CIRCUIT PARTS LAYOUT



LED PWB



DC JACK BOARD

MEMO

SHARP