Technical Information Manual

S30H-1721-00

PC 330/350 Pentium (75/90/100 MHz)
PC 330/350 Pentium (120/133/150/166 MHz)
PC 360 Pentium Pro

Technical Information Manual

S30H-1721-00

PC 330/350 Pentium (75/90/100 MHz)
PC 330/350 Pentium (120/133/150/166 MHz)
PC 360 Pentium Pro

Note

Before using this information and the product it supports, be sure to read the general information under Appendix B, “Notices” on page 70.

First Edition (February 1996)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

This publication could include technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or the program(s) described in this publication at any time.

It is possible that this publication may contain reference to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country.

Requests for technical information about IBM products should be made to your IBM reseller or IBM marketing representative.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to:

IBM Director of Licensing
IBM Corporation
500 Columbus Avenue
Thornwood, NY 10594
U.S.A.

© **Copyright International Business Machines Corporation Februray 1996. All rights reserved.**
Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Contents

© Copyright IBM Corp. Februray 1996

Figures

© Copyright IBM Corp. Februray 1996

Tables

© Copyright IBM Corp. Februray 1996

Preface

This *Technical Information Manual* provides system-specific hardware and software information for the IBM personal computer (IBM 300 Series). Specifically, this manual describes the IBM PC 330/350—Pentium (75/90/100 MHz), the IBM PC 330/350—Pentium (120/133/150/166 MHz), and the IBM PC 360—Pentium Pro. It is intended for individuals who have questions about the technical aspects of IBM Personal Computers. It is also intended for developers who want to provide hardware and software products to operate with these IBM systems. In general, this manual is for anyone who wants a more in-depth view of how IBM Personal Computers work. Users of this publication should have a basic understanding of computer architecture and programming concepts.

Organization

This manual describes the IBM PC 330/350—Pentium (75/90/100 MHz), the IBM PC 330/350—Pentium (120/133/150/166 MHz), and the IBM PC 360—Pentium Pro personal computers. It provides a system level overview and a detailed description of the subsystems that comprise IBM personal computers.

This manual is set up in the following manner:

- **Chapter 1. System Description**

  This chapter describes the IBM 300 Series: features, devices, and specifications.

- **Chapter 2. Connectors and Jumpers**

  This chapter describes the connectors and jumpers found on the system board and risers. It provides connector and pin assignments and jumper descriptions.

- **Chapter 3. Memory Subsystems**

  This chapter describes the different types of memory used.

- **Chapter 4. System Compatibility**

  This chapter describes the compatibility issues.

- **Chapter 5. Direct Memory Access Controller**

  This chapter describes the direct memory access (DMA) controller.

- **Chapter 6. Interrupt Controller**

  This chapter describes the interrupt controller.

- **Chapter 7. System Timers**

  This chapter describes the system timers.

- **Chapter 8. Bus Architecture**

  This chapter describes the ISA and PCI I/O channel architectures.

- **Appendix A. Error Codes**
- **Appendix B. IBM personal computer System Features**
- **Appendix C. Notices**

© Copyright IBM Corp. Februray 1996

Related Publications

This *Technical Information Manual* can be used with the following publications. These publications contain additional information about many of the subjects that are discussed in this manual and also provide additional information that is not included in this manual.

- *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*
- *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces*
- *IBM Personal System/2 ATA/IDE Fixed Disk Drives Technical Reference*
- *IBM Personal System/2 Hardware Interface Technical Reference—Architectures, (update—order number S10G-6466)*
- *S3 Trio64*, published by S3 Incorporated, Santa Clara, CA
- *Intel Microprocessor and Peripheral Component Literature*, published by Intel Corporation, Santa Clara, CA
- *82420/82430 PCISet ISA and EISA Bridges*, part number 290483-001 published by Intel Corporation, Santa Clara, CA
- *82430 PCISet Cache/Memory Subsystem*, part number 290482-001 published by Intel Corporation, Santa Clara, CA
- *PCI Local Bus Specification - Revision 2.0*, dated April 30, 1993, published by the PCI Special Interest Group, Hillsboro, OR
- *Extended Capabilities Port: Specification Kit - Revision 1.06*, dated July 14, 1993, published by Microsoft Corporation, Redmond, WA
- *ANSI ATA-2 (AT Attachment), Rev. 2j*, dated 2 December 1994

Manual Style

Warning: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

Signals

In this manual, signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

Numerics

In this manual, use of the letter “h” indicates a hexadecimal number. Also when numerical modifiers such as “K”, “M” and “G“ are used, they typically indicate powers of 2, not powers of 10 (unless expressing hard disk storage capacity). For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes(2^{20}), and 1 GB equals 1 073 741 824 bytes(2^{30}).

When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: The actual storage capacity available to the user can vary, depending on the operating system and other system requirements.

Chapter 1. System Description

© Copyright IBM Corp. Februray 1996

Personal Computer Description

Your IBM personal computer (PC) is a versatile product designed to give you state-of-the-art computing power with room for growth in the future. Many model variations are available for the personal computer family. The following components are used to differentiate the models that are available:

- Pentium and Pentium Pro microprocessors
- OverDrive microprocessor upgrades
- System unit packaging
- Local-bus architecture
- Video-bus architecture
- ISA/PCI I/O-bus compatibility
- ISA/PCI expansion slots
- Video and storage devices
- Enhanced IDE drives
- Memory upgrades
- External cache upgrades
- Video memory upgrades
- Advanced power management
- Enhanced security features
- PCMCIA support (requires optional adapter card in ISA slot)
- SCSI support (requires optional adapter card in PCI slot)

These features, as well as many of the others the personal computer offers, are described in more detail in the following chapters. Not all of the features are offered on all models.

The models in the IBM 300 Series are designated by expansion capability and microprocessor.

- The PC 330 has three expansion slots and three drive bays
- The PC 350 has five expansion slots and five drive bays.
- The PC 360 has six expansion slots and five drive bays.

Type Number and Model Number Conversion

This section provides an explanation of the personal computer *Type and Model numbers*. These numbers identify the features of the system.

Interrupt 15h, the *Return System Configuration Parameters function*; ((AH)=C0h) returns the model byte, submodel byte, BIOS revision code, and other configuration information. The model byte for the personal computer family is FCh, and the submodel byte is 01h.

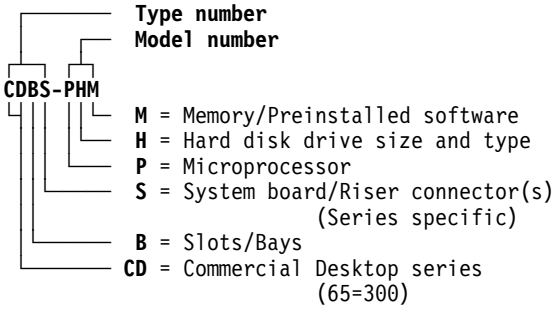
The Type Number contains the following information:

- personal computer Series identification (300 Series)
- Number of slots and bays
- Type of system board/riser connector(s) (Series specific)

The Model Number contains the following information:

- Microprocessor Type
- Hard disk drive size and type
- Amount of memory installed and preinstalled software information

The following figure shows the position of each digit of the type number and model number, and description of each position.



As an example, if the machine type number and model number are **6575—33G**, each digit decodes as follows:

Digits	Information
65	PC 300 Series system
7	System has 3 slots and 3 bays
5	Pentium-5V with ISA/PCI
3	P54C-75 MHz
3	270MB IDE hard disk drive installed
G	Shipped with 8MB of memory and preinstalled with OS/2

The codes and descriptions for type and model numbers, are in the following tables.

Note: Certain models will not be offered in all geographic locations. This information is subject to change.

CD—personal computer Series Codes

CD	personal computer Series
65	300

B—Slot/Bay Codes

B	Slots and Bays
7	3 slots and 3 bays
8	5 slots and 5 bays
9	6 slots and 6 bays

S—System Board/Riser Connector(s) (PC 300 Series Only)

S	System Board/Riser Connector(s)
6	Pentium 75-166 with ISA/PCI
8	Pentium Pro with ISA/PCI

P—Microprocessor

P	Microprocessor
1	Pentium 100 MHz, without L2 cache
2	Pentium 75 MHz, without L2 cache
3	Pentium 75 MHz
4	Pentium 90 MHz
5	Pentium 100 MHz
6	Pentium 120 MHz
7	Pentium 133 MHz
8	Pentium 150 MHz
9	Pentium 166 MHz
C	Pentium Pro 150
E	Reserved
F	Reserved
G	Reserved

H—Hard Disk Drive Size and Type

H	Hard Disk Drive Size and Type
0	No hard disk drive
2	170MB IDE
3	270MB IDE
4	364MB IDE
5	540MB IDE
6	635MB IDE
7	850MB IDE
8	1GB IDE
9	1.2GB IDE
A	1.7GB IDE
B	Reserved
C	540MB SCSI
D	850MB SCSI
E	1GB SCSI
F	2GB SCSI with 6X CDROM
N	270MB with Multimedia
P	364MB with Multimedia
R	540MB with Multimedia
S	850MB with CDROM
T	1GB with CDROM
U	Universal
V	Base model built to order
W	Special Bid
X	1.2GB IDE with CDROM
Y	635MB IDE with CDROM
Z	1.7GB IDE with CDROM

M—Memory and Preinstalled Software

M	Memory and Preinstalled Software (PC 300 Series, U.S. Only)
A	8MB with DOS and Microsoft Windows
B	4MB with DOS and Microsoft Windows
D	4MB with no preinstalled software
E	8MB with no preinstalled software
F	8MB with SelectaSystem
G	8MB with OS/2 WARP
H	16MB with SelectaSystem
J	16MB with OS/2 Warp
K	32MB with OS/2 Warp
L	Reserved
S	8MB with Windows 95
T	16MB with Windows 95
U	16MB with no preinstalled software
V	Reserved
W	Reserved
X	32MB with no preinstalled software

System Board Devices and Features

There are two different system boards for the PC 330/350—Pentium personal computers. and only one system board for the PC 360—Pentium Pro personal computers. The following tables list the devices and features for each system board type in the personal computer family. Additional information about each device can be found either in this manual or in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces*.

PC 330/350—Pentium (75/90/100 MHz)

The following table lists the devices and features for the PC 330/350—Pentium (75/90/100 MHz) system board.

Table 1 (Page 1 of 2). System Board Devices and Features PC 330/350—Pentium (75/90/100 MHz)

Device	Features
Microprocessor	• Intel Pentium—75/90/100 MHz – 32-bit address bus, 64-bit data bus – 16KB internal L1 cache – 256KB write-through L2 cache (optional) – Superscalar architecture (two execution units) – Math coprocessor function included in the Pentium • Microprocessor is upgradable for future Intel processor technology
Video Subsystem	• S3 Trio864 video controller – High performance, 64-bit, SVGA PCI local-bus video – Analog output – 1MB video dynamic random access memory (DRAM) upgradable to 2MB • 64-bit graphics accelerator
Bus Architecture	• ISA/PCI bus-compatible I/O expansion slots
Flash ROM Subsystem	• 256KB flash ROM for POST/BIOS
RAM Subsystem	• 8MB to 128MB
CMOS RAM Subsystem	128-byte CMOS RAM with real-time clock, calendar, and battery
DMA Controller	• Seven AT-compatible DMA channels – Four 8-bit channels – Three 16-bit channels
Interrupt Controller	• 15 levels of system interrupts • AT-bus interrupts are edge triggered • PCI bus interrupts are level sensitive
System Timers	• Channel 0—System timer • Channel 1—Refresh generation • Channel 2—Tone generation for speaker
Audio Subsystem	• Driven by system-timer channel 2 • On-board piezo-electric beeper
Diskette Drive Controller	• Supports – 3.5-in. diskette drive (1.44MB and 2.88MB) – 5.25-in. diskette drive (360KB and 1.2MB) – FIFO operations
Keyboard/Auxiliary-Device Controller	• Keyboard connector • Auxiliary-device connector • Password security
Parallel Port Controller	• Supports bidirectional input and output, extended capabilities port (ECP) mode, and enhanced parallel port (EPP) mode
Serial Port Controller	• Two RS-232D interface—16550A compatible • Programmable as serial port 1–4

Table 1 (Page 2 of 2). System Board Devices and Features PC 330/350—Pentium (75/90/100 MHz)	
Device	**Features**
Hard Disk Drive Connector	• PC 330 supports up to two internal drives • PC 350 supports up to four internal drives
Operating System Support	• IBM PC DOS • IBM OS/2 • MS-DOS • DOS with Microsoft Windows. • DOS with Windows for Work Groups • Microsoft Windows NT • Novell NetWare • Novell UnixWare • SCO UNIX • Solaris • Microport System V/4 • DEC PathWorks

PC 330/350—Pentium (120/133/150/166 MHz)

The following table lists the devices and features for the PC 330/350—Pentium (120/133/150/166 MHz) system board.

Table 2 (Page 1 of 2). System Board Devices and Features PC 330/350—Pentium (120/133/150/166 MHz)	
Device	**Features**
Microprocessor	• Intel Pentium—120/133/150/166 MHz – 32-bit address bus, 64-bit data bus – 16KB L1 internal cache – 256KB write-back synchronous L2 cache – Superscalar architecture (two execution units) – Math coprocessor function included in the Pentium • Microprocessor is upgradable for future Intel processor technology
Video Subsystem	• S3 Trio864 video controller – High performance, 64-bit, SVGA PCI local-bus video – Analog output – 1MB video dynamic random access memory (DRAM) upgradable to 2MB • 64-bit graphics accelerator
Bus Architecture	• ISA/PCI bus-compatible I/O expansion slots
Flash ROM Subsystem	• 256KB flash ROM for POST/BIOS
RAM Subsystem	• 8MB to 128MB
CMOS RAM Subsystem	128-byte CMOS RAM with real-time clock, calendar, and battery
DMA Controller	• Seven AT-compatible DMA channels – Four 8-bit channels – Three 16-bit channels
Interrupt Controller	• 15 levels of system interrupts • AT-bus interrupts are edge triggered • PCI bus interrupts are level sensitive
System Timers	• Channel 0—System timer • Channel 1—Refresh generation • Channel 2—Tone generation for speaker
Audio Subsystem	• Driven by system-timer channel 2 • On-board piezo-electric beeper
Diskette Drive Controller	• Supports – 3.5-in. diskette drive (1.44MB and 2.88MB) – 5.25-in. diskette drive (360KB and 1.2MB) – FIFO operations

Table 2 (Page 2 of 2). System Board Devices and Features PC 330/350—Pentium (120/133/150/166 MHz)	
Device	**Features**
Keyboard/Auxiliary-Device Controller	• Keyboard connector • Auxiliary-device connector • Password security
Parallel Port Controller	• Supports bidirectional input and output, extended capabilities port (ECP) mode, and enhanced parallel port (EPP) mode
Serial Port Controller	• Two RS-232D interface—16550A compatible • Programmable as serial port 1–4
Hard Disk Drive Connector	• PC 330 supports up to two internal drives • PC 350 supports up to four internal drives
Operating System Support	• IBM PC DOS • IBM OS/2 • MS-DOS • DOS with Microsoft Windows. • DOS with Windows for Work Groups • Microsoft Windows NT • Novell NetWare • Novell UnixWare • SCO UNIX • Solaris • Microport System V/4 • DEC PathWorks

PC 360—Pentium Pro

The following table lists the devices and features for the PC 360—Pentium Pro system board.

Table 3 (Page 1 of 2). System Board Devices and Features PC 360—Pentium Pro	
Device	**Features**
Microprocessor	• Intel Pentium Pro—150 MHz – 32-bit address bus, 64-bit data bus – 16KB internal L1 cache – 256KB internal L2 cache – Superscalar architecture (two execution units) – Math coprocessor function included in the Pentium • Microprocessor is upgradable for future Intel processor technology
Video Subsystem	• Matrox Millenium PCI video card • 4MB video dynamic random access memory (DRAM) • 64-bit graphics accelerator
Bus Architecture	• ISA/PCI bus-compatible I/O expansion slots
Flash ROM Subsystem	• 256KB flash ROM for POST/BIOS
RAM Subsystem	• 16MB to 128MB • Interleave capable
CMOS RAM Subsystem	128-byte CMOS RAM with real-time clock, calendar, and battery
DMA Controller	• Seven AT-compatible DMA channels – Four 8-bit channels – Three 16-bit channels
Interrupt Controller	• 15 levels of system interrupts • AT-bus interrupts are edge triggered • PCI bus interrupts are level sensitive
System Timers	• Channel 0—System timer • Channel 1—Refresh generation • Channel 2—Tone generation for speaker

Table 3 (Page 2 of 2). System Board Devices and Features PC 360—Pentium Pro	
Device	**Features**
Audio Subsystem	• Driven by system-timer channel 2 • On-board piezo-electric beeper
Diskette Drive Controller	• Supports – 3.5-in. diskette drive (1.44MB and 2.88MB) – 5.25-in. diskette drive (360KB and 1.2MB) – FIFO operations
Keyboard/Auxiliary-Device Controller	• Keyboard connector • Auxiliary-device connector • Password security
Parallel Port Controller	• Supports bidirectional input and output, extended capabilities port (ECP) mode, and enhanced parallel port (EPP) mode
Serial Port Controller	• Two RS-232D interface—16550A compatible • Programmable as serial port 1–4
Hard Disk Drive Connector	• PC 360 supports up to four internal drives
Operating System Support	• IBM PC DOS • IBM OS/2 • MS-DOS • DOS with Microsoft Windows • DOS with Windows for Work Groups • Microsoft Windows 95 • Microsoft Windows NT • Novell NetWare • Novell UnixWare • SCO Open Server • Solaris • DEC PathWorks

System Board I/O Address Map

The following tables list the system board I/O address maps for the IBM 300 Series personal computer family. Any addresses that are not shown are reserved.

PC 330/350—Pentium

The following table shows the system board I/O address map for PC 330/350—Pentium system boards.

Table 4. System Board I/O Address Map PC 330/350—Pentium

Address (Hex)	Device
0000–000F	PIIX–DMA 1
0020–0021	PIIX–Interrupt controller 1
002E–002F	Ultra I/O configuration registers
0040–0043	PIIX–Timer 1
0048–004B	PIIX–Timer 2
0060	Keyboard controller data byte
0061	PIIX–NMI, speaker control
0064	Keyboard controller, CMD/STAT byte
0070, bit 7	PIIX–Enable NMI
0070, bits 6:0	PIIX–Real time clock, address
0071	PIIX–Real time clock, data
0078–0079	Reserved–board configuration
0080–008F	PIIX–DMA page register
00A0–00A1	PIIX–Interrupt controller 2
00C0–00DE	PIIX–DMA 2
00F0	Reset numeric error
0170–0177	Secondary IDE channel
01F0–01F7	Primary IDE channel
0278–027B	Parallel port 2
02F8–02FF	On-board serial port 2
0376	Secondary IDE channel command port
0377	Secondary IDE channel status port
0378–037F	Parallel port 1
03B4–03B5	Trio/64
03BA	Trio/64
03BC–03BF	Parallel Port 3
03C0–03CA	Trio/64
03CC	Trio/64
03CE–03CF	Trio/64
03D4–03D5	Trio/64
03DA	Trio/64
03E8–03EF	Serial port 3
03F0–03F5	Diskette channel 1
03F6	Primary IDE channel command port
03F7 (Write)	Diskette drive channel 1 command
03F7, bit 7	Diskette change channel 1
03F7, bits 6:0	Primary IDE channel status port
03F8–03FF	On-board serial port 1
LPT + 400h	ECP port
04D0–04D1	Edge/level INTR control
0CF8	PCI configuration address register
0CF9	Turbo and reset control register
0CFC–0CFF	PCI configuration data registers
FF00–FF07	IDE Bus Master register
FFA0–FFA7	IDE primary channel
FFA8–FFAF	IDE secondary channel

PC 360—Pentium Pro

The following table shows the system board I/O address map for PC 360—Pentium Pro system board.

Table 5. System Board I/O Address Map PC 360—Pentium Pro

Address (Hex)	Device
0000–000F	PIIX–DMA 1
0020–0021	PIIX–Interrupt controller 1
002E–002F	Ultra I/O configuration registers
0040–0043	PIIX–Timer 1
0048–004B	PIIX–Timer 2
0060	Keyboard controller data byte
0061	PIIX–NMI, speaker control
0064	Keyboard controller, CMD/STAT byte
0070, bit 7	PIIX–Enable NMI
0070, bits 6:0	PIIX–Real time clock, address
0071	PIIX–Real time clock, data
0078–0079	Reserved–board configuration
0080–008F	PIIX–DMA page register
00A0–00A1	PIIX–Interrupt controller 2
00C0–00DE	PIIX–DMA 2
00F0	Reset numeric error
0170–0177	Secondary IDE channel
01F0–01F7	Primary IDE channel
0278–027B	Parallel port 2
02F8–02FF	On-board serial port 2
0376	Secondary IDE channel command port
0377	Secondary IDE channel status port
0378–037F	Parallel port 1
03BC–03BF	Parallel Port x
03E8–03EF	Serial port 3
03F0–03F5	Diskette drive channel 1
03F6	Primary IDE channel command port
03F7 (Write)	Diskette drive channel 1 command
03F7, bit 7	Diskette change channel 1
03F7, bits 6:0	Primary IDE channel status port
03F8–03FF	On-board serial port 1
LPT + 400h	ECP port
04D0–04D1	Edge/level INTR control
0CF8	PCI configuration address register
0CF9	Turbo and reset control register
0CFC–0CFF	PCI configuration data registers

Video Subsystems

IBM 300 Series personal computers use the super video graphics array (SVGA) video subsystem. It is a high-performance graphics subsystem that operates in CGA, EGA, VGA, or SVGA modes. IBM 300 Series personal computers use two different SVGA graphics controllers. These graphics controller are the:

- S3 Trio64 (used in PC 330/350—Pentium (75/91/100 MHz) and PC 330/350—Pentium (120/133/150/166) systems.
- Matrox Millennium PCI Graphics Adapter (used in PC 360—Pentium Pro (150 MHz) systems. The Matrox Graphics adapter card is preinstalled in PCI slot 4.

Microprocessors

The following microprocessors are used in IBM personal computers. See Intel's microprocessor literature for more information.

Pentium The Pentium has a 32-bit address bus and a 64-bit data bus. It is software-compatible with all previous microprocessors. The Pentium has an internal, split data and instruction, 16KB write-back cache. It includes pipelined math coprocessor functions and superscalar architecture (two execution units).

Pentium Pro The Pentium Pro has a 32-bit address bus and a 64-bit data bus. It integrates a 256KB level-2 cache in a dual cavity pin grid array (P6A) package. It provides a substantial performance increase while maintaining binary compatibility with 8086, 80286, i386, Intel486 and Pentium microprocessors.

Power Supply

The power supply converts the AC input voltage to four DC output voltages and provides power for the following:

- System board
- Adapters
- Internal DASD drives
- Keyboard and auxiliary device

The power supply requirements are supplied by a 145-watt (PC 330) or 200-watt (PC 350 and PC 360) power supply. The following table shows the input power specifications for personal computers. The power available for each component with the system is shown in Table 10 on page 14.

Table 6. AC Input Power Requirements

Specification	Measurements
Input voltage (range is switch selected; sinewave input is required)	
Low range	100 (min)–125 (max) V ac
High range	200 (min)–240 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

DC Output Parameters

The power supply DC outputs characterized in the following tables, include the current supply capability of all the connectors including planar, DASD, PCI, and auxiliary outputs.

PC 330—Pentium

Table 7. DC Output Parameters (145 Watt) PC 330—Pentium

Output Voltage	Regulation	Minimum Current (amps)	Maximum Current (amps)
+5 volts	+5% to -4%	1.5A	18.0A
+12 volts	+5% to -4%	0.2A	4.2A
-12 volts	+10% to -9%	0.0A	0.4A
-5 volts	+5% to -4%	0.0A	0.3A
+3.3 volts (1)	+5% to -4%	0.0A	10.0A
+5 volt (aux)	+5% to -10%	0.0A	.02A

Note: Simultaneous loading of +5v/3.3v must not exceed 90 watts maximum.

PC 350—Pentium

Table 8. DC Output Parameters (200 Watt) PC 350—Pentium

Output Voltage	Regulation	Minimum Current (amps)	Maximum Current (amps)
+5 volts	+5% to -4%	1.5A	20.0A
+12 volts	+5% to -4%	0.2A	8.0A
-12 volts	+10% to -9%	0.0A	0.5A
-5 volts	+5% to -4%	0.0A	0.5A
+3.3 volts (1)	+5% to -4%	0.0A	20.0A
+5 volt (aux)	+5% to -10%	0.0A	.02A

Note: Simultaneous loading of +5v/3.3v must not exceed 90 watts maximum.

PC 360—Pentium Pro

The power supply provides 180 Watts continuous/200 Watts peak power to the planar and peripherals. It provides a fan that cools both the power supply and the microprocessor by drawing external air through the power supply and blowing it onto the processor. A single connector provides the voltages required by the planar, including 3.3VDC. Five connectors are provided for attachment of peripheral devices. Three are used by devices that ship standard with the system (3.5-inch diskette drive, 6x CDROM, IDE, or SCSI hard disk drive).

Table 9. DC Output Parameters (200 Watt) PC 360—Pentium Pro

Output Voltage	Regulation	Minimum Current (amps)	Maximum Current (amps)
+12VDC	+/-5%	0.0	6.0
+5VDC	+/-5%	1.0	22.0
+3.3VDC	+/-5%	0.3	14.0
-5VDC	+/-10%	0.0	0.5[1]
-12VDC	+/-10%	0.0	0.8[1]
+5VSB	+/-5%	0.0	0.010

Note: The system has 6 bays and the power supply provides 5 power connectors. In order to power a 6th device, the user must purchase a Y-connector.

Component Outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The system board voltages are +5 V dc, –5 V dc, +12 V dc, and –12 V dc. The drive voltages are +5 V dc and +12 V dc. The following table shows the approximate power that is provided for system components. Many components draw less current than the maximum shown.

Table 10 (Page 1 of 2). Component Maximum Current

Supply Voltage	Maximum Current	Regulation Limits
System Board:		
+5.0 V dc	4.000 A[1]	+5.0% to –4.5%
+12.0 V dc	0.025 A	+5.0% to –4.5%
–12.0 V dc	0.025 A	+10.0% to –9.5%
Keyboard Port:		
+5.0 V dc	275 mA	+5.0% to –4.5%
Auxiliary Device Port:		
+5.0 V dc	300 mA	+5.0% to –4.5%
AT-Bus Adapter Cards (Per Slot):		
+5.0 V dc	2.000 A	+5.0% to –4.5%
–5.0 V dc	0.100 A	+10.0% to –9.5%
+12.0 V dc	0.175 A	+5.0% to –4.5%
–12.0 V dc	0.100 A	+10.0% to –9.5%
PCI bus Adapter Cards (Per Slot):		
+5.0 V dc	5.000 A	+5.0% to –4.5%
+3.3 V dc[2]	5.000 A	±300 mV

[1] Maximum total combined output current on -12V and -5V outputs is 0.8A.

Table 10 (Page 2 of 2). Component Maximum Current

Supply Voltage	Maximum Current	Regulation Limits
Internal DASD:		
+5.0 V dc	1.000 A	+5.0% to –4.5%
+12.0 V dc	1.500 A	+5.0% to –4.5%

[1] This load varies according to personal computer system type and microprocessor type.

Note: Some adapters and hard disk drives draw more current than the recommended limits. Special attention should be given as to how suitable that device is for use in any system. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output Protection

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply.

If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector Description

The power supply has up to five 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in Table 10 on page 14. Signal and pin assignments are shown on page 28.

Other System Features

This section contains information about additional features available on all personal computers. These features include security features and advanced power management.

Security Features

The following security features are supported on personal computers.

- Cover key lock[2]
- U-bolt anchoring[3]
- Diskette write protect
- Serial port I/O control
- Parallel port I/O control
- Power-on password
- Administrator password
- Boot sequence control
- Unattended start mode
- Sliding front door lock[4]

Power-On Password

Eight bytes of RT/CMOS RAM are reserved for the power-on password and the check character.

The user can set, change, or delete a power-on password by using the Configuration/Setup Utility Program. A power-on password can be from 1 to 7 characters long. The power-on password never appears on the screen.

If the power-on password is unknown or forgotten, it can be bypassed (erased) with the following procedure:

1. Power-off the system.
2. Move the password jumper (on the system board) so that it connects the center pin and the previously unjumpered pin on the opposite end of the connector. For more details, see *Installing Options in Your Personal Computer*.
3. Power-on the system.

Note:

In the 300 Series Personal Computers, this procedure erases both the power-on password and the administrator password, as well as the current computer configuration. Use the Configuration/Setup Utility Program to reconfigure the computer and reset passwords.

Administrator Password

The administrator password prevents unauthorized access to the Configuration/Setup Utility Program.

An authorized user can set, change, or delete an administrator password by using the Configuration/Setup Utility Program. An administrator password can be from 1 to 7 characters long. The administrator password never appears on the screen.

In the 300 Series Personal Computers, both the administrator password and the power-on password are removed by moving the password jumper located on the system board, as described in the previous section. (See *Installing Options in Your Personal Computer*).

---

2 The PC 360—Pentium Pro provides for the use of a padlock instead of a cover key lock.

3 The PC 360—Pentium Pro does not have a U-bolt option.

4 The PC 360—Pentium Pro does not have a sliding front door lock.

Selectable Drive-Startup Sequence

The selectable drive-startup (selectable boot) sequence allows the user to specify the order in which the devices are searched for the boot record of an operating system. The diskette drive (A), hard disk drives, and remote program load (RPL) can be part of the search sequence. Changing the sequence for selectable drive-startup affects the drive-letter assignment each time the system is reset (either a power-on reset or a soft reset).

The user selects the sequence by using the Setup Utility. Drive B is not selectable in the sequence; however in some systems, Drive B can be mapped as Drive A making it selectable. The selected sequence is then stored in RT/CMOS RAM. After the system is reset, it searches, in the specified sequence, for a device that contains a boot record.

After the operating system is booted, the drive lettering is determined by where the boot record was found and by the search sequence.

Advanced Power Management

The PC 330/350—Pentium personal computer IBM 300 Series come with built-in energy-saving capabilities. Power management is a feature that reduces the power consumption of systems when they are not being used. Power management, when enabled, initiates reduced power modes for the display, microprocessor, and hard disk drive after a specified period of inactivity.

The next table summarizes the power-management modes.

Table 11. Power Management Modes

Mode	Power	Response
On (Ready)	System is at full power	Standard operation
On (Standby)	System is at reduced power	Any use of keyboard, mouse, or hard disk drive restores full power
Off	System is powered off	Power switch restores full power

The PC 330/350—Pentium systems BIOS has support for APM V1.O AND V1.1. This enables the system to enter a *Power Managed* state, which reduces the power drawn from the AC wall outlet. Power Management is enabled through the Configuration/Setup Utility Program and is controlled by the individual operating system.

Note: The PC 360—Pentium Pro personal computer does not have Power Management capabilities.

Physical Specifications

The following tables describe the physical specifications of IBM 300 Series personal computers. Each mechanical package is described separately.

PC 330—Pentium

Table 12. Physical Specifications PC 330—Pentium

Size	
Width	360 mm (14.2 in.)
Depth	450 mm (17.7 in.)
Height	130 mm (5.1 in.)
Weight	
Minimum configuration	8.6 kg (19.0 lb)
Maximum configuration (fully populated with typical options)	10.4 kg (23.0 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	3.05 m (10 ft)
Air Temperature	
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 80%
System off	8% to 80%
Maximum Altitude[1]	2133.6 m (7000 ft)
Heat Output	
Minimum configuration	35 W (120 BTU per hour)
Maximum configuration[2]	200 W (685 BTU per hour)
Electrical	
Input voltage (range is switch selected; sinewave input is required)	
Low range	100 (min) to 125 (max) V ac
High range	200 (min) to 240 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, in kilovolt-ampere (kVA)	
Minimum configuration	0.08 kVA
Maximum configuration	0.30 kVA
Electromagnetic Compatibility	FCC Class B

[1] This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
[2] Based on the 145-watt maximum capacity of the system power supply.

PC 350—Pentium

Table 13. Physical Specifications PC 350—Pentium

Size	
Width	420 mm (16.5 in.)
Depth	448 mm (17.6 in.)
Height	160 mm (6.3 in.)
Weight	
Minimum configuration	12.7 kg (28.0 lb)
Maximum configuration (fully populated with typical options)	14.1 kg (31.1 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	3.05 m (10 ft)
Air Temperature	
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 80%
System off	8% to 80%
Maximum Altitude[1]	2133.6 m (7000 ft)
Heat Output	
Minimum configuration	35 W (120 BTU per hour)
Maximum configuration[2]	310 W (1060 BTU per hour)
Electrical	
Input voltage (range is switch selected; sinewave input is required)	
Low range	110 (min) to 125 (max) V ac
High range	200 (min) to 240 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, in kilovolt-ampere (kVA)	
Minimum configuration	0.08 kVA
Maximum configuration	0.52 kVA
Electromagnetic Compatibility	FCC Class B

[1] This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
[2] Based on the 200-watt maximum capacity of the system power supply.

PC 360—Pentium Pro

Table 14. Physical Specifications PC 360—Pentium Pro

Size	
Width	21 cm (8.3 in.)
Depth	46 cm (18 in.)
Height	40.5 cm (16 in.)
Weight	
Minimum configuration	8.6 kg (19.0 lb)
Standard configuration as shipped	13.4 kg (29.5 lb)
Cables	
Power cable	1.8 m (6 ft)
Keyboard cable	3.05 m (10 ft)
Air Temperature	
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)
Humidity	
System on	8% to 80%
System off	8% to 80%
Maximum Altitude[1]	2133.6 m (7000 ft)
Heat Output	
Minimum configuration	35 W (120 BTU per hour)
Maximum configuration[2]	310 W (1060 BTU per hour)
Electrical	
Input voltage (range is switch selected; sinewave input is required)	
Low range	100 (min) to 125 (max) V ac
High range	200 (min) to 240 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, in kilovolt-ampere (kVA)	
Minimum configuration	0.08 kVA
Maximum configuration	0.52 kVA
Electromagnetic Compatibility	FCC Class B

[1] This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
[2] Based on the 200-watt maximum capacity of the system power supply.

Chapter 2. Connectors and Jumpers

© Copyright IBM Corp. Februray 1996

System Board Connectors

The following tables show the connectors that are available on IBM 300 Series personal computer system boards and risers.

Diskette Drive Connector

The personal computer has a 34-pin connector that supports the attachment of up to two diskette drives. The following tables show the signal and pin assignments for the system board diskette drive connector for PC 300 Series computers.

Table 15. PC 300 Series Diskette Drive Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Ground	2	High density select
3	Ground	4	Not connected
5	Ground or key	6	-Data rate select 0
7	Ground	8	-Index
9	Ground	10	-Motor enable 0
11	Ground	12	-Drive select 1
13	Ground	14	-Drive select 0
15	Ground	16	-Motor enable 1
17	Ground or MSEN1	18	-Direction in
19	Ground	20	-Step
21	Ground	22	-Write data
23	Ground	24	-Write enable
25	Ground	26	-Track 0
27	Ground or MSEN0	28	-Write protect
29	Ground	30	-Read data
31	Ground	32	-Head 1 select
33	Ground	34	-Diskette change

Display Connector

The personal computer has a 15-pin display connector. The following table shows the signal and pin assignments for the system board display connector.

Table 16. Display Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Red video	2	Green video
3	Blue video	4	Monitor ID bit 2
5	Sync ground	6	Red ground
7	Green ground	8	Blue ground
9	Not connected	10	Sync ground
11	Monitor ID bit 0	12	Monitor ID bit 1/DDC1 serial data
13	Horizontal sync	14	Vertical sync/DDC1 clock
15	Monitor ID bit 3		

Hard Disk Drive Connectors (Primary/Secondary)

The personal computer provides a dedicated I/O channel for connecting a hard disk drive. The signals that are provided by this connector include the 16-bit data bus, address lines A0 to A2, IRQ, and -IO CS16. These signals operate in the same way as the normal I/O-channel signals. The interface to the hard disk drive complies with *ANSI ATA-2 (AT Attachment), Rev. 2j*, dated 2 December 1994.

The address decode logic for the hard disk drive is on the system board. On a valid decode of A0 through A15 equal to hex 01F0 through 01F7, -HFCS0 (hex 0170 through 0177, -HFCS2 for a secondary hard disk

drive) goes active. On a valid decode of A0 through A15 equal to hex 03F6 through 03F7, -HFCS1 (hex 0376 through 0377, -HFCS3 for a secondary hard disk drive) goes active.

The following table shows the signal and pin assignments for the hard disk drive connector.

Table 17. Hard Disk Drive Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	-RESET	2	Ground
3	Data bus bit 7	4	Data bus bit 8
5	Data bus bit 6	6	Data bus bit 9
7	Data bus bit 5	8	Data bus bit 10
9	Data bus bit 4	10	Data bus bit 11
11	Data bus bit 3	12	Data bus bit 12
13	Data bus bit 2	14	Data bus bit 13
15	Data bus bit 1	16	Data bus bit 14
17	Data bus bit 0	18	Data bus bit 15
19	Ground	20	Key (Reserved)
21	DRQ0/DRQ1	22	Ground
23	-IO Write	24	Ground
25	-IO Read	26	Ground
27	IO Channel Ready	28	VCC pullup
29	DACK0/DACK1	30	Ground
31	IRQ14/IRQ15	32	VCC pullup
33	Device address A1	34	Ground
35	Device address A0	36	Device address A2
37	-HFCS0	38	-HFCS1
39	Activity #	40	Ground

I/O Channel Connector

The I/O channel (ISA bus) is buffered to provide sufficient drive for the 98-pin connectors, assuming two low-power Schottky (LS) loads per slot.

The following figure shows the signal and pin assignments for the I/O channel connectors.

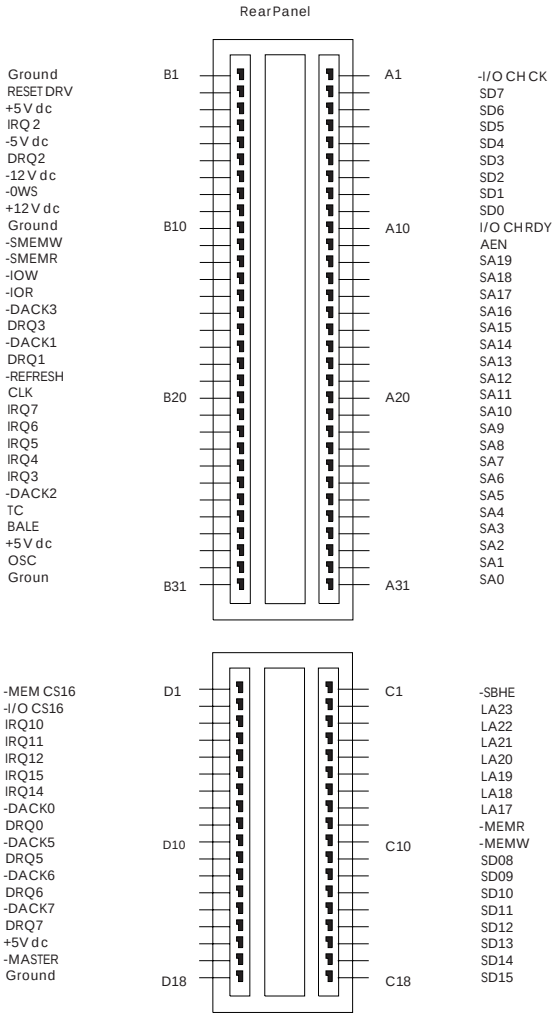


Figure 1. I/O Channel (ISA bus) Connector

Keyboard and Auxiliary-Device Connectors

The keyboard and auxiliary-device connectors use 6-pin miniature DIN connectors. The signals and voltages are the same for both connectors and are assigned as shown in the following table.

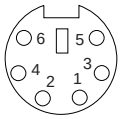


Table 18. Keyboard and Auxiliary-Device Signal and Pin Assignments

Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 V dc
5	I/O	Clock
6	NA	Reserved

Serial Port Connectors (A and B)

The interface uses the standard D-shell connector and pin assignments defined for RS-232D. The voltage levels are EIA only. Current loop interface is not supported.

The following table shows the signal and pin assignments for the serial port connector in a communication environment.

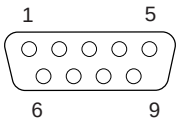


Table 19. Serial Port Connector Signal and Pin Assignments

Pin	I/O	Signal Name	Pin	I/O	Signal Name
1	I	Data carrier detect	6	I	Data set ready
2	I	Receive data	7	O	Request to send
3	O	Transmit data	8	I	Clear to send
4	O	Data terminal read	9	I	Ring indicator
7	NA	Signal ground			

Parallel Port Connector

The parallel port connector is a standard 25-pin D-shell connector. The following table shows the signal and pin assignments for the parallel port connector.

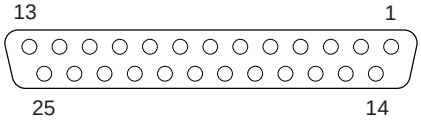


Table 20. Parallel Port Connector Signal and Pin Assignments

Pin	I/O	Signal Name	Pin	I/O	Signal Name
1	O	-STROBE	14	O	-AUTO FD XT
2	I/O	Data bit 0	15	I	-ERROR
3	I/O	Data bit 1	16	O	-INIT
4	I/O	Data bit 2	17	O	-SLCT IN
5	I/O	Data bit 3	18	NA	Ground
6	I/O	Data bit 4	19	NA	Ground
7	I/O	Data bit 5	20	NA	Ground
8	I/O	Data bit 6	21	NA	Ground
9	I/O	Data bit 7	22	NA	Ground
10	I	-ACK	23	NA	Ground
11	I	BUSY	24	NA	Ground
12	I	PE	25	NA	Ground
13	I	SLCT			

PCI Connectors

The Peripheral Component Interconnect (PCI) connector is a 124-pin connector. Personal computers with PCI risers support the 32-bit, 5 V dc, local-bus signalling environment that is defined in the *PCI Local Bus Specification - Revision 2.0*. The following table shows the signal and pin assignments for the PCI connector.

Note: 3.3 V dc is supplied through an optional 5 V dc to 3.3 V dc regulator.

Table 21 (Page 1 of 2). PCI Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1 A	TRST#	32 A	Address 16
2 A	+12 V dc	33 A	+3.3 V dc
3 A	TMS	34 A	FRAME#
4 A	TDI	35 A	Ground
5 A	+5 V dc	36 A	TRDY#
6 A	INTA#	37 A	Ground
7 A	INTC#	38 A	STOP#
8 A	+5 V dc	39 A	+3.3 V dc
9 A	Reserved	40 A	SDONE
10 A	+5 V dc (I/O)	41 A	SBO#
11 A	Reserved	42 A	Ground
12 A	Ground	43 A	PAR
13 A	Ground	44 A	Address/Data 15
14 A	Reserved	45 A	+3.3 V dc
15 A	RST#	46 A	Address/Data 13
16 A	+5 V dc (I/O)	47 A	Address/Data 11
17 A	GNT#	48 A	Ground
18 A	Ground	49 A	Address/Data 9
19 A	Reserved	50 A	Connector key
20 A	Address/Data 30	51 A	Connector key
21 A	+3.3 V dc	52 A	C/BE 0“#
22 A	Address/Data 28	53 A	+3.3 V dc
23 A	Address/Data 26	54 A	Address/Data 6
24 A	Ground	55 A	Address/Data 4

Table 21 (Page 2 of 2). PCI Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
25 A	Address/Data 24	56 A	Ground
26 A	IDSEL	57 A	Address/Data 2
27 A	+3.3 V dc	58 A	Address/Data 0
28 A	Address/Data 22	59 A	+5 V dc (I/O)
29 A	Address/Data 20	60 A	REQ64#
30 A	Ground	61 A	+5 V dc
31 A	Address/Data 18	62 A	+5 V dc
1 B	–12 V dc	32 B	Address/Data 17
2 B	TCK	33 B	C/BE 2“#
3 B	Ground	34 B	Ground
4 B	TDO	35 B	IRDY#
5 B	+5 V dc	36 B	+3.3 V dc
6 B	+5 V dc	37 B	DEVSEL#
7 B	INTB#	38 B	Ground
8 B	INTD#	39 B	LOCK#
9 B	PRSNT1#	40 B	PERR#
10 B	Reserved	41 B	+3.3 V dc
11 B	PRSNT2	42 B	SERR#
12 B	Ground	43 B	+3.3 V dc
13 B	Ground	44 B	C/BE 1“#
14 B	Reserved	45 B	Address/Data 14
15 B	Ground	46 B	Ground
16 B	CLK	47 B	Address/Data 12
17 B	Ground	48 B	Address/Data 10
18 B	REQ#	49 B	Ground
19 B	+5 V dc (I/O)	50 B	Connector key
20 B	Address/Data 31	51 B	Connector key
21 B	Address/Data 29	52 B	Address/Data 8
22 B	Ground	53 B	Address/Data 7
23 B	Address/Data 27	54 B	+3.3 V dc
24 B	Address/Data 25	55 B	Address/Data 5
25 B	+3.3 V dc	56 B	Address/Data 3
26 B	C/BE 3“#	57 B	Ground
27 B	Address/Data 23	58 B	Address/Data 1
28 B	Ground	59 B	+5 V dc (I/O)
29 B	Address/Data 21	60 B	ACK64#
30 B	Address/Data 19	61 B	+5 V dc
31 B	+3.3 V dc	62 B	+5 V dc

Power Supply Connectors

The power supply in personal computers has up to five 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in Table 10 on page 14.

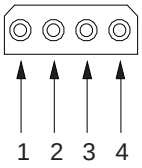


Table 22. Power Supply Connector (Internal Devices) Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	+12 V dc	3	Ground
2	Ground	4	+5 V dc

The PC 330/350 systems have a 12-pin power supply connector. The following table shows the signal and pin assignments for the system board power supply connector.

Table 23. Power Supply Connector (System Board) Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Power good (+5 V dc)	2	+5 V dc
3	+12 V dc	4	–12 V dc
5	Ground	6	Ground
7	Ground	8	Ground
9	–5 V dc	10	+5 V dc
11	+5 V dc	12	+5 V dc

The PC 330/350 systems have an additional 6-pin power supply connector which plugs into the riser. The following table shows the signal and pin assignments for the system board power supply connector.

Table 24. Power Supply Connector (3.3 V dc) Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Ground	2	Ground
3	Ground	4	+3.3 V dc
5	+3.3 V dc	6	+3.3 V dc

System Board Memory Connectors

All system boards have four 72-pin memory connectors. For more information on the supported single inline memory modules for each system see Table 28 on page 36.

The following table shows the signal and pin assignments for the 72-pin system board memory connectors. Data bits 0 through 15 are the low word, and data bits 16 through 31 are the high word.

Note: The PC 330/350 system boards do not support parity detection. (Pins 35-38)

Table 25. System Board Memory Connector Signal and Pin Assignments

Pin	Signal	Pin	Signal
1	Ground	37	Parity 1
2	Data 0	38	Parity 3
3	Data 16	39	Ground
4	Data 1	40	Column address strobe 0
5	Data 17	41	Column address strobe 2
6	Data 2	42	Column address strobe 3
7	Data 18	43	Column address strobe 1
8	Data 3	44	Row address strobe 0
9	Data 19	45	Row address strobe 1
10	+5 V dc	46	Reserved
11	Reserved	47	Write enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Address 10	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 V dc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Reserved	65	Data 15
30	+5 V dc	66	Reserved
31	Address 8	67	Reserved
32	Address 9	68	Reserved
33	Row address strobe 3	69	Reserved
34	Row address strobe 2	70	Reserved
35	Parity 2	71	Reserved
36	Parity 0	72	Ground

Video Feature Connector

The personal computer has a 26-pin connector that supports the attachment of additional video features. The following table shows the signal and pin assignments for the video feature connector.

Note: This connector is not present on PC 360—Pentium Pro systems.

Table 26. VESA Feature Connector For PC 330/350—Pentium Systems

Pin	Signal	Pin	Signal
1	Ground	2	Data 0
3	Ground	4	Data 1
5	Ground	6	Data 2
7	Data enable	8	Data 3
9	Sync enable	10	Data 4
11	PCLK enable	12	Data 5
13	Not used	14	Data 6
15	Ground	16	Data 7
17	Ground	18	PCLK
19	Ground	20	BLANK
21	Ground	22	HSYNC
23	Not used	24	VSYNC
25	Ground	26	Ground

System Board Jumpers

Changing Jumper Positions

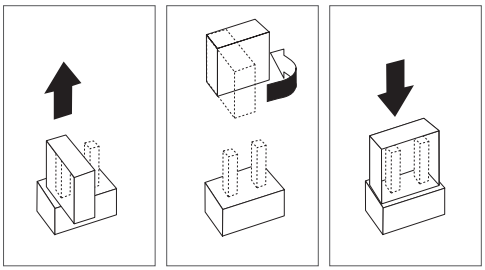
Personal computers have one or both of the following types of jumper blocks:

- Two-pin
- Three-pin

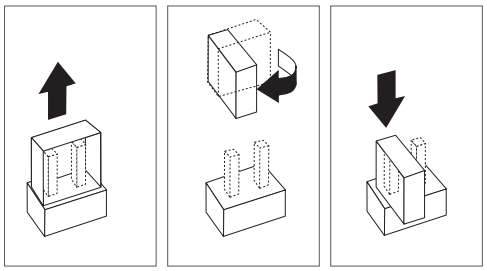
Two-Pin Jumper Blocks

With the two-pin jumper blocks, each jumper can be positioned to fit over both pins, one pin only, or it can be entirely removed. To change a jumper's position for a two-pin jumper block:

1. Turn off the system; then disconnect the system power cord.
2. Remove the system cover.
3. Lift the jumper straight off the pin block.
4. Do one of the following:
   - Align the holes in the bottom of the jumper with the two pins on the pin block, and then slide the jumper onto these pins.



- Align one of the holes in the bottom of the jumper with one of the pins on the pin block, and then slide the jumper onto that pin only.

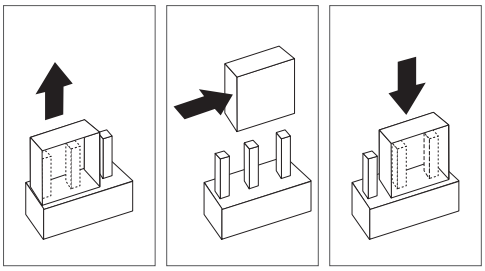


5. Reinstall the system cover.
6. Reconnect the system power cord; then turn on system power.

Three-Pin Jumper Blocks

With the three-pin jumper blocks, each jumper covers two of the three pins on a pin block. To change a jumper's position for a three-pin jumper block:

1. Turn off the system; then disconnect the system power cord.
2. Remove the system cover.
3. Lift the jumper straight off the pin block.
4. Align the holes in the bottom of the jumper with the center pin and the pin that was not covered previously.

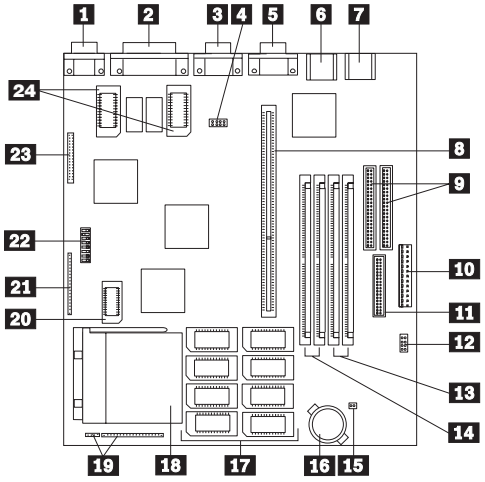


5. Slide the jumper fully onto these pins.
6. Reinstall the system cover.
7. Reconnect the system power cord; then turn on system power.

System Board PC 330/350—Pentium (75/90/100 MHz)

Note: Your system board might look slightly different from the one shown in this book. Your personal computer has the system board diagram, switch and jumper settings, pasted to the inside cover.

PC 330/350—Pentium (75/90/100 MHz) System Board

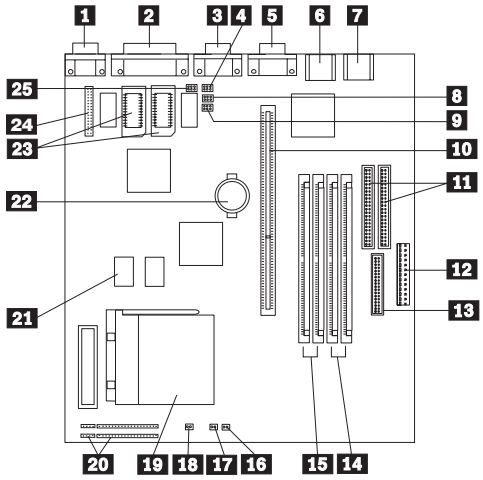


1. Video Port
2. ECP/EPP Parallel Port
3. Serial (B) Port
4. Boot Block Jumper
5. Serial (A) Port
6. PS/2 Mouse Port
7. PS/2 Keyboard Port
8. ISA/PCI Riser Connector
9. Primary/Secondary IDE Connectors
10. Primary Power Supply Input
11. Diskette Connector
12. VRE Jumper
13. Memory SIMMs 1,2 (BANK 0)
14. Memory SIMMs 3,4 (BANK 1)
15. 3.3V Voltage Regulator
16. Battery
17. 256K/512KB L2 Cache Sockets (Optional)
18. Processor Socket (5)
19. Front Panel I/O Connectors
20. L2 Tag Ram (Optional)
21. Front Panel I/O Connectors
22. Configuration Switch Block
23. VESA Feature Connector
24. 1 MB Video Memory Sockets (Optional)

System Board PC 330/350—Pentium (120/133/150/166 MHz)

Note: Your system board might look slightly different from the one shown in this book. Your personal computer has the system board diagram, switch and jumper settings, pasted to the inside cover.

PC 330/350—Pentium (120/133/150/166 MHz) System Board

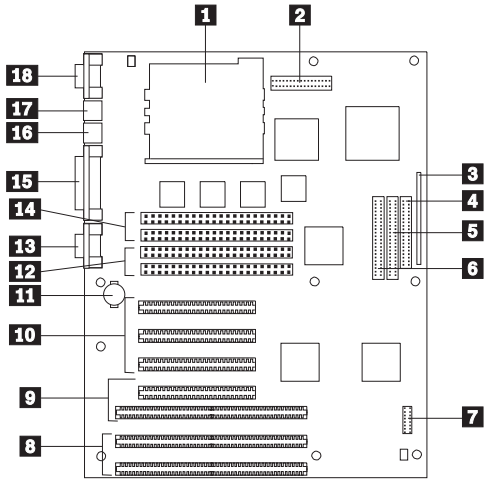


1. Video Port
2. ECP/EPP Parallel Port
3. Serial (B) Port
4. Configuration Jumpers
5. Serial (A) Port
6. PS/2 Mouse Port
7. PS/2 Keyboard Port
8. Configuration Jumpers
9. Configuration Jumpers
10. ISA/PCI Riser Connector
11. Enhanced IDE Connectors
12. Primary Input Power Supply
13. Diskette Connector
14. Memory SIMMs 3,4 (Bank 1)
15. Memory SIMMs 1,2 (Bank 0)
16. Power-On LED Connector
17. Hard Disk Activity LED Connector
18. Auxiliary Fan Connector
19. Processor Socket (7)
20. Speaker Connector
21. 256KB Synchronous Burst L2 Cache Sockets
22. Battery
23. 1MB Video Memory Sockets (Optional)
24. VESA Feature Connector
25. Configuration Jumpers

System Board PC 360—Pentium Pro

Note: Your system board might look slightly different from the one shown in this book. Your personal computer has the system board diagram, switch and jumper settings, pasted to the inside cover.

PC 360—Pentium Pro System Board



1. Processor Socket (8)
2. Primary Power Supply Input
3. Front Panel Connectors
4. Diskette Connector
5. Primary IDE Connector
6. Seconday IDE Connector
7. Configuration Switch Block
8. ISA Slots
9. Shared ISA/PCI Slots
10. PCI Slots
11. Battery
12. Memory SIMMs 3,4 (Bank 1)
13. Serial (B) Port
14. Memory SIMMs 1,2 (Bank 0)
15. ECP/EPP Parallel Port
16. PS/2 Mouse Port
17. PS/2 Keyboard Port
18. Serial (A) Port

Chapter 3. Memory Subsystems

© Copyright IBM Corp. Februray 1996

Memory Description

Personal computers use the following types of memory:

- Flash memory (sometimes called flash ROM)
- Random access memory (RAM)
- Nonvolatile random access memory (NVRAM)
- Cache memory

Flash Memory Subsystem

The flash memory subsystem contains 256KB of read-only memory. Mapped flash memory is active at power-on time and is assigned the top of the first and last 1MB of the address range (addresses hex 000E0000h to 000FFFFFh and FFFE0000h to FFFFFFFFh). After POST ensures that system memory is operating properly, the ROM code is copied to RAM address range hex 000E0000h to 000FFFFFh, and ROM access at the top of the last 1MB of the address range (FFFE0000h to FFFFFFFF) is disabled.

The Flash component is organized as 256 x 8 (256 KB). The Flash device is divided into five areas. See Table 27.

Table 27. Flash Memory Organization

Address	Address	Flash Memory Area
F0000H	FFFFFH	64 KB Main BIOS
EC000H	EFFFFH	16 KB Boot Block (Not Flash erasable)
EA000H	EBFFFH	8 KB Plug and Play ESCD storage area
E8000H	E9FFFH	8 KB IBM LOGO and vital product data (VPD)
E0000H	E7FFFH	32 KB system BIOS reserved during boot

RAM Subsystem

The following table describes the RAM subsystem for personal computers. Personal computers have 72-pin memory connectors.

Table 28. Memory Types and Sizes

Machine Type/ Model Name	Memory Connectors	Supported Inline Memory Modules	Maximum Memory Supported
PC 330/350—Pentium	Four 72-pin	4MB, 8MB, 16MB, 32MB (70ns Fast Page) or (60ns EDO)[2]	128MB
360—Pentium Pro (P150 MHz)	Four 72-pin	4MB, 8MB, 16MB, 32MB (60 ns Fast Page)[2]	128MB

[2] Memory modules must be installed in matched pairs. Tin lead SIMMs are required.

PC 330/350—Pentium

The PC 330/350—Pentium systems memory controller does not generate memory data parity; therefore, parity checking is not done. If you install parity SIMMs, the parity bits are ignored.

PC 360—Pentium Pro

The PC 360—Pentium Pro planar provides four 72-pin SIMM 5.0 volt sites for memory expansion. The sockets support 1M x 32/36 (4MB), 2M x 32/36 (8MB), 4M x 32/36 (16 MB), and 8M x 32/36 (32MB) single-sided or double-sided SIMM modules. The maximum memory size, using four 8M x 32/36 SIMM modules, is 128MB. Memory timing requires 60 ns fast page devices. When 36-bit parity SIMMs are installed, error correction code (ECC) will be supported (i.e. the parity bits are used to store ECC syndrome data). Tin lead SIMMs are required.

The four SIMM sockets are arranged as interleave-0 and interleave-1, with each interleave consisting of two sockets and providing a 64-bit wide data path. Because of the 2-way interleaved memory architecture (for improved performance), all slots have to be populated by same size SIMMs. If only two slots of interleave-0 or interleave-1 are populated, memory functions in non-interleaved mode. The minimum memory size for 2-way interleaving is 16MB using four 4MB SIMMs. There are no jumper settings required for the memory size or type, which is automatically detected by the system BIOS. The tables that follow show the preferred combinations of single inline memory modules (SIMMs) for the PC 330/350—Pentium personal computers.

Table 29. PC 330/350—Pentium System Memory Table

Total Memory	Bank 0 SIMM 1 and 2	Bank 1 SIMM 3 and 4
8MB	4MB	–
16MB	4MB	4MB
16MB	8MB	–
24MB	4MB	8MB
24MB	8MB	4MB
32MB	16MB	–
32MB	8MB	8MB
40MB	4MB	16MB
40MB	16MB	4MB
72MB	4MB	32MB
80MB	32MB	8MB
128MB	32MB	32MB

Note: These are the *preferred* combinations of SIMMS for your computer because they provide the best performance. Each bank must contain a matched pair of SIMMs having the same size and speed.

The PC 360—Pentium Pro supports only 60ns, or faster, Fast Page DRAMs. It must be noted that using faster than specified SIMMs will not improve memory performance since memory timings are fixed to support only 60ns SIMMs. If Fast page DRAM is installed in both banks, all SIMMs must be of the same size. If only one bank is to be populated, then populate bank 1 to facilitate easier memory upgrades. Otherwise bank 0 SIMMs must be removed and reinstalled after installing bank 1 SIMMs.

Table 30. PC 360—Pentium Pro System Memory Table

Total Memory	Bank 0 SIMM 1 and 2	Bank 1 SIMM 3 and 4
8MB	4MB	–
16MB	4MB	4MB[5]
16MB	8MB	–
32MB	8MB	8MB[5]
32MB	16MB	–
64MB	32MB	–
64MB	16MB	16MB[5]
128MB	32MB	32MB[5]

System Memory Map

The first 640KB of system board RAM is mapped starting at address hex 00000000. A 256-byte area and a 1KB area of this RAM are reserved for BIOS data areas. See the section about BIOS data areas in the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for details.

The following figures show the memory maps for the IBM 300 Series personal computer systems. Memory can be mapped differently if POST detects an error.

Note: After POST completes, portions of the 64KB segment starting at memory address hex E0000 are available, for upper memory blocks and adapters.

PC 330/350—Pentium

Table 31. PC 330/350—Pentium - System Memory Map

Address Range (Decimal)	Address Range (hex)	Size	Description
1024K–131072K	100000–8000000	127M	Extended memory
960K–1023K	F0000–FFFFF	64K	System BIOS
944K–959K	EC000–EFFFF	16K	FLASH Boot Block
936K–943K	EA000–EBFFF	8K	ECSD (plug and play configuration area)
928K–935K	E8000–E9FFF	8K	OEM LOGO and vital product data area
896K–927K	E0000–E7FFF	32K	BIOS Reserved
800K–895K	C8000–DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K–799K	A0000–C7FFF	160K	Off-board video memory and BIOS
639K	9FC00–9FFFF	1K	Off-board video memory and BIOS
512K–638K	80000–9FBFF	127K	Extended conventional
0K–511K	00000–7FFFF	512K	Conventional

[5] Represents an *Interleaved* configuration for optimum performance.

PC 360—Pentium Pro

Table 32. PC 360—Pentium Pro System Memory Map

Address Range (Decimal)	Address Range (hex)	Size	Description
1024K–131072K	100000–8000000	127M	Extended memory
960K–1023K	F0000–FFFFF	64K	System BIOS
952K–959K	EC000–EFFFF	16K	FLASH Boot Block
948K–951K	EA000–EBFFF	8K	ECSD (plug and play configuration area)
944K–947K	E8000–E9FFF	8K	IBM LOGO
896K–943K	E0000–E7FFF	32K	BIOS Reserved
800K–895K	C8000–DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K–799K	A0000–C7FFF	160K	Off-board video memory and BIOS
639K	9FC00–9FFFF	1K	Off-board video memory and BIOS
512K–638K	80000–9FBFF	127K	Extended conventional
0K–511K	00000–7FFFF	512K	Conventional

Cache Memory

Cache memory is a RAM storage location between the microprocessor and system memory. All IBM 300 Series Pentium microprocessors have a 16KB level-1 cache that is internal to the microprocessor. All IBM 300 Series personal computer systems also support an external or level-2 (L2) cache. All IBM 300 Series system boards support either 0, or 256KB L2 cache. The following table shows the maximum L2 cache that is supported for each system board type in the IBM 300 Series personal computer family.

Table 33. L2 Cache

System Board	L2 Cache Standard	L2 Cache Maximum
PC 330/350—Pentium (75/90/100 MHz)	0KB[6]	256KB
PC 330/350—Pentium (120/133/150/166 MHz)	256KB[7]	256KB
PC 360—Pentium Pro	256KB[8]	256KB

6 Cache Sockets are on system board (Optional)

7 Synchronous burst SRAM soldered to the system board

8 L2 cache is internal on the PC 360—Pentium Pro microprocessor

Chapter 4. System Compatibility

© Copyright IBM Corp. Februray 1996

Compatibility Description

When you design application programs, either for a specific model, or for many models and multiple product lines, you must consider certain compatibility issues. This section briefly discusses hardware, software, and BIOS compatibility issues.

Hardware Compatibility

The personal computer family maintains many of the interfaces used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces for the personal computer family are compatible with the following interfaces:

- The Intel 8259 interrupt controllers (edge-triggered mode).
- The National Semiconductor NS16450 and NS16550A serial communication controllers.
- The Motorola MC146818 Time of Day Clock command and status (CMOS reorganized).
- The Intel 8254 timer, driven from a 1.193-MHz clock (channels 0, 1, and 2).
- The Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions. The Mode register is partially supported.
- The Intel 8272 or 82077 diskette drive controllers.
- The Intel 8042 keyboard controller at addresses hex 0060 and 0064.
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.

Use the following information to develop application programs for personal computer products. Whenever possible, use BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware Interrupts

Hardware interrupts are level-sensitive in systems using PCI bus architecture, and are edge-triggered in systems using the Personal Computer type I/O architecture. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent, regardless of whether the incoming interrupt request to the controller is active or inactive.

In systems using level-sensitive interrupts, the interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation, or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

The interrupt controller in systems using level-sensitive interrupts requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag (STI) command

In systems using level-sensitive interrupts, hardware prevents the interrupt controllers from being set to the edge-triggered mode. In systems using edge-triggered interrupts, hardware prevents the interrupt controllers from being set to the level-sensitive mode.

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt hex 71) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Diskette Drives and Controller

The following tables show the reading, writing, and formatting capabilities of each type of diskette drive.

Table 34. 5.25-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	160/180KB Mode	320/360KB Mode	1.2MB Mode
5.25-inch diskette drive:			
Single sided (48 TPI)	RWF	—	—
Double sided (48 TPI)	RWF	RWF	—
High capacity (1.2MB)	RWF	RWF	RWF

R = Read W = Write F = Format

Table 35. 3.5-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	720KB Mode	1.44MB Mode	2.88MB Mode
3.5-inch diskette drive:			
1.44MB drive	RWF	RWF	—
2.88MB drive	RWF	RWF	RWF

R = Read W = Write F = Format

Notes:

1. You cannot use 5.25-inch diskettes that are designed for the 1.2MB mode in either a 160/180KB or 320/360KB diskette drive.
2. Low-density 5.25-inch diskettes that are written to or formatted by a high-capacity 1.2MB diskette drive can be reliably read only by another 1.2MB diskette drive.
3. You cannot use 3.5-inch diskettes that are designed for the 2.88MB mode in a 1.44MB diskette drive.

Copy Protection

The following methods of copy protection might not work in systems using the 3.5-inch 1.44MB diskette drive.

- Bypassing BIOS routines:
  - Data transfer rate: BIOS selects the proper data transfer rate for the media being used.
  - Diskette parameter table: Copy protection, which creates its own diskette parameter table, might not work in these drives.
- Diskette drive controls:
  - Rotational speed: The time between two events in a diskette drive is a function of the controller.
  - Access time: Diskette BIOS routines must set the track-to-track access time for the different types of media that are used in the drives.
  - 'Diskette change' signal: Copy protection might not be able to reset this signal.
- Write-current control: Copy protection that uses write-current control does not work, because the controller selects the proper write current for the media that is being used.

Detailed information about specific diskette drives is available in the *IBM Personal System/2 Hardware Interface Technical Reference—Common Interfaces* and in separate option technical references.

Hard Disk Drives and Controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported. Detailed information about specific hard disk drives and hard disk drive adapters is available in the *IBM Personal System/2 ATA/IDE Fixed Disk Drives Technical Reference*.

Software Compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software Interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, you must check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-Sensitive Programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function ((AH)=C0H). See the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of model bytes for other IBM Personal Computer and Personal System/2 products, and see page 2 for the personal computer model and submodel bytes.

BIOS Compatibility

The personal computer systems support BIOS interfaces as described in the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*.

Chapter 5. Direct Memory Access Controller

© Copyright IBM Corp. Februray 1996

DMA Description

The direct memory access (DMA) controller allows data to be transferred directly between I/O devices and memory, bypassing the system microprocessor. This allows greater system microprocessor throughput by freeing the system microprocessor of I/O tasks.

The DMA controller is software programmable. The system microprocessor can address the DMA controller and read or modify the internal registers to define the DMA modes, transfer addresses, transfer counts, channel masks, and page registers.

The functions of the DMA controller can be grouped into two categories: program condition and DMA transfer.

During program condition, the DMA registers can be programmed or read. Program condition commences when the system microprocessor refers to the DMA controller within a specific address range (see “DMA I/O Address Map” on page 49). The DMA controller needs a minimum of 1.25 microseconds to complete any program command that is generated by the system microprocessor. Each single transfer requires a minimum of 1.25 microseconds to transfer either a byte or a word.

The DMA controller supports:

- Register and program compatibility with the IBM Personal Computer AT DMA channels (8237-compatible mode)
- 16MB (24-bit) address capability for memory
- Seven independent DMA channels that are capable of transferring data between memory and I/O devices
- Serial DMA operations with overlapped read and write cycles for each transfer operation
- Each channel fixed to a byte or word transfer
- Sharing of the system bus interface and control logic

DMA Controller Operations

The DMA controller performs one type of operation: data transfers between memory and I/O devices.

The DMA controller performs serial transfers with a minimum of five 200-nanosecond clock cycles for memory-to-I/O or I/O-to-memory operations. No burst mode or memory-to-memory transfers are supported.

Byte Pointer

The byte pointer is a flip-flop that allows 8-bit ports to access the contents of the 16-bit registers in the DMA controller. The Clear Byte Pointer command resets the flip-flop to point to the low byte.

A read or write operation on the first 8 bits of the 16-bit register transfers the low byte and toggles the flip-flop. A read or write operation on the second 8 bits of the 16-bit register transfers the high byte and again toggles the flip-flop.

DMA Channels

DMA channels 0 through 3 support 8-bit data transfers between 8-bit I/O adapters and 8-bit or 16-bit system memory. Each channel can transfer data throughout the 16MB system-address space in 64KB blocks. The system board includes the logic that contains the equivalent of two 8237 controller chips.

The following table shows the DMA channel assignments for personal computers.

Table 36. DMA Channel Assignments

Channel	Data Width	Assignment
DRQ0	8 bits	Unused
DRQ1	8 bits	Unused
DRQ2	8 bits	Diskette drive
DRQ3	8 bits	Unused[1]
DRQ4		Cascade
DRQ5	16 bits	Unused
DRQ6	16 bits	Unused
DRQ7	16 bits	Unused

[1] Used by parallel port if in ECP mode.

Address Generation for DMA Channels 0 through 3

The following table shows address generation for DMA channels 0 through 3.

Table 37. DMA Address Generation for Channels 0–3

Source	DMA Page Registers	Controller
Address	A23---------A16	A15---------A0

Note: The 'byte high enable' (BHE) addressing signal is generated by inverting address line A0.

Address Generation for DMA Channels 5 through 7

DMA channel 4 is used to cascade channels 5 through 7 to the microprocessor. Channels 5, 6, and 7 support 16-bit data transfers between 16-bit I/O adapters and 16-bit system memory. These channels can transfer data throughout the 16MB system-address space in 128KB blocks. Channels 5, 6, and 7 cannot transfer data on odd-byte boundaries.

The following table shows address generation for the DMA channels 5 through 7.

Table 38. DMA Address Generation for Channels 5–7

Source	DMA Page Registers	Controller
Address	A23---------A17	A16---------A1

Note: The addressing signals, BHE and A0, are forced to logical 0.

Page Register Addresses

The following table shows the addresses for the page registers.

Table 39. Page Register Addresses

Page Register	I/O Address (Hex)
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

Addresses for all DMA channels do not increase or decrease through page boundaries (64KB for channels 0 through 3, and 128KB for channels 5 through 7).

DMA channels 5 through 7 perform 16-bit data transfers. Access is only to 16-bit devices (I/O or memory) during the DMA cycles of channels 5 through 7. Access to the DMA controller, which controls these channels, is through I/O addresses hex 0C0 through 0DF.

All DMA memory transfers that are performed with channels 5 through 7 must occur on even-byte boundaries. When the base address for these channels is programmed, the real address divided by 2 is written to the Base Address register. When the base word count for channels 5 through 7 is programmed, the count is the number of 16-bit words that are to be transferred. Therefore, DMA channels 5 through 7 can transfer 65 536 words, or 128KB maximum, for any selected page of memory. These DMA channels divide the 16MB memory space into 128KB pages. When the DMA page registers for channels 5 through 7 are programmed, data bits D7 through D1 contain the most significant 7 address bits (A23 through A17) of the desired memory space. Data bit D0 of the page registers for channels 5 through 7 is not used in the generation of the DMA memory address.

At power-on time, all internal locations, especially the mode registers, should be loaded with valid values, even if some channels are unused.

DMA I/O Address Map

Table 40. DMA I/O Addresses for Memory Addresses, Word Counts, and Command/Status Registers

Address (Hex)	Description	Bits	Byte Pointer
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register[1]	00–07	
0082	Channel 3, Page Table Address register[1]	00–07	
0083	Channel 1, Page Table Address register[1]	00–07	
0087	Channel 0, Page Table Address register[1]	00–07	
0089	Channel 6, Page Table Address register[1]	00–07	
008A	Channel 7, Page Table Address register[1]	00–07	
008B	Channel 5, Page Table Address register[1]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

[1] Upper byte of Memory Address register

DMA Registers

All system microprocessor accesses to the DMA registers must be 8-bit I/O instructions. The following table lists the name and size of each DMA register.

Table 41. DMA Registers

Register	Size (Bits)	Number of Registers	Allocation
Memory Address	16	8	1 per channel
Transfer Count	16	8	1 per channel
Page	8	8	1 per channel
Mask	4	2	1 for channels 7–4 1 for channels 3–0
Mode	8	8	1 per channel
Status	8	2	1 for channel 7–4 1 for channel 3–0

Memory Address Register

Each DMA channel has a 16-bit Memory Address register. This register holds the value of the address that is used during DMA transfers. The address is increased or decreased after each transfer, and the intermediate values of the address are stored in this register during the transfer. This register can be accessed by the microprocessor in successive 8-bit bytes. Auto-initialization restores this register to its original value.

The corresponding DMA page register contains the most significant byte of the DMA memory address.

Transfer Count Register

Each DMA channel has a 16-bit Transfer Count register that is loaded by the system microprocessor. The transfer count determines the number of transfers to be executed by the DMA channel before reaching terminal count. The number of transfers is always one more than the count specifies. For example, if the count is 0, the DMA performs one transfer. As the value in the register goes from hex 0000 to FFFF, the DMA channel generates a terminal-count pulse. The system microprocessor reads the Transfer Count register in successive I/O bytes when the DMA controller is in the program condition. Auto-initialization restores the register to its original value.

Mask Register

Each DMA channel has a corresponding mask bit that disables the DMA from servicing the requesting device. Each mask bit can be set or cleared by the system microprocessor. A system reset or DMA master clear operation sets all mask bits to 1. A Clear Mask Register command sets all mask bits to 0. This register can be programmed using the 8237-compatible mode commands.

Table 42. Set/Clear Single Mask Bit, Using 8237-Compatible Mode

Bit	Function
7–3	Reserved (must be set to 0)
2	0 = Clear mask bit 1 = Set mask bit
1, 0	00 = Select channel 0 or 4 01 = Select channel 1 or 5 10 = Select channel 2 or 6 11 = Select channel 3 or 7

Table 43. Write DMA Mask Register, Using 8237-Compatible Mode

Bit	Function
7–4	Reserved (must be set to 0)
3	0 = Clear channel 3 or 7 mask bit 1 = Set channel 3 or 7 mask bit
2	0 = Clear channel 2 or 6 mask bit 1 = Set channel 2 or 6 mask bit
1	0 = Clear channel 1 or 5 mask bit 1 = Set channel 1 or 5 mask bit
0	0 = Clear channel 0 or 4 mask bit 1 = Set channel 0 or 4 mask bit

Mode Register

Each DMA channel has a Mode register that identifies the type of operation that takes place when that channel is activated. The Mode register is programmed by the system microprocessor, and the contents are reformatted and stored internally in the DMA controller. This is a write-only register.

Table 44. 8237-Compatible Mode Register

Bit	Function
7, 6	Reserved (must be set to 0)
5	0 = Increase address 1 = Decrease address
4	0 = Disable auto-initialization 1 = Enable auto-initialization
3, 2	00 = Verify operation 01 = Write operation 10 = Read operation 11 = Reserved
1, 0	00 = Select channel 0 or 4 01 = Select channel 1 or 5 10 = Select channel 2 or 6 11 = Select channel 3 or 7

Status Register

Two Status registers indicate which channels have reached terminal count. Bits 3 through 0 are set to 1 every time a corresponding channel reaches terminal count. All bits are cleared by a reset or after a system microprocessor Status Read command. When these registers are written to, they are Command registers, as shown in Table 46 on page 53.

Table 45. Status Register—Read

Bit	Function
7	Channel 3 or 7 request
6	Channel 2 or 6 request
5	Channel 1 or 5 request
4	Channel 0 request
3	Channel 3 or 7 terminal count
2	Channel 2 or 6 terminal count
1	Channel 1 or 5 terminal count
0	Channel 0 terminal count

Table 46. Command Register—Write

Bit	Function
7	0 = DACK is active low 1 = DACK is active high
6	0 = DRQ is active high 1 = DRQ is active low
5	0 = Late write 1 = Extended write
4	0 = Fixed priority 1 = Rotating priority
3	0 = Normal timing 1 = Compressed timing
2	0 = Enable controller 1 = Disable controller
1	Reserved
0	Reserved (must be set to 0)

The following table shows an example of programming DMA channel 2.

Table 47. DMA Channel 2 Programming Example

Program Step	OUT to	ADDRESS Data
Set channel-mask bit	(000AH)	*x*6H
Clear byte pointer	(000CH)	*xx*H
Write memory address	(0004H)	*xx*H
Write memory address	(0004H)	*xx*H
Write page table address	(0081H)	*xx*H
Clear byte pointer	(000CH)	*xx*H
Write register count	(0005H)	*xx*H
Write register count	(0005H)	*xx*H
Write mode register	(000BH)	*xx*H
Clear channel 2 mask bit	(000AH)	*x*2H

Values inside ( ) are addresses; *x* represents data.

Chapter 6. Interrupt Controller

© Copyright IBM Corp. Februray 1996

Interrupt Controller Description

The system provides 16 levels of system interrupts (including the NMI). Any or all of the interrupts, including the non-maskable interrupt, can be masked. The system board uses the logic equivalent of two Intel 8259A interrupt controllers.

Note: Interrupts on personal computers that have VL/ISA risers are edge-triggered. Interrupts on the personal computers that have PCI risers are level-sensitive.

Interrupt Assignments

The following table shows the interrupt levels and their functions. The interrupt levels are listed in the order of priority. The highest priority is the NMI, and the lowest is IRQ7.

Note: If you install ISA bus (AT-bus) adapters in your system, be sure that no interrupts or DMA channels (see Table 36 on page 47) conflict with existing resources.

Table 48. Interrupt Level Assignments by Priority

Level		Function
NMI		Parity or channel check
IRQ0		Timer
IRQ1		Keyboard
IRQ2		Cascade interrupt requests from IRQ8–IRQ15
	IRQ8	Real-time clock
	IRQ9[1]	Redirect cascade (can be used by ISA or PCI adapters)
	IRQ10	Available (can be used by ISA or PCI adapters)
	IRQ11	Available (can be used by ISA or PCI adapters)
	IRQ12	Mouse port, if enabled (otherwise can be used by ISA or PCI adapters)
	IRQ13	Math coprocessor exception
	IRQ14	Hard disk drive, if enabled (otherwise, can be used by ISA or PCI adapters)
	IRQ15	Hard disk drive 2, if enabled (otherwise, can be used by ISA or PCI adapters)
IRQ3		Serial port 2, if enabled (otherwise, can be used by ISA or PCI adapters)
IRQ4		Serial port 1, if enabled (otherwise, can be used by ISA or PCI adapters)
IRQ5		Available (parallel port 2, or can be used by ISA or PCI adapters)
IRQ6		Diskette, if enabled (otherwise, can be used by ISA or PCI adapters)
IRQ7		Parallel port 1, if enabled (otherwise, can be used by ISA or PCI adapters)

[1] IRQ9 can be used as the vertical retrace interrupt by some software.

Note: In systems with a PCI bus, for IRQ5, IRQ9, IRQ10, and IRQ11, any three of the four available interrupts can be used at one time for AT-bus adapters. The remaining interrupt is used for the PCI bus.

Note: Before programming the interrupt controllers, disable the interrupts by executing a CLI instruction. This includes the Mask register, end of interrupts, initialization control words, and operational control words.

Interrupt Controller Registers

The following tables show the interrupt controller registers and their functions during write and read operations. Before normal operation can begin, the interrupt controller must follow an initialization sequence as shown in the following table.

Table 49. Interrupt Controller Registers—Write

Interrupt Controller 1 Address (Hex)	Interrupt Controller 2 Address (Hex)	Bit 4	Bit 3	Register Function
0020	00A0	1	X	Write Initialization Command Word 1
0021	00A1	X	X	Write Initialization Command Word 2
0021	00A1	X	X	Write Initialization Command Word 3
0021	00A1	X	X	Write Initialization Command Word 4 (if needed)
0021	00A1	X	X	Write Operation Control Word 1
0020	00A0	0	0	Write Operation Control Word 2
0020	00A0	0	1	Write Operation Control Word 3

X = don't care bits

Table 50. Interrupt Controller Registers—Read

Interrupt Controller 1 Address (Hex)	Interrupt Controller 2 Address (Hex)	Register Function
0020	00A0	Interrupt Request register, In-Service register, or Poll command[1]
0021	00A1	Interrupt Mask register

[1] Function depends on how Operation Control Word 3 was set up prior to the read operation.

Chapter 7. System Timers

© Copyright IBM Corp. Februray 1996

System Timers Description

The system has three programmable timers: channel 0, channel 1, and channel 2. These channels are similar to those in the original IBM Personal Computer, IBM Personal Computer XT and the IBM Personal Computer AT. The timers that are used in the IBM personal computer IBM 300 Series are compatible with the Intel 8254. The following is a block diagram of the timers.

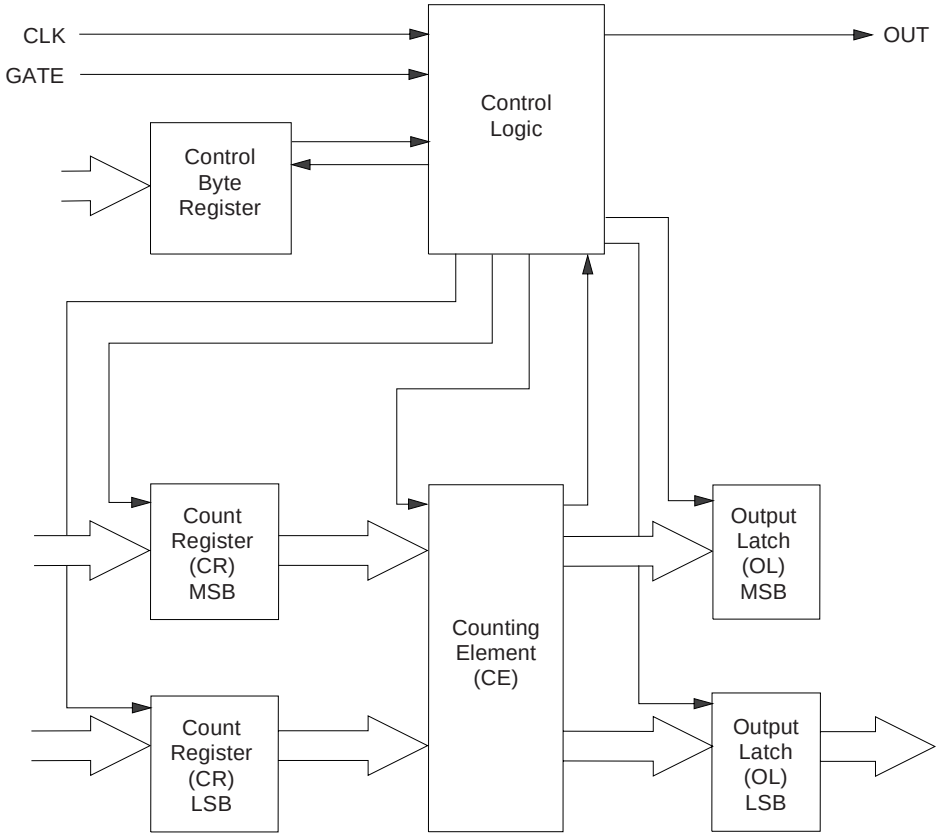


Figure 2. System Timer Block Diagram

Channel 0—System Timer

- GATE 0 is always enabled.
- CLK IN 0 is driven by 1.193 MHz.
- CLK OUT 0 drives the interrupt controller chip, IRQ0.

Channel 1—Refresh Request Generator

- GATE 1 is always enabled.
- CLK IN 1 is driven by 1.193 MHz.
- CLK OUT 1 is request-refresh cycle.

  Note: Channel 1 is programmed as a rate generator to produce a refresh request every 15 microseconds.

Channel 2—Tone Generation for Speaker or Beeper

- GATE 2 is controlled by bit 0 (PPI) of port hex 0061.
- CLK IN 2 is driven by 1.193 MHz.
- CLK OUT 2 is connected to the input port hex 0061, bit 5. CLK OUT 2 is also logically ANDed with port hex 0061, bit 1 to produce the 'speaker data enable' signal. The output of the AND gate is buffered to the system speaker or beeper.

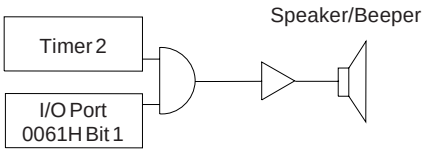


Figure 3. Audio Subsystem Block Diagram

Timers 0, 1, and 2

Each timer is independent. Timers 0, 1, and 2 are 16-bit down counters that can be preset. They can count in binary and binary-coded decimal (BCD).

Programming the System Timers

The system treats the programmable interval timer as an arrangement of four external I/O ports. Three ports are treated as count registers and one as a control register for mode programming. Timers are programmed by writing a control word and then an initial count. Control words are written into the control-word registers, which are located at I/O address hex 0043 for timers 0, 1, and 2. Initial counts are written into the count registers, not the control-word registers. The format of the initial count is determined by the control word that is used.

The count is written to the count register, then transferred to the counting element, according to the mode definition. When the count is read, the data is presented at the output latch.

Counter Write Operations

The control word must be written before the initial count is written, and the count must follow the count format that is specified in the control word. A new initial count can be written to the counters at any time without affecting the programmed mode of the counter. The effect on counting is described in "System Timer Modes" on page 61. The new count must follow the programmed count format.

Counter Read Operations

The counters can be read using the Counter Latch command (see "Counter Latch Command" on page 61).

If the counter is programmed for 2-byte counts, 2 bytes must be read. The 2 bytes need not be read consecutively; read, write, or programming operations of other counters can be inserted between them.

Note: If the counters are programmed to read or write 2-byte counts, the program must finish writing the second byte before transferring control to another routine that reads or writes into the same counter. Otherwise, an incorrect count results.

Registers

Table 51. System Timer/Counter Registers

I/O Address (Hex)	Register
0040	Read/Write Timer/Counter 0
0041	Read/Write Timer/Counter 1
0042	Read/Write Timer/Counter 2
0043	Write Control Byte for Counters 0, 1, or 2

Channel 0 (Hex 0040) and Channel 2 (Hex 0042) Count Registers

Before the count is written to I/O address hex 0040 for channel 0 or hex 0042 for channel 2, the Control byte must be written to address hex 0043, indicating the format of the count (least significant byte only, most significant byte only, or least significant byte followed by most significant byte).

Control Byte Register—Channel 0, 1, or 2 (Hex 0043)

This is a write-only register. Table 52 through Table 55 describe the format of the Control byte (I/O address hex 0043) for counters 0, 1, and 2.

Table 52. SC—Select Counter, I/O Address Hex 0043

Bit 7 SC1	Bit 6 SC0	Function
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Reserved

Table 53. RW—Read/Write Counter, I/O Address Hex 0043

Bit 5 RW1	Bit 4 RW0	Function
0	0	Counter Latch command
0	1	Read/write counter bits 0–7 only
1	0	Read/write counter bits 8–15 only
1	1	Read/write counter bits 0–7 first, then bits 8–15

Table 54. M—Counter Mode, I/O Address Hex 0043

Bit 3 M2	Bit 2 M1	Bit 1 M0	Function
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

Don't care bits (X) should be set to 0.

Table 55. Binary-Coded-Decimal (BCD) Bit

Bit 0 BCD	Function
0	Binary counter (16 bits)
1	Binary-coded-decimal-counter (4 decades)

Counter Latch Command

The Counter Latch command is written to the Control Byte register. The SC0 and SC1 bits select the counter, and bits 5 and 4 distinguish this command from a Control byte. Table 56 on page 61 shows the format of the Counter Latch command.

Table 56. Counter Latch Command

Bit	Function
7	SC1—Specifies the counter to be latched
6	SC0—Specifies the counter to be latched
5, 4	0—Specifies the Counter Latch command
3–0	Reserved (set to 0)

The count is latched into the selected counter output latch when the Counter Latch command is received. This count is held in the latch until it is read by the system microprocessor (or until the counter is reprogrammed). After the count is read by the system microprocessor, it is automatically unlatched, and the output latch resumes following the counting element. Counter Latch commands have no effect on the programmed mode of the counter. All subsequent latch commands that are issued to a given counter before the count is read are ignored. A read cycle to the counter latch returns the value that is latched by the first Counter Latch command.

System Timer Modes

The following terms are used in describing the timer modes:

CLK pulse The rising edge, then the falling edge of the CLK input to a counter.

Trigger The rising edge of the GATE input to a counter.

Counter load The transfer of a count from the counter register to the counting element.

Mode 0—Interrupt on Terminal Count

Event counting can be performed in mode 0. Counting is enabled when GATE is set to 1 and disabled when GATE is set to 0. If GATE is set to 1 when the Control byte and initial count are written to the counter, the sequence for mode 0 is:

1. The Control byte is written to the counter, and OUT goes low.
2. The initial count is written.
3. The initial count is loaded on the next CLK pulse. This CLK pulse does not decremented the count.

   The count is decremented until the counter reaches 0. For an initial count of *n*, the counter reaches 0 after *n*+1 CLK pulses.
4. OUT goes high.

OUT remains high until a new count or new mode 0 Control byte is written into the counter.

If GATE is set to 0 when an initial count is written to the counter, it is loaded on the next CLK pulse even though counting is not enabled. After GATE enables counting, OUT goes high *n* CLK pulses later.

If a new count is written to a counter while it is counting, the count is loaded on the next CLK pulse, and counting continues from the new count. If a 2-byte count is written to the counter, the following occurs:

1. The first byte that is written to the counter disables the counting. OUT goes low immediately, and there is no delay for the CLK pulse.
2. When the second byte is written to the counter, the new count is loaded on the next CLK pulse. OUT goes high when the counter reaches 0.

Mode 1—Hardware Re-triggerable One-Shot

The counter is armed by writing the Control byte and initial count to the counter. When a trigger occurs, the counter is loaded. The sequence for mode 1 is:

1. OUT is high.
2. The Control byte and initial count are written to the counter.
3. On the CLK pulse following a trigger, OUT goes low and begins the one-shot pulse.
4. The count is decremented until the counter reaches 0.
5. OUT goes high.

OUT remains high until the CLK pulse after the next trigger.

For an initial count of *n*, a one-shot pulse is *n* CLK pulses long. The one-shot pulse repeats the same count of *n* for the next triggers. OUT remains low for *n* CLK pulses following any trigger. GATE does not affect OUT. A new count that is written to the counter does not affect the current one-shot pulse unless the counter is re-triggered. If the counter is re-triggered, the new count is loaded, and the one-shot pulse continues.

Note: Mode 1 is valid only on counter 2.

Mode 2—Rate Generator

This mode causes the counter to perform a divide-by-*n* function. Counting is enabled when GATE is set to 1 and disabled when GATE is set to 0. The sequence for mode 2 is:

1. OUT is high.
2. The Control byte and initial count are written to the counter.
3. The initial count is loaded on the next CLK pulse.
4. The count is decremented until the counter reaches 1.
5. OUT goes low for one CLK pulse.
6. OUT goes high.
7. The counter reloads the initial count.
8. The process is repeated.

If GATE goes low during the OUT pulse, OUT goes high. On the next CLK pulse, a trigger reloads the counter with the initial count. OUT goes low *n* CLK pulses after the trigger. This allows the GATE input to be used to synchronize the counter.

OUT goes low *n* CLK pulses after the initial count is written, to allow software synchronization of the counter.

The current counting sequence is not affected by a new count being written to the counter. If the counter receives a trigger after a new count is written and before the end of the current count, the new count is

loaded on the next CLK pulse, and counting continues from the new count. If the counter does not receive the trigger, the new count is loaded following the current counting cycle.

Mode 3—Square Wave

Mode 3 is the same as mode 2 except for the duty cycle of OUT. Counting is enabled when GATE is set to 1 and disabled when GATE is set to 0. An initial count of *n* causes OUT to be a square wave. The period of the square wave is *n* CLK pulses. If OUT is low and GATE goes low, OUT goes high. On the next CLK pulse, a trigger reloads the counter with the initial count.

After a Control byte and the initial count are written, the counter is loaded on the next CLK pulse, to allow software synchronization of the counter.

The current counting sequence is not affected by a new count being written to the counter. If the counter receives a trigger after a new count is written and before the end of the current-count half-cycle of the square wave, the new count is loaded on the next CLK pulse, and counting continues from the new count. If the counter does not receive the trigger, the new count is loaded following the current half-cycle.

Implementations of mode 3 differ, depending on whether the count that is written is an odd or even number. If the count is even, the sequence for mode 3 is:

1. OUT is high.
2. The initial count is loaded on the first CLK pulse.
3. The count is decremented by 2 on succeeding CLK pulses.
4. The count is decremented until the counter reaches 0.
5. OUT changes state.
6. The counter is reloaded with the initial count.
7. The process is repeated indefinitely.

If the count is odd, the sequence for mode 3 is:

1. OUT is high.
2. The initial count minus 1 is loaded on the first CLK pulse.
3. The count is decremented by 2 on succeeding CLK pulses.
4. The count is decremented until the counter reaches 0.
5. One CLK pulse after the count reaches 0, OUT goes low.
6. The counter is reloaded with the initial count minus 1.
7. The count is decremented by 2 on succeeding CLK pulses.
8. The count is decremented until the counter reaches 0.
9. OUT goes high.
10. The process is repeated indefinitely.

Using an odd count, mode 3 causes OUT to go high for a count of (*n*+1)/2 and low for a count of (*n*–1)/2.

Mode 3 can operate such that OUT is initially set low when the Control byte is written. For this condition, the sequence for mode 3 is:

1. OUT is low.
2. The count is decremented to half of the initial count.
3. OUT goes high.
4. The count is decremented until the counter reaches 0.
5. OUT goes low.
6. The process is repeated indefinitely.

This process results in a square wave with a period of *n* CLK pulses.

Note: If OUT must be high after the Control byte is written, the Control byte must be written twice. This applies only to mode 3.

Mode 4—Software Re-triggerable Strobe

Counting is enabled when GATE is set to 1, and disabled when GATE is set to 0. Counting is triggered when an initial count is written. The sequence for mode 4 is:

1. OUT is high.
2. The Control byte and initial count are written to the counter.
3. The initial count is loaded on the next CLK pulse. The count is not decremented by this clock pulse.
4. The count is decremented until the counter reaches 0. For an initial count of *n*, the counter reaches 0 after *n*+1 CLK pulses.
5. OUT goes low for one CLK pulse.
6. OUT goes high.

GATE must not go low for one-half CLK pulse before or after OUT goes low. If this occurs, OUT remains low until GATE is restored to high.

If a new count is written to a counter while it is counting, the count is loaded on the next CLK pulse. Counting then continues from the new count. If a 2-byte count is written, the following occurs:

1. The first byte that is written to the counter does not affect counting.
2. When the second byte is written to the counter, the new count is loaded on the next CLK pulse.

The mode 4 sequence can be re-triggered by software. The period from when the new count of *n* is written to when OUT goes low is *n*+1 CLK pulses.

Mode 5—Hardware Re-triggerable Strobe

Counting is triggered by the rising edge of GATE. The sequence for mode 5 is:

1. OUT is high.
2. The Control byte and initial count are written to the counter. Counting is triggered by the rising edge of GATE.
3. The counter is loaded on the next CLK pulse after the trigger. The count is not decremented by this CLK pulse.
4. The count is decremented until the counter reaches 0.
5. OUT goes low for one CLK pulse. This occurs (*n*+1) pulses after the trigger.
6. OUT goes high.

The counting sequence can be re-triggered. OUT goes low *n*+1 pulses after the trigger. GATE does not affect OUT.

The current counting sequence is not affected by a new count being written to the counter. If the counter receives a trigger after a new count is written and before the end of the current count, the new count is loaded on the next CLK pulse, and counting continues from the new count.

Note: Mode 5 is valid only on counter 2.

Operations Common to All Modes

When Control bytes are written to a counter, the control logic is reset, and OUT goes to a known state. This does not require a CLK pulse.

New counts are loaded and counters are decremented on the falling edge of the CLK pulse.

Counters do not stop when they reach 0. In modes 0, 1, 4, and 5, the counter wraps around to the highest count and continues counting. Modes 2 and 3 are periodic; the counter reloads itself with the initial count and continues from there.

GATE is sampled on the rising edge of the CLK pulse.

Table 57 shows the minimum and maximum initial counts for the counters.

Table 57. Minimum and Maximum Initial Counts, Counters 0 and 2

Mode	Minimum Count	Maximum Count
0	1	0 = 2^{16} (binary counting) or 10^4 (BCD counting)
1	1	0 = 2^{16} (binary counting) or 10^4 (BCD counting)
2	2	0 = 2^{16} (binary counting) or 10^4 (BCD counting)
3	2	0 = 2^{16} (binary counting) or 10^4 (BCD counting)
4	1	0 = 2^{16} (binary counting) or 10^4 (BCD counting)
5	1	0 = 2^{16} (binary counting) or 10^4 (BCD counting)

Chapter 8. Bus Architecture

© Copyright IBM Corp. Februray 1996

Bus Architecture Descriptions

The IBM personal computer IBM 300 Series gives you a choice of bus architectures.

ISA Bus

One of the most widely used and successful bus architectures is the AT bus, also called the *Industry Standard Architecture (ISA) bus*, or the I/O channel. The ISA bus is a 16-bit bus that operates at a speed of 8 MHz. It can transfer up to 8MB of data per second between the microprocessor and an I/O device. Practical performance ranges between 4MB to 8MB per second.

The ISA bus continues to be popular because so many adapters, devices, and applications have been designed and marketed for it. ISA is very adequate for users of DOS applications in a standalone environment, or for DOS network requestors with moderate performance requirements.

Although the ISA bus is widely used and is suitable for many applications, it cannot transfer data fast enough for today's high-speed microprocessors and I/O devices. For example, the ISA bus might not provide the performance needs of video devices and applications with high resolution and high-color content. Also, ISA might not be capable of handling the throughput required by some fast hard disks, network controllers, or full-motion video adapters.

The ISA bus is buffered to provide sufficient power for the 98-pin connectors, assuming two low-power Schottky (LS) loads per slot. The signal assignments and pin assignments for the I/O channel connectors are shown in Figure 1 on page 24.

PCI Bus

The PCI bus, available for all personal computer models, is similar in many ways to the VL bus. Like the VL bus, the PCI bus supplements the standard ISA bus by providing a faster I/O bus (up to 33 MHz with a wider, 32-bit data path). Data transfer rates of up to 132MB per second are also possible.

Unlike the VL bus, which connects directly to the microprocessor local bus, the PCI bus connects through a buffered bridge controller. PCI devices get all their data through the PCI controller. The PCI controller looks at all signals from the microprocessor local bus, then passes them to the ISA or MCA controller, or to peripherals connected to the PCI bus. For more information about the PCI bridge controller, see *82420/82430 PCISet ISA and EISA Bridges*, part number 290483-001 published by Intel Corporation, Santa Clara, CA.

Also unlike the VL bus, the PCI bus is not governed by the speed of the microprocessor. PCI can operate at speeds as fast as 33 MHz, slow down, or even stop if there is no activity on the bus, all independent of the microprocessor's operations. This independence is a distinguishing feature of PCI that allows the microprocessor to do other work while the I/O bus is busy. Microprocessor independence also makes PCI more adaptable to various microprocessor speeds and families, and allows more consistency in the design and use of PCI peripherals across multiple computer families.

The signal assignments and pin assignments for the PCI connectors are shown in Table 21 on page 26. For additional information, see the *PCI Local Bus Specification - Revision 2.0*, dated April 30, 1993, published by the PCI Special Interest Group.

Bus Voltage Levels

Four voltage levels are provided for I/O adapters. The maximum available values (for each slot) are as follows:

- +5 V dc (+5%, –4.5%) at 2.0 A
- –5 V dc (+10%, –9.5%) at 0.100 A
- +12 V dc (+5%, –4.5%) at 0.175 A
- –12 V dc (+10%, –9.5%) at 0.100 A

The I/O CH RDY signal is available on the I/O channel to allow operation with slow I/O or memory devices. I/O CH RDY is held inactive by an addressed device to lengthen the operation. For each clock cycle that the line is held inactive, one wait state is added to the I/O or DMA operation.

Two voltage levels are provided for PCI bus adapters. The maximum available values (for each slot) are as follows:

- +5 V dc (+5%, –4.5%) at 7.576 A
- +3.3 V dc (+5%, –4.5%) at 4.00 A

Appendix A. Error Codes

POST Error Codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages. An *x* in an error message can represent any number.

Table 58. POST Error Messages

Code	Description
101	System Board Failure
102	System Board Failure
106	Diskette Drive Error
161	Bad CMOS Battery
162	Configuration Change has Occurred
163	Date and Time Incorrect
164	Memory Size Error
201	Memory Error
229	Configuration Error (Cache)
301	Keyboard Error
303	Keyboard Error
962	Configuration Error (Parallel Port)
1162	Configuration Error (Serial Port)
1762	Hard Disk Error

Beep Codes

For the following beep codes, the numbers indicate the sequence and number of beeps. For example, a "2-3-2" error symptom (a burst of two beeps, three beeps, then a burst of two beeps) indicates a memory module problem. An *x* in an error message can represent any number.

Table 59. Beep Codes

Beep Code	Probable Cause
4	Video adapter, system board
1-1-3	System board
1-1-4	System board
1-2-*x*	System board
1-3-*x*	Memory module, system board
1-4-4	Keyboard, system board
1-4-*x*	Memory module, system board
2-1-1, 2-1-2	System board
2-1-*x*	Memory module, system board
2-2-2	Video adapter, system board
2-2-*x*	Memory module, system board
2-3-*x*	Memory module, system board
2-4-*x*	Memory module, system board
3-1-*x*	System board
3-2-4	System board, keyboard
3-3-4	Video adapter, system board, display
3-4-1	Video adapter, system board, display
3-3-2	Video adapter, system board
All other beep code sequences	System board

© Copyright IBM Corp. Februray 1996

Appendix B. Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates. Any reference to an IBM product, program, or service is not intended to state or imply that only that IBM product, program, or service may be used. Subject to IBM's valid intellectual property or other legally protectable rights, any functionally equivalent product, program, or service may be used instead of the IBM product, program, or service. The evaluation and verification of operation in conjunction with other products, except those expressly designated by IBM, are the responsibility of the user.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries, in writing, to:

IBM Director of Licensing
IBM Corporation
500 Columbus Avenue
Thornwood, NY 10594
U.S.A.

© Copyright IBM Corp. Februray 1996

Trademarks

The following terms are trademarks of the IBM Corporation in the United States or other countries or both:

AT	Personal Computer AT
IBM	Personal Computer XT
Micro Channel	Personal System/2
OS/2	SelectaSystem

The following terms are trademarks of other companies:

DEC PathWorks	Digital Equipment Corporation
Hercules	Hercules Computer Technology
i386	Intel Corporation
Intel	Intel Corporation
Intel486	Intel Corporation
Matrox	Matrox Electronic Systems, Ltd.
Microsoft	Microsoft Corporation
Motorola	Motorola, Incorporated
MS-DOS	Microsoft Corporation
National Semiconductor	National Semiconductor Corporation
NetWare	Novell, Inc.
Novell	Novell, Inc.
OverDrive	Intel Corporation
PCMCIA	Personal Computer Memory Card International Association
Pentium	Intel Corporation
S3	S3 Incorporated
SCO	The Santa Cruz Operation Incorporated
Solaris	Sun Microsystems Inc.
UnixWare	Novell Inc
VESA	Video Electronics Standards Association
VL bus	Video Electronics Standards Association

Unix is a registered trademark in the United States and other countries licensed exclusively through X/Open Company Limited

Windows is a trademark of Microsoft Corporation

Index

Special Characters

A

B

C

D

© Copyright IBM Corp. Februray 1996

E

F

H

I

J

K

S

T

U

V

W

Part Number: 30H1721

Printed in U.S.A.