Technical Information Manual

PC 300GL Types 6563, 6564, 6574
PC 300PL Type 6565

Note

Before using this information and the product it supports, be sure to read the general information under Appendix E, “Notices and trademarks” on page 41.

First Edition (October 1999)

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Preface

This *Technical Information Manual* provides information for the IBM PC 300®GL personal computer types 6563, 6564, and 6574 and PC 300PL personal computer type 6565. It is intended for developers who want to provide hardware and software products to operate with these IBM computers and provides an in-depth view of how these IBM computers work. Users of this publication should have an understanding of computer architecture and programming concepts.

Related publications

In addition to this manual, the following IBM publications provide information related to the operation of the IBM PC 300GL and PC 300PL personal computer. To order publications in the U.S. and Puerto Rico, call 1-800-879-2755. In other countries, contact an IBM reseller or an IBM marketing representative.

- *PC 300GL and PC 300PL User Guide*
  This publication contains information about configuring, operating, and maintaining the PC 300GL and PC 300PL personal computer, as well as installing new options in the PC 300GL and PC 300PL personal computer. Also included are warranty information, instructions for diagnosing and solving problems, and information on how to obtain help and service.
- *Understanding Your Personal Computer*
  This online document includes general information about using computers and detailed information about the features of the PC 300GL and PC 300PL personal computer.
- *About Your Software*
  This publication (provided only with computers that have IBM-preinstalled software) contains information about the preinstalled software package.
- *Hardware Maintenance Manual*
  This publication contains information for trained service technicians. It is available at http://www.ibm.com/pc/us/cdt/hmm.html on the World Wide Web, and it can also be ordered from IBM. To purchase a copy, see the "Getting Help, Service, and Information" section in *PC 300GL and PC 300PL User Guide*.
- *Compatibility Report*
  This publication contains information about compatible hardware and software for the PC 300GL and PC 300PL personal computer. It is available at http://www.ibm.com/pc/us/cdt on the World Wide Web.
- *Network Administrator's Guide*
  This publication contains information for network administrators who configure and service local area networks (LANs). Look for this publication at http://www.ibm.com/pc/us/cdt on the World Wide Web.

Terminology usage

Attention: The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the term *hex* indicates a hexadecimal number.

When numerical modifiers such as K, M, and G are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System overview

PC 300GL personal computer types 6563, 6564, and 6574 and PC 300PL personal computer type 6565 personal computers are computer systems designed to provide state-of-the-art computing power with room for future growth.

Features

The major features are:

- An Intel Pentium™ III microprocessor with MMX™ technology, streaming single instruction multiple data (SIMD) extensions, and 512 KB L2 cache
- Up to 1 GB of system memory
- Integrated IDE bus master controller, Ultra DMA-66 capable
- EIDE hard disk drive
- System management
  - Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)
  - Wake on LAN® support
  - Desktop Management Interface (DMI) BIOS and DMI software
  - Integrated network protocols
  - Enablement for remote administration
  - Ability to update POST and BIOS over the network
  - Wake on Ring support
  - Automatic power-on startup
  - System Management (SM) BIOS and software
  - Ability to store POST hardware test results
  - Selectable startup sequence
  - Selectable Automatic Power On Startup Sequence
  - CMOS Save/Restore utility program
  - CMOS setup over LAN
- IDE CD-ROM[1] drive, standard on some models
- Asset security
  - Security settings provided by the Configuration/Setup Utility program
    - Power-on and administrator password protection
    - Startup sequence control
    - Hard disk drive and diskette drive access control
    - I/O port control
  - Cover lock loop
  - Cover key lock (PC 300PL models only)
  - U-bolt and security cabling (optional)
  - Operating system security
  - Diskette write-protection
  - Alert on LAN™ support

[1] Variable read rate. Actual playback speed will vary and is often less than the maximum possible.

- Accelerated graphics port (AGP) video adapter with up to 16 MB of Synchronous Graphics Random Access Memory
- Integrated 16-bit audio controller and built-in high quality speaker (supports SoundBlaster, Adlib, and Microsoft® Windows® Sound System applications)
- Networking
  - IBM 10/100 megabits-per-second (Mbps) PCI Ethernet adapter with Wake on LAN in some models
  - IBM PCI token ring adapter with Wake on LAN support (optional).
- Expansion: four drive bays, three PCI expansion slots
- PCI I/O bus compatibility
- EnergyStar compliance (some models only)
- 3.5-inch, 1.44 MB diskette drive
- Input/output features
  - One 25-pin, ECP/EPP parallel port
  - Two 9-pin, 16550 universal asynchronous receiver/transmitter (UART) serial ports
  - Two 4-pin, Universal Serial Bus (USB) ports
  - One 6-pin, keyboard port (Windows 95 compatible)
  - One 6-pin, mouse port
  - One 15-pin, DDC2B-compliant monitor port on AGP adapter
  - Three 3.5-mm audio jacks (line/headphone out, line in, microphone)

Wake on LAN

The power supply of the computer supports the Wake on LAN feature. With the Wake on LAN feature, the computer can be turned on when a specific LAN frame is passed to the computer over the LAN.

To use the Wake on LAN feature, the computer must be equipped with a network adapter that supports Wake on LAN. Some models come with a network adapter that supports Wake on LAN.

You can find the menu used for setting the Wake on LAN feature in the Configuration/Setup Utility program.

Wake on Ring

All models can be configured to turn on the computer after a ring is detected from an external or internal modem. The menu for setting the Wake on Ring feature is in the Configuration/Setup Utility program. Two options control this feature:

- **Serial Ring Detect:** Use this option if the computer has an external modem connected to the serial port.
- **Modem Ring Detect:** Use this option if the computer has an internal modem.

Chapter 2. System board features

This section includes information about system board features. For an illustration of the system board, see 10.

Pentium III microprocessor with MMX technology

PC 300GL personal computer types 6563, 6564, and 6574 and PC 300PL personal computer type 6565 come with an Intel Pentium III microprocessor. The microprocessor has an attached heat sink, plugs directly into a connector on the system board.

More information on this microprocessor is available at http://www.intel.com on the World Wide Web.

Features

The features of this microprocessor are as follows:

- Optimization for 32-bit software
- Operation at a low voltage level
- 64-bit microprocessor data bus
- 100 or 133 MHz front-side bus (FSB)
- Up to 512 KB L2 cache integrated into the microprocessor operating at half core speed
  - 4-way set associative
  - Nonblocking
- 32-bit microprocessor address bus
- Math coprocessor
- MMX technology, which boosts the processing of graphic, video, and audio data

L2 cache

The Pentium III microprocessor provides up to 512 KB L2 cache. The L2 cache ECC function is automatically enabled if ECC memory is installed. If nonparity memory is installed, the L2 cache ECC is disabled. (For information on overriding ECC settings, see Chapter 4, Configuration/Setup Utility program, in *PC 300GL and PC 300PL User Guide*.)

Chip set control

The AGP 4X/133 chip set design liscenced from Via Technologies, Inc. is the interface between the microprocessor and the following:

- Memory subsystem
- PCI bus
- IDE bus master connection
- High-performance, PCI-to-ISA bridge
- USB ports
- SMBus
- Enhanced DMA controller
- Real-time clock (RTC)

System memory

The system memory interface is controlled by the AGP 4X/133 chip set design liscenced from Via Technologies, Inc.. Synchronous dynamic random access memory (SDRAM) is standard.

The maximum amount of system memory is 1 GB. For memory expansion, the system board provides two dual inline memory module (DIMM) connectors and supports 133 MHz DIMMs in sizes of 64 MB, 128 MB, 256 MB, and 512 MB. 100 MHz DIMMs may be used in systems with 100 MHz FSB. The amount of memory that is preinstalled varies by model.

The following information applies to system memory:

- SDRAM, nonparity memory is standard.
- The maximum height of memory modules is 6.35 cm (2.5 in.).
- Only PC 100 and PC 133 industry-standard, gold-lead DIMMs are supported.
- The PC 300GL supports error correcting code (ECC). A mix of ECC and nonparity types configures as nonparity.
- Auto-configure, auto-detect maximum system memory, using serial presence detect and configuration interface (BIOS specific).

For information on the pin assignments for the memory module connectors, see “Memory connectors” on page 25.

The following figure shows some possible configurations for the supported DIMMs.

Note: Values in the following table are represented in megabytes (MB).

Figure 1. Memory configurations

Total memory (MB)	Mem 0	Mem 1
64	64	0
96	64	32
128	64	64
128	128	0
160	128	32
192	128	64
256	128	128
384	256	128
512	256	256
512	512	0
578	512	64
640	512	128
1024	512	512

PCI bus

The fully synchronous 33 MHz PCI bus originates in the chip set. Features of the PCI bus are:

- Integrated arbiter with multitransaction PCI arbitration acceleration hooks
- Zero-wait-state, microprocessor-to-PCI write interface for high-performance graphics
- Built-in PCI bus arbiter with support for up to five masters
- Microprocessor-to-PCI memory write posting with 5-Dword-deep buffers
- Conversion of back-to-back sequential microprocessor-to-PCI memory write to PCI burst write

- PCI-to-DRAM posting 18 Dwords
- PCI-to-DRAM up to 100+ MB/sec bandwidth
- PCI 2.1 compliant with V_{aux} and SMBus support
- Delayed transaction
- PCI parity checking and generation support

IDE bus master interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions*.

The bus master for the IDE interface is integrated into the I/O hub of the AGP 4X/133 chipset. The chip set is PCI 2.1 compliant. It connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and IDE bus. The chip set is capable of supporting PIO mode 0–4 devices and IDE DMA mode 0–3 devices. Ultra DMA 66 transfers up to 66 Mbytes/second using ATA 66 cable.

The IDE devices receive their power through a four-position power cable containing +5, +12, and ground voltage. When devices are added to the IDE interface, one device is designated as the master device and another is designated as the slave or subordinate device. These designations are determined by switches or jumpers on each device. There are two IDE ports, one designated Primary and the other Secondary, allowing for up to four devices to be attached. The total number of physical IDE devices is determined by the mechanical package.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see “Input/output address map” on page 35 and Figure 34 on page 39 (for IRQ assignments).

Two connectors are provided on the riser for the IDE interface. For information on the connector pin assignments, see “IDE connectors” on page 31.

USB interface

Universal Serial Bus (USB) technology is a standard feature of the computer. The system board provides the USB interface with two connectors integrated into the the chip set. A USB-enabled device can attach to a connector, and if that device is a hub, multiple peripheral devices can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 MB/sec with a maximum of 127 peripheral devices. The USB is compliant with Universal Host Controller Interface Guide 1.0.

Features provided by USB technology include:

- Support for hot-pluggable devices
- Support for concurrent operation of multiple devices
- Suitability for different device bandwidths
- Support for up to five meters length from host to hub or from hub to hub
- Guaranteed bandwidth and low latencies appropriate for specific devices
- Wide range of packet sizes
- Limited power to hubs

For information on the connector pin assignments for the USB interface, see “USB port connectors” on page 33.

Video subsystem

The PC 300GL personal computer types 6563, 6564, and 6574 and PC 300PL personal computer type 6565 come with one of the following graphics solutions:

1. S3 Savage4 Accelerated Graphics Port (AGP) 2X adapter with 8 MB 125 MHz SDRAM and a 15-pin VGA connector
2. S3 Savage4 Extreme AGP4X adapter, with 16 MB 166 MHz SGRAM and a DVI-I connector and 15-pin VGA converter.

The Savage4 graphics accelerator supports the following features:

- 128-bit 2D graphics engine
- High-performance 2D/3D video accelerator
- 3D rendering
- Motion video architecture
- High speed memory bus
- Flat panel desktop monitor support
- Full software support
- ACPI and PCI power management
- PCI 2.2 bus support, including bus mastering
- 300 MHz RAMDAC with gamma correction
- I2C serial bus and flash ROM support
- 2.5 V core with 3.3V/5V tolerant I/O
- Hardware and BIOS support for VESA timings and DDC monitor communications

The integrated video subsystem supports all video graphics array (VGA) modes and is compliant with super video graphics array (SVGA) modes and Video Electronics Standards Association (VESA) 1.2. Some enhanced features include:

- Integrated video susbystem on a chip, including 2D, 3D, and a video port
- 66 MHz AGP system bus interface with 2X or 4X mode
- Sideband signaling (some models only)
- Command list bus mastering support for fast 2D performance
- 64-bit, 125 MHz SDRAM or 166 MHz SGRAM interface
- Plug and Play support
- 4 MB dynamic display cache memory
- Advanced Power Management support
- Color space conversion
- Hardware scaling

The integrated graphics memory controller subsystem supports the VESA Display Data Channel (DDC) standard 1.1 and uses DDC1 and DDC2B to determine optimal values during automatic monitor detection.

The video subsystem has the following resource assignments:

Figure 2. Video subsystem resources

Resource	Assignment
ROM	Hex C0000–C7FFF (32KB)
RAM	Hex A0000–BFFFF (standard VGA frame buffer)
I/O	VGA, Sequencer, CRT controller, graphics controller, attribute, RAMDAC, extended sequencer, extended CRTC Registers
IRQ	PCI interrupt #1 (enabled by default in the Configuration/Setup Utility program. Normally assigned to IRQ 0Bh when nothing else is installed in the system. The interrupt is used by 3D applications)
DMA	None, NA for AGP bus

For further information on resource assignments, see Appendix B, “System address maps” on page 35 and Appendix C, “IRQ and DMA channel assignments” on page 39.

The PC 300GL personal computer types 6563, 6564, and 6574 and &pctype01.supports the following video subsystem modes:

Figure 3. Supported VGA video modes

Mode (hex)	Display mode	Screen resolution	Colors	Buffer start (hex)	Dot clock (MHz)	Sweep rate (kHz)	Refresh rate (Hz)
00	Text	40 x 25 characters	2	B8000	28.322	31.5	70
01	Text	40 x 25 characters	16	B8000	28.322	31.5	70
02	Text	80 x 25 characters	Black/white	B8000	28.322	31.5	70
03	Text	80 x 25 characters	16	B8000	28.322	31.5	70
04	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
05	Graphics	320 x 200 pixels	4	B8000	25.175	31.5	70
06	Text	640 x 200 pixels	2	B8000	25.175	31.5	70
07	Text	80 x 25 characters	Mono	B0000	28.322	31.5	70
0D	Graphics	320 x 200 pixels	16	A0000	25.175	31.5	70
0E	Graphics	640 x 200 pixels	16	A0000	25.175	31.5	70
0F	Graphics	640 x 350 pixels	Mono	A0000	25.175	31.5	70
10	Graphics	640 x 350 pixels	16	A0000	25.175	31.5	70
11	Graphics	640 x 480 pixels	2	A0000	25.175	31.5	60
12	Graphics	640 x 480 pixels	16	A0000	25.175	31.5	60
13	Graphics	320 x 200 pixels	256	A0000	25.175	31.5	70

The video subsystem provides a 15-pin monitor connector on the system board. For information on connector pin assignments, see Appendix A, “Connector pin assignments” on page 24.

Audio subsystem

PC 300GL and PC 300PL personal computers come with an integrated audio controller. These models, which are capable of playing and recording sounds, support SoundBlaster, Adlib, and Microsoft Windows Sound System applications.

The device drivers for the preinstalled audio adapter are on the hard disk. The device drivers are also available on the *Product Recovery* CD provided with models that come with preinstalled software.

If you connect an optional device to the audio adapter, follow the instructions provided by the manufacturer. (Note that device drivers might be required. If necessary, contact the manufacturer for information on these device drivers.)

The following connectors are available on the audio adapter or integrated audio controller:

- *Line Out* port for connecting powered speakers or headphones. You must connect a set of speakers to the Line Out port to hear audio from the adapter. These speakers must be powered with a built-in amplifier. In general, any powered speakers designed for use with personal computers can be used with the audio adapter. These speakers are available with a wide range of features and power outputs.
- *Line In* port for connecting musical devices, such as a portable CD-ROM player or stereo.
- *Microphone* for connecting a microphone.

Integrated peripheral controller

Control of the integrated input/output (I/O) and diskette drive controllers is provided by a single module, the Integrated peripheral controller (SMC FDC 87B813). This module, which supports Plug and Play, controls the following features:

- Diskette drive interface
- Serial port
- Parallel port
- Keyboard and mouse ports

Diskette drive interface

PC 300GL and PC 300PL personal computers have four drive bays for installing internal devices. The following is a list of devices that the diskette drive subsystem supports:

- 1.44 MB, 3.5 inch diskette drive
- 1.44 MB, 3.5 inch, 3-mode drive for Japan (no BIOS support for 3-mode drive)
- 1.2 MB, 5.25 inch diskette drive
- 1 Mbps, 500 Kbps, or 250 Kbps internal tape drive

One connector is provided on the system board for diskette drive support. For information on the connector pin assignments, see “Diskette drive connector” on page 32.

Serial ports

Two universal asynchronous receiver/transmitter (UART) serial ports are integrated into the system board. The serial ports include 16-byte data, first-in first-out (FIFO) buffers and have programmable baud rate generators. The serial ports are NS16450 and PC16550A compatible.

For information on the connector pin assignments, see “Serial port connector” on page 34.

Note: Current loop interface is not supported.

The following figure shows the serial port assignments in the configuration.

Figure 4. Serial port assignments

Port assignment	Address range (hex)	IRQ level
Serial 1	03F8–03FF	IRQ4
Serial 2	02F8–02FF	IRQ3
Serial 3	03E8–03FF	IRQ4
Serial 4	02E8–02FF	IRQ3

The default setting for the serial port is COM1.

Parallel port

Integrated in the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility program with the default mode set to SPP. The ECP and EPP modes are compliant with IEEE 1284.

The following figure shows the parallel port assignments used in the configuration.

Figure 5. Parallel port assignments

Port assignment	Address range (hex)	IRQ level
Parallel 1	03BC–03BE	IRQ7
Parallel 2	0378–037F	IRQ5
Parallel 3	0278–027F	IRQ5

The default setting for the parallel port is Parallel 1.

The system board has one connector for the parallel port. For information on the connector pin assignments, see “Parallel port connector” on page 34.

Keyboard and mouse ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller; it is compatible with 8042AH. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices: one controls the keyboard and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on the addresses of the keyboard for operation. For the keyboard and mouse interfaces, no resource assignments are given in the system memory addresses or DMA channels. For information on the resource assignments, see “Input/output address map” on page 35 and Figure 34 on page 39 (for IRQ assignments).

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see “Mouse and keyboard port connectors” on page 33.

Network connection

Some PC 300GL and PC 300PL models are equipped with an Ethernet or token ring adapter that supports the Wake on LAN feature.

Features of the optional Ethernet adapter are:

- Operates in shared 10BASE-T or 100BASE-TX environment
- Transmits and receives data at 10 Mbps or 100 Mbps
- Has a RJ-45 connector for LAN attachment
- Operates in symmetrical multiprocessing (SMP) environments
- Supports Wake on LAN
- Supports Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)

Features of the optional token ring adapter are:

- Transmits and receives data at 4 Mbps or 16 Mbps
- Has a RJ-45 and D-shell connectors for LAN attachment
- Supports Wake on LAN
- Supports Remote Program Load (RPL) and Dynamic Host Configuration Protocol (DHCP)

Real-time clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by an external battery source of 3 V dc.

The system uses 242 bytes of complementary metal-oxide semiconductor (CMOS) memory to store data. Moving a jumper on the system board erases CMOS memory.

To locate the battery, see 10.

Flash EEPROM

The system board uses a 2 Mbit of flash electrically erasable, programmable, read-only memory (EEPROM) to store the basic input/output system (BIOS), video BIOS, IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a stand-alone utility program that is available on a 3.5-inch diskette that you can download from the IBM Web site: htt://www.pc.ibm.com/.

Expansion adapters

Each PCI-expansion connector is a 32-bit slot. PCI-expansion connectors support the 32-bit 5 V dc, local-bus signalling environment that is defined in *PCI Local Bus Specification 2.1*.

PC 300GL personal computer types 6563, 6564, and 6574 and PC 300PL personal computer type 6565 personal computers have three PCI slots to support the addition of adapters. For information on installing adapters, see *PC 300GL and PC 300PL User Guide*.

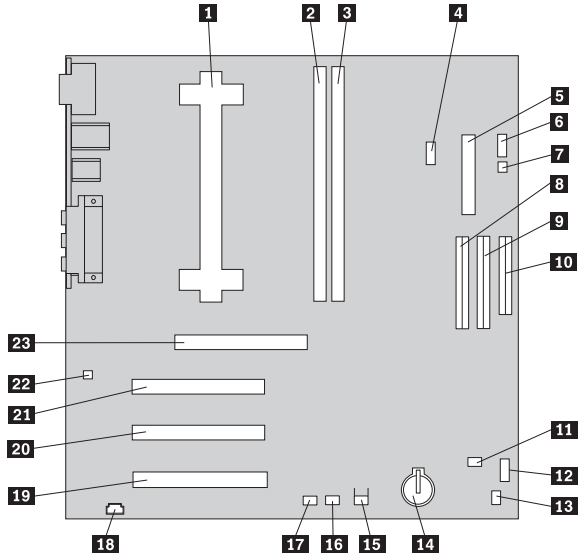
For information on the connector pin assignments, see “PCI connectors” on page 29.

Physical layout

The system board might look slightly different from the one shown.

Note: A diagram of the system board, including switch and jumper settings, is attached to the underside of the computer cover.

1 Microprocessor
2 DIMM 0
3 DIMM 1
4 Fan connector
5 Power connector
6 Switch/LED connector
7 RFID connector (some models only)
8 Primary EIDE connector
9 Secondary EIDE connector
10 Diskette drive connector
11 Fan connector
12 Large rocker switch (not on all models)
13 Small rocker switch
14 Battery
15 Tamper detect switch (some models only)
16 Wake on LAN connector
17 Alert on LAN connector
18 CD-ROM connector
19 PCI adapter slot 1
20 PCI adapter slot 2
21 PCI adapter slot 3 (use this slot for an Alert on LAN adapter)
22 Chassis speaker connector
23 AGP adapter slot



Rocker switches

The two rocker switches on the system board are used for custom configurations. For the location of the small and large rocker switches, see the 10, above.

The large rocker switch has eight switches on it for setting microprocessor speeds for compatibility with the system board.

The following table shows the rocker switch settings for microprocessor speed compatibility with the system board:

Figure 6. Microprocessor switch settings

Microprocessor speed	1	2	3	4	5	6	7	8
100 MHz 150 MHz 200 MHz	Off	Off	On	Off	Off	Off	Off	Off
133 MHz 200 MHz 266 MHz	On	On	On	On	Off	Off	Off	Off
133 MHz 200 MHz 266 MHz	Off	Off	Off	Off	Off	Off	Off	Off
166 MHz 250 MHz 333 MHz	On	On	On	Off	Off	Off	Off	Off
200 MHz 300 MHz 400 MHz	On	On	Off	On	Off	Off	Off	Off
233 MHz 350 MHz 466 MHz	On	On	Off	Off	Off	Off	Off	Off
266 MHz 400 MHz 533 MHz	On	Off	On	On	Off	Off	Off	Off
300 MHz 450 MHz 600 MHz	On	Off	On	Off	Off	Off	Off	Off
333 MHz 500 MHz 666 MHz	On	Off	Off	On	Off	Off	Off	Off
366 MHz 550 MHz 733 MHz	On	Off	Off	Off	Off	Off	Off	Off
400 MHz 600 MHz 800 MHz	Off	On	On	On	Off	Off	Off	Off
433 MHz 650 MHz 866 MHz	Off	On	On	Off	Off	Off	Off	Off
466 MHz 700 MHz 933 MHz	Off	On	Off	On	Off	Off	Off	Off
500 MHz 750 MHz 1000 MHz	Off	On	Off	Off	Off	Off	Off	Off
533 MHz 800 MHz 1066 MHz	Off	Off	On	On	Off	Off	Off	Off
Reserved	Off	Off	Off	On	Off	Off	Off	Off

The small rocker switch has three functions. By moving switch 1 to the On position, you activate the diskette write-protect feature. For more information, see *PC 300GL and PC 300PL User Guide*. By

moving switch 2 to the on position, you clear the CMOS. This rocker switch is also used for flash recovery. See *PC 300GL and PC 300PL User Guide* for instructions.

Function	On
Diskette write-protect	Switch 1
Clear CMOS	Switch 2

Cable connectors

Connections for attaching devices are provided on the back of the computer. The connectors are:

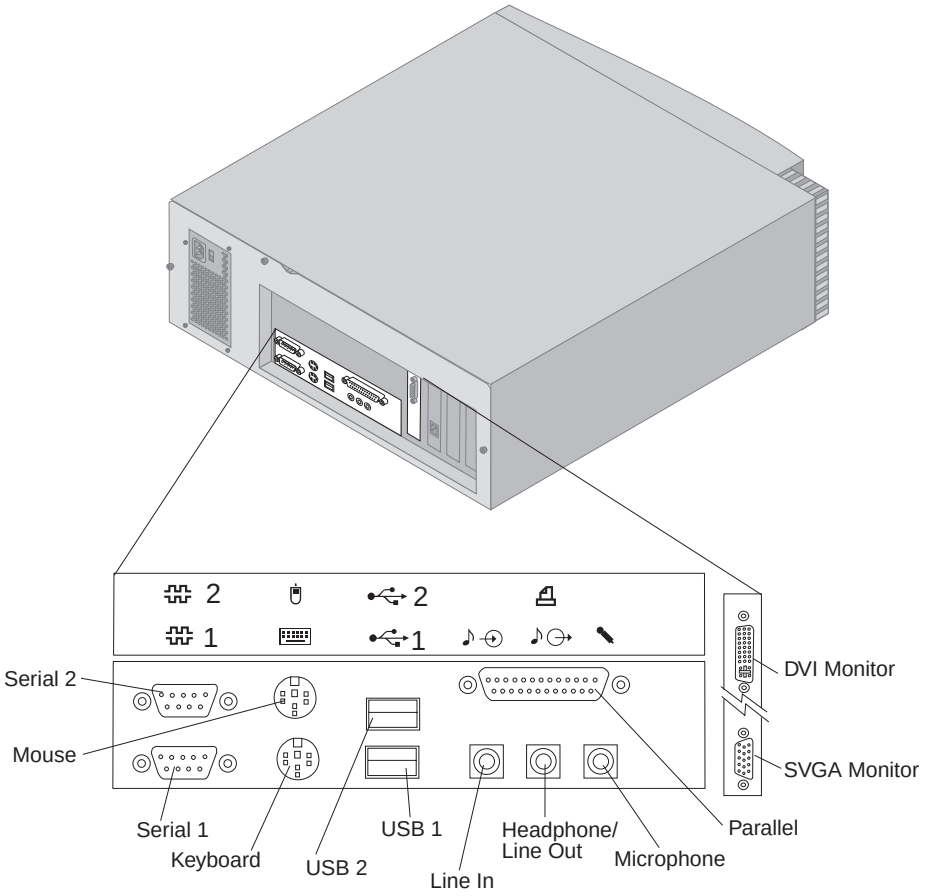
- USB (2)
- Mouse
- Keyboard
- Serial
- Parallel
- Monitor
- Some models only: Ethernet adapter with an RJ-45 connector
- Integrated audio controller with line in, line out, and microphone connectors

Connector panel

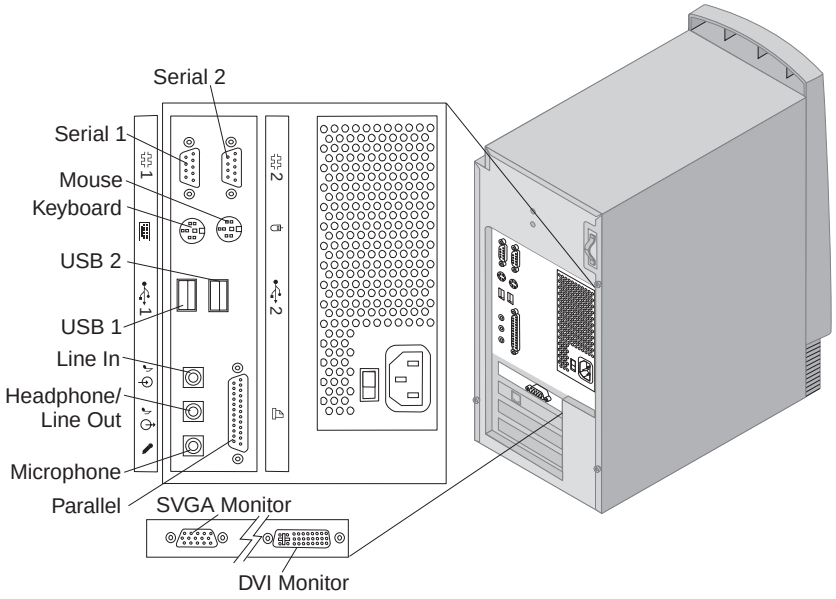
Each connectors for a feature that is integrated into the system board can be identified by a symbol directly below the connector. A connector provided by an adapter might not have an identifying symbol.

For pin-out details on connectors, see Appendix A, “Connector pin assignments” on page 24.

The following illustration shows the connector panel for the desktop model:



The following illustration shows the connector panel for the tower model:



Chapter 3. Physical specifications

This section lists the physical specifications for the PC 300GL personal computer types 6563, 6564, and 6574. The PC 300GL and PC 300PL has four expansion slots and four drive bays.

Note: The PC 300GL and PC 300PL computers comply with FCC Class B.

PC 300GL — desktop

Dimensions

- Height: 138 mm (5.43 in.)
- Width: 400 mm (15.75 in.)
- Depth: 429 mm (16.9 in.)

Weight

- Minimum configuration as shipped: 9.53 kg (21 lb)
- Maximum configuration: 10.4 kg (23 lb)

Environment

- Air temperature:
  - System on: 10° to 35°C (50° to 95°F)
  - System off: 10° to 43°C (50° to 110°F)
- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%
- Maximum altitude: 2134 m (7000 ft), the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

Electrical input

- Input voltage:
  - Low range:
    - Minimum: 90 V ac
    - Maximum: 137 V ac
    - Input frequency range: 57-63 Hz
    - Voltage switch setting: 115 V ac
  - High range:
    - Minimum: 180 V ac
    - Maximum: 265 V ac
    - Input frequency range: 47-53 Hz
    - Voltage switch setting: 230 V ac
  - Input kilovolt-amperes (kVA) (approximately):
    - Minimum configuration as shipped: 0.08 kVA
    - Maximum configuration: 0.51 kVA

Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power-management optional features in use.

Heat output

- Approximate heat output in British thermal units (Btu) per hour:
  - Minimum configuration: 256 Btu/hr (75 watts)
  - Maximum configuration: 706 Btu/hr (207 watts)

Airflow

- Approximately 0.5 cubic meter per minute (18 cubic feet per minute)

Acoustical noise-emission values

- Average sound-pressure levels:
  - At operator position:
    - Idle: 33 dBA
    - Operating: 39 dBA
  - At bystander position–1 meter (3.3 ft):
    - Idle: 30 dBA
    - Operating: 34 dBA
- Declared (upper limit) sound power levels:
  - Idle: 4.4 bels
  - Operating: 4.9 bels

Note: These levels were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779, and are reported in accordance with ISO 9296. Actual sound-pressure levels in your location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound power levels indicate an upper limit, below which a large number of computers will operate.

PC 300GL — tower

Dimensions

- Height: 378 mm (14.9 in.)
- Width: 192 mm (7.6 in.)
- Depth: 383 mm (15.1 in.)

Weight

- Minimum configuration as shipped: 8.30 kg (18.3 lb)
- Maximum configuration: 10.2 kg (22.5 lb)

Environment

- Air temperature:
  - System on: 10° to 35°C (50° to 95°F)
  - System off: 10° to 43°C (50° to 110°F)
- Humidity:
  - System on: 8% to 80%
  - System off: 8% to 80%
- Maximum altitude: 2134 m (7000 ft), the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.

Electrical input

- Input voltage:
  - Low range:
    - Minimum: 90 V ac
    - Maximum: 137 V ac
    - Input frequency range: 57-63 Hz
    - Voltage switch setting: 115 V ac
  - High range:
    - Minimum: 180 V ac
    - Maximum: 265 V ac
    - Input frequency range: 47-53 Hz
    - Voltage switch setting: 230 V ac
  - Input kilovolt-amperes (kVA) (approximate):
    - Minimum configuration as shipped: 0.08 kVA
    - Maximum configuration: 0.51 kVA

Note: Power consumption and heat output vary depending on the number and type of optional features installed and the power-management optional features in use.

Heat output

- Approximate heat output in British thermal units (Btu) per hour:
  - Minimum configuration: 256 Btu/hr (75 watts)
  - Maximum configuration: 706 Btu/hr (207 watts)

Airflow

- Approximately 0.5 cubic meter per minute (18 cubic feet per minute)

Acoustical noise-emission values

- Average sound-pressure levels:
  - At operator position:
    - Idle: 33 dBA
    - Operating: 40 dBA
  - At bystander position–1 meter (3.3 ft):
    - Idle: 30 dBA
    - Operating: 34 dBA
  - Declared (upper limit) sound-power levels:
    - Idle: 4.4 bels
    - Operating: 4.9 bels

Note: These levels were measured in controlled acoustical environments according to procedures specified by the American National Standards Institute (ANSI) S12.10 and ISO 7779, and are reported in accordance with ISO 9296. Actual sound-pressure levels in your location might exceed the average values stated because of room reflections and other nearby noise sources. The declared sound power levels indicate an upper limit, below which a large number of computers will operate.

Note: PC 300GL computers do not support ISA expansion adapters or the IBM PCMCIA adapter for PCI.

Cabling requirements for Wake on LAN adapters

The PC 300GL personal computer has a 3-pin header on the system board that provides the AUX5 (auxiliary 5 volts) and wake-up signal connections. Newer Wake on LAN adapters have a single 3-pin header that connects to the 3-pin header on the system board. Some Wake on LAN adapters have two headers: a 3-pin, right-angle header for AUX5 , and a 2-pin straight header for the wake-up signal. These Wake on LAN adapter options include a Y-cable that has a 3-pin system board connector on one end and splits into the 3-pin and 2-pin connectors to the adapter.

Chapter 4. Power supply

The power supply requirements are supplied by a 145-watt power supply. The power supply provides 3.3-volt power for the Pentium III microprocessor and core chip set and 5-volt power for PCI adapters. Also included is an auxiliary 5-volt (AUX 5) supply to provide power to power management circuitry and a Wake on LAN adapter. The power supply converts the ac input voltage into four dc output voltages and provides power for the following:

- System board
- Adapters
- Internal drives
- Keyboard and auxiliary devices
- USB devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

The power supply connects to the system board with a 2 x 10 connector.

Power input

The following figure shows the power input-specifications. The power supply has a manual switch to select the correct input voltage.

Figure 7. Power-input requirements

Specification	Measurements
Input voltage, low range	100 (min) to 127 (max) V ac
Input voltage, high range	200 (min) to 240 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power output

The power supply outputs shown in the following figures include the current supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Figure 8. Power output (145 watts)

Output voltage	Regulation	Minimum current	Maximum current
+5 volts	+5% to –5%	1.5 A	18.0 A
+12 volts	+5% to –5%	0.02 A	4.2 A
–12 volts	+10% to –10%	0.0 A	0.4 A
+3.3 volts	+5% to –5%	0.0 A	10.0 A
+5 volt (auxiliary)	+5% to –5%	0.0 A	0.720 A

The total combined 3.3 V and 5 V power must not exceed 100 watts.

Component outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Figure 9. System board

Supply voltage	Maximum current	Regulation limits
+3.3 V dc	5000 mA	+5.0% to –5.0%
+5.0 V dc	6000 mA	+5.0% to –4.0%
+12.0 V dc	25.0 mA	+5.0% to –5.0%
–12.0 V dc	25.0 mA	+10.0% to –9.0%

Figure 10. Keyboard port

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	275 mA	+5.0% to –4.0%

Figure 11. Auxiliary device port

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	300 mA	+5.0% to –4.0%

Figure 12. PCI-bus adapters (per slot)

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	1000 mA	+5.0% to –4.0%
+3.3 V dc	1500 mA	+5.0% to –4.0%

Note: For each PCI connector, the maximum power consumption is rated at 5 watts for +5 V dc and +3.3 V dc combined. If maximum power is used, then the overall system configuration will be limited in performance.

Figure 13. USB port

Supply voltage	Maximum current	Regulation limits
+5.0 V DC	500 mA	+5.0% to –4.0%

Figure 14. Internal DASD

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	1400 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA at startup, 400 mA when active	+5.0% to –5.0%

Figure 15. Video port pin 9

Supply voltage	Maximum current	Regulation limits
+5.0 V dc	1100mA	+5.0% to – 5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output protection

The power supply protects against output overcurrent, overvoltage, and short circuits. See the power supply specifications on the previous pages for details.

A short circuit that is placed on any dc output (between outputs or between an output and DC return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all DC outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector description

The power supply for the PC 300GL and PC 300PL personal computer has four, 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in “Component outputs” on page 18. For connector pin assignments, see Appendix A, “Connector pin assignments” on page 24.

Chapter 5. System software

This section briefly describes some of the system software included with the computer.

BIOS

The computer uses the IBM basic input/output system (BIOS), which is stored in flash electrically erasable programmable read-only memory (EEPROM). Some features of the BIOS are:

- PCI support according to PCI BIOS Specification 2.1
- Microsoft PCI IRQ Routing Table
- Plug and Play support according to Plug and Play BIOS Specification 1.1a
- Advanced Power Management (APM) support according to APM BIOS Interface Specification 1.2
- Wake on LAN support
- Wake on Ring support
- Remote Initial Program Load (RIPL) and Dynamic Host Configuration Protocol (DHCP)
- Flash-over-LAN support
- Alternate startup sequence
- IBM Look and Feel – such as screen arrangements and user interface
- ACPI (Advanced Configuration and Power Interfaces)
- IDE Logical block addressing (LBA support)
- LSA 2.0 support
- Bootable CD ROM support
- LS120 support
- DM BIOS 2.1 (DMI 2.0 compliant)
- PC99 compliance

Plug and Play

Support for Plug and Play conforms to the following:

- Plug and Play BIOS Specification 1.1a and 1.0
- Plug and Play BIOS Extension Design Guide 1.0
- Plug and Play BIOS Specification, Errata, and Clarifications 1.0
- Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2
- Plug and Play Kit for DOS and Windows

POST

IBM power-on self-test (POST) code is used. Also, initialization code is included for the on-board system devices and controllers.

POST error codes include text messages for determining the cause of an error. For more information, see Appendix D, “Error codes” on page 40.

Configuration/Setup Utility program

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, and power management.

More information on using the Configuration/Setup Utility program is provided in *PC 300GL and PC 300PL User Guide*.

Advanced Power Management (APM)

The PC 300GL computers come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.2. This enables the system to enter a power-managed state, which reduces the power drawn from the AC electrical outlet. Advanced Power Management is enabled through the Configuration/Setup Utility program and is controlled by the individual operating system.

For more information on APM, see *PC 300GL and PC 300PL User Guide* and *Understanding Your Personal Computer*.

Advanced Configuration and Power Interface (ACPI)

Automatic Configuration and Power Interface (ACPI) BIOS mode enables the operating system to control the power management features of your computer. Not all operating systems support ACPI BIOS mode. Refer to your operating system documentation to determine if ACPI is supported.

Flash update utility program

The flash update utility program is a stand-alone program to support flash updates. This utility program updates the BIOS code and the machine readable information (MRI) to different languages.

The flash update utility program is available on the IBM Web site at http://www.ibm.com/pc/support/ and can be copied to a 3.5-inch diskette.

Diagnostic program

The diagnostic program that comes with PC 300PL and PC 300GL computers is provided as a startable *IBM Enhanced Diagnostic* diskette image on the IBM *Product Recovery* CD or the *Device Driver and IBM Enhanced Diagnostic* CD. It runs independently of the operating system. The user interface for running the diagnostics and utilities is provided by WaterGate Software's PC-Doctor. It can also be downloaded from the following World Wide Web page: http://www.ibm.com/pc/support/. For more information on this diagnostic program, see *PC 300GL and PC 300PL User Guide*.

PC 300GL and PC 300PL computers use the PC-Doctor and IBM Enhanced Diagnostics programs. See *About Your Software* and *PC 300GL and PC 300PL User Guide* for more information.

Chapter 6. System compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues for the computer. Refer to *Compatibility Report* for a list of compatible hardware and software options.

Hardware compatibility

This section discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- Intel 8259 interrupt controllers (edge-triggered mode)
- National Semiconductor NS16450 and NS16550A serial communication controllers
- Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- Intel 8272 or 82077 diskette drive controllers
- Intel 8042 keyboard controller at addresses hex 0060 and hex 0064
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- Parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use this information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware interrupts

Hardware interrupts are level-sensitive for PCI interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay

3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt hex 71) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Hard disk drives and controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-sensitive programs

Programs can select machine specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function (AH)=C0H).

Appendix A. Connector pin assignments

The following figures show the pin assignments for various system board connectors.

SVGA monitor connector

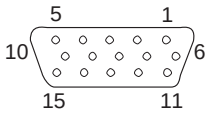


Figure 16. SVGA monitor port connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Red	O	2	Green	O
3	Blue	O	4	Monitor ID 2 - Not used	I
5	Ground	NA	6	Red ground	NA
7	Green ground	NA	8	Blue ground	NA
9	+5 V, used by DDC2B	NA	10	Ground	NA
11	Monitor ID 0 - Not used	I	12	DDC2B serial data	I/O
13	Horizontal sync	O	14	Vertical sync	O
15	DDC2B clock	I/O			

DVI monitor connector

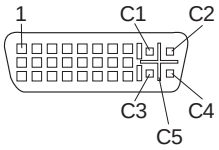


Figure 17. DVI monitor port connector pin assignments - main pin field

Pin	Signal	Pin	Signal
1	TMDS data 2+	2	TMDS data 2–
3	TMDS data 2/4 return	4	TMDS data 4–
5	TMDS data 4+	6	DDC clock
7	DDC data	8	Analog vertical sync
9	TMDS data 1–	10	TMDS data 1+
11	TMDS 1/3 shield	12	TMDS data 3+
13	TMDS data 3+	14	+5V power
15	Ground	16	Hot plug detect
17	TMDS Data 0–	18	TMDS data 0+
19	TMDS data 0–	20	TMDS Data 0/5 shield
21	TMDS data 5+	22	TMDS clock shield
23	TMDS clock+	24	TMDS cloc–

Figure 18. DVI connector pin assignments - micro cross section	
Pin	**Signal**
C1	Red video out
C2	Green video out
C3	Analog blue
C4	Analog horizontal sync
C5[2]	Video/pixel clock return

Memory connectors

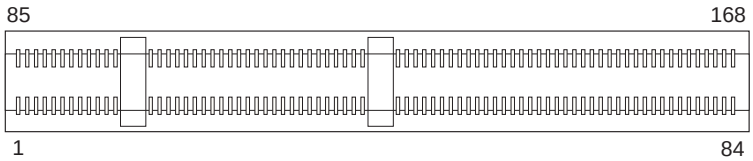


Figure 19 (Page 1 of 3). System Memory Connector Pin Assignments					
Pin	**x64 non-parity**	**x72 ECC**	**Pin**	**x64 non-parity**	**x72 ECC**
1	VSS	VSS	85	VSS	VSS
2	DQ0	DQ0	86	DQ32	DQ32
3	DQ1	DQ1	87	DQ33	DQ33
4	DQ2	DQ2	88	DQ34	DQ34
5	DQ3	DQ3	89	DQ35	DQ35
6	VCC	VCC	90	VCC	VCC
7	DQ4	DQ4	91	DQ36	DQ36
8	DQ5	DQ5	92	DQ37	DQ37
9	DQ6	DQ6	93	DQ38	DQ38
10	DQ7	DQ7	94	DQ39	DQ39
11	DQ8	DQ8	95	DQ40	DQ40
12	VSS	VSS	96	VSS	VSS
13	DQ9	DQ9	97	DQ41	DQ41
14	DQ10	DQ10	98	DQ42	DQ42
15	DQ11	DQ11	99	DQ43	DQ43
16	DQ12	DQ12	100	DQ44	DQ44
17	DQ13	DQ13	101	DQ45	DQ45
18	VCC	VCC	102	VCC	VCC
19	DQ14	DQ14	103	DQ46	DQ46
20	DQ15	DQ15	104	DQ47	DQ47
21	NC	CB0	105	NC	CB4
22	NC	CB1	106	NC	CB5
23	VSS	VSS	107	VSS	VSS

[2] The shield cross at the center of pins C1, C2, C3, and C4.

Figure 19 (Page 2 of 3). System Memory Connector Pin Assignments

Pin	x64 non-parity	x72 ECC	Pin	x64 non-parity	x72 ECC
24	NC	NC	108	NC	NC
25	NC	NC	109	NC	NC
26	VCC	VCC	110	VCC	VCC
27	/WE	/WE0	111	/CAS	/CAS
28	DQMB0	DQMB0	112	DQMB4	DQMB4
29	DQMB1	DQMB1	113	DQMB5	DQMB5
30	/S0	/S0	114	NC	/S1
31	DU	NC	115	/RAS	/RAS
32	VSS	VSS	116	VSS	VSS
33	A0	A0	117	A1	A1
34	A2	A2	118	A3	A3
35	A4	A4	119	A5	A5
36	A6	A6	120	A7	A7
37	A8	A8	121	A9	A9
38	A10/AP	A10/AP	122	BA0	BA0
39	NC	BA1	123	NC	A11
40	VCC	VCC	124	VCC	VCC
41	VCC	VCC	125	CK1	CK1
42	CK0	CK0	126	A12	A12
43	VSS	VSS	127	VSS	VSS
44	DU	NC	128	CKE0	CKE0
45	/S2	/S2	129	NC	/S3
46	DQMB2	DQMB2	130	DQMB6	DQMB6
47	DQMB3	DQMB3	131	DQMB7	DQMB7
48	DU	NC	132	A13	A13
49	VCC	VCC	133	VCC	VCC
50	NC	NC	134	NC	NC
51	NC	NC	135	NC	NC
52	NC	CB2	136	NC	CB6
53	NC	CB3	137	NC	CB7
54	VSS	VSS	138	VSS	VSS
55	DQ16	DQ16	139	DQ48	DQ48
56	DQ17	DQ17	140	DQ49	DQ49
57	DQ18	DQ18	141	DQ50	DQ50
58	DQ19	DQ19	142	DQ51	DQ51
59	VCC	VCC	143	VCC	VCC
60	DQ20	DQ20	144	DQ52	DQ52
61	NC	NC	145	NC	NC
62	NC	NC	146	NC	NC
63	NC	CKE1	147	NC	NC
64	VSS	VSS	148	VSS	VSS
65	DQ21	DQ21	149	DQ53	DQ53
66	DQ22	DQ22	150	DQ54	DQ54

Figure 19 (Page 3 of 3). System Memory Connector Pin Assignments

Pin	x64 non-parity	x72 ECC	Pin	x64 non-parity	x72 ECC
67	DQ23	DQ23	151	DQ55	DQ55
68	VSS	VSS	152	VSS	VSS
69	DQ24	DQ24	153	DQ56	DQ56
70	DQ25	DQ25	154	DQ57	DQ57
71	DQ26	DQ26	155	DQ58	DQ58
72	DQ27	DQ27	156	DQ59	DQ59
73	VCC	VCC	157	VCC	VCC
74	DQ28	DQ28	158	DQ60	DQ60
75	DQ29	DQ29	159	DQ61	DQ61
76	DQ30	DQ30	160	DQ62	DQ62
77	DQ31	DQ31	161	DQ63	DQ63
78	VSS	VSS	162	VSS	VSS
79	CK2	CK2	163	CK3	CK3
80	NC	NC	164	NC	NC
81	NC	NC	165	SA0	SA0
82	SDA	SDA	166	SA1	SA1
83	SCL	SCL	167	SA2	SA2
84	VCC	VCC	168	VCC	VCC

Figure 20 (Page 1 of 3). System memory connector pin input/output

Pin	Signal name	I/O	Pin	Signal name	I/O
1	GND	N/A	85	GND	N/A
2	MD0	I/O	86	MD32	I/O
3	MD1	I/O	87	MD33	I/O
4	MD2	I/O	88	MD34	I/O
5	MD3	I/O	89	MD35	I/O
6	VDD	I/O	90	VDD	N/A
7	MD4	I/O	91	MD36	N/A
8	MD5	I/O	92	MD37	I/O
9	MD6	I/O	93	MD38	I/O
10	MD7	I/O	94	MD39	I/O
11	MD8 (PAR0)	I/O	95	MD40	I/O
12	GND	N/A	96	GND	N/A
13	MD9	I/O	97	MD41	I/O
14	MD10	I/O	98	MD42	I/O
15	MD11	I/O	99	MD43	I/O
16	MD12	I/O	100	MD44	I/O
17	MD13	I/O	101	MD45	I/O
18	VDD	N/A	102	VDD	N/A
19	MD14	I/O	103	MD46	I/O
20	MD15	I/O	104	MD47	I/O
21	NC	I/O	105	NC	I/O
22	NC	I/O	106	NC	I/O

Figure 20 (Page 2 of 3). System memory connector pin input/output

Pin	Signal name	I/O	Pin	Signal name	I/O
23	GND	I/O	107	GND	N/A
24	NC	N/A	108	NC	N/A
25	NC	N/A	109	NC	N/A
26	VDD	N/A	110	VDD	N/A
27	WE#	I	111	CAS#	N/A
28	DQMB0#	I	112	DQMB4#	I
29	DQMB1#	I	113	DQMB4#	I
30	S0#	I	114	S1#	I
31	OE0#	i	115	RAS#	N/A
32	GND	N/A	116	GND	N/A
33	A0	I	117	A1	I
34	A2	I	118	A3	I
35	A4	I	119	A5	I
36	A6	I	120	A7	I
37	A8	I	121	A9	I
38	A10/AP	I	122	A11	I
39	NC	BA1	123	NC	A11
40	VDD	N/A	124	VDD	N/A
41	NC	N/A	125	CK1	N/A
42	CK0	N/A	126	A14	O
43	GND	N/A	127	GND	N/A
44	OE2#	I	128	CKE0	N/A
45	S2#	I	129	S3#	I
46	DQMB2#	I	130	DQMB6#	I
47	DQMB3#	I	131	DQMB7#	I
48	WE2#	I	132	A15	I
49	VDD	N/A	133	VDD	N/A
50	NC	N/A	134	NC	N/A
51	NC	N/A	135	NC	N/A
52	NC	I/O	136	NC	I/O
53	NC	I/O	137	NC	I/O
54	GND	NA	138	GND	N/A
55	MD16	I/O	139	MD48	I/O
56	MD17	I/O	140	MD49	I/O
57	MD18	I/O	141	MD50	I/O
58	MD19	I/O	142	MD51	I/O
59	VDD	N/A	143	VDD	N/A
60	MD20	I/O	144	MD52	I/O
61	CKE1	N/A	145	NC	N/A
62	VREF	N/A	146	VREF	N/A
63	(CKE1)*	N/A	147	NC	N/A
64	GND	N/A	148	GND	N/A
65	MD21	I/O	149	MD53	I/O

Figure 20 (Page 3 of 3). System memory connector pin input/output

Pin	Signal name	I/O	Pin	Signal name	I/O
66	MD22	I/O	150	MD54	I/O
67	MD23	I/O	151	MD55	I/O
68	GND	N/A	152	GND	N/A
69	MD24	I/O	153	MD56	I/O
70	MD25	I/O	154	MD57	I/O
71	MD26	I/O	155	MD58	I/O
72	MD27	I/O	156	MD59	I/O
73	VDD	N/A	157	VDD	N/A
74	MD28	I/O	158	MD60	I/O
75	MD29	I/O	159	MD61	I/O
76	MD30	I/O	160	MD62	I/O
77	MD31	I/O	161	MD63	I/O
78	GND	N/A	162	GND	N/A
79	CK2	O	163	CK3	O
80	NC	N/A	164	NC	N/A
81	NC	O	165	SA0	O
82	SDA	O	166	SA1	O
83	SCL	O	167	SA0	O
84	VDD	N/A	168	VDD	N/A

PCI connectors

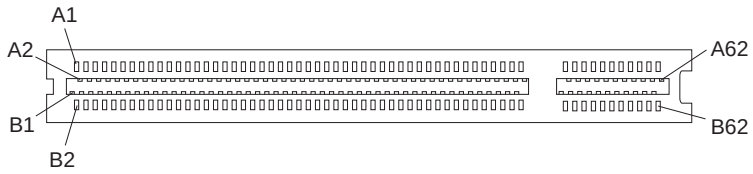


Figure 21 (Page 1 of 3). PCI connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	–12 V dc	NA
A2	+12 V dc	NA	B2	TCK	O
A3	TMS	O	B3	Ground	NA
A4	TDI	O	B4	TDO	I
A5	+5 V dc	NA	B5	+5 V dc	NA
A6	INTA#	I	B6	+5 V dc	NA
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc	NA	B8	INTD#	I
A9	Reserved	NA	B9	PRSNT1#	I
A10	+5 V dc (I/O)	NA	B10	Reserved	NA
A11	Reserved	NA	B11	PRSNT2	I
A12	Ground	NA	B12	Ground	NA
A13	Ground	NA	B13	Ground	NA

Figure 21 (Page 2 of 3). PCI connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A14	Reserved	NA	B14	Reserved	NA
A15	RST#	O	B15	Ground	NA
A16	+5 V dc (I/O)	NA	B16	CLK	O
A17	GNT#	O	B17	Ground	NA
A18	Ground	NA	B18	REQ#	I
A19	PCIPME	NA	B19	+5 V dc (I/O)	NA
A20	Address/Data 30	I/O	B20	Address/data 31	I/O
A21	+3.3 V DC	NA	B21	Address/data 29	I/O
A22	Address/data 28	I/O	B22	Ground	NA
A23	Address/data 26	I/O	B23	Address/data 27	I/O
A24	Ground	I/O	B24	Address/data 25	NA
A25	Address/data 24	I/O	B25	+3.3 V dc	NA
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V dc	NA	B27	Address/data 23	I/O
A28	Address/data 22	I/O	B28	Ground	NA
A29	Address/data 20	I/O	B29	Address/data 21	I/O
A30	Ground	I/O	B30	Address/data 19	NA
A31	Address/data 18	I/O	B31	+3.3 V dc	NA
A32	Address/data 16	I/O	B32	Address/data 17	I/O
A33	+3.3 V dc	NA	B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	NA
A35	Ground	NA	B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	NA
A37	Ground	NA	B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	NA
A39	+3.3 V dc	NA	B39	LOCK#	I/O
A40	SDONE	I/O	B40	PERR#	I/O
A41	SBO#	I/O	B41	+3.3 V DC	NA
A42	Ground	NA	B42	SERR#	I/O
A43	+3.3 V dc	NA	B43	+3.3 V dc	NA
A44	C/BE(1)#	I/O	B44	C/BE 1#	I/O
A45	Address/data 14	I/O	B45	Address/data 14	I/O
A46	Ground	NA	B46	Ground	NA
A47	Address/data 12	I/O	B47	Address/Data 12	I/O
A48	Address/data 10	I/O	B48	Address/data 10	I/O
A49	Ground	NA	B49	Ground	NA
A50	Key	NA	B50	Key	NA
A51	Key	NA	B51	Key	NA
A52	Address/data 8	I/O	B52	Address/data 8	I/O
A53	Address/data 7	I/O	B53	Address/data 7	I/O
A54	+3.3 V DC	NA	B54	+3.3 V dc	NA
A55	Address/data 5	I/O	B55	Address/data 5	I/O
A56	Address/data 3	I/O	B56	Address/data 3	I/O

Figure 21 (Page 3 of 3). PCI connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
A57	Ground	NA	B57	Ground	NA
A58	Address/data 1	I/O	B58	Address/data 1	I/O
A59	+5 V dc (I/O)	NA	B59	+5 V dc (I/O)	NA
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V dc	NA	B61	+5 V DC	NA
A62	+5 V dc	NA	B62	+5 V dc	NA

IDE connectors

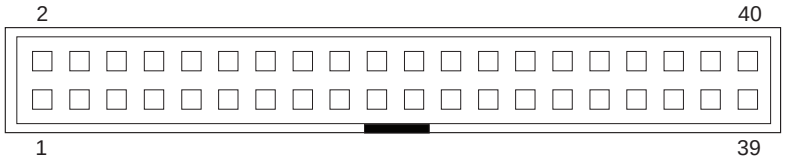


Figure 22. IDE connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	RESET	O	21	NC	NA
2	Ground	NA	22	Ground	NA
3	Data bus bit 7	I/O	23	I/O write	O
4	Data bus bit 8	I/O	24	NC	NA
5	Data bus bit 6	I/O	25	I/O read	O
6	Data bus bit 9	I/O	26	Ground	NA
7	Data bus bit 5	I/O	27	I/O channel ready	I
8	Data bus bit 10	I/O	28	ALE	O
9	Data bus bit 4	I/O	29	NC	NA
10	Data bus bit 11	I/O	30	Ground	NA
11	Data bus bit 3	I/O	31	IRQ	I
12	Data bus bit 12	I/O	32	CS16#	I
13	Data bus bit 2	I/O	33	SA1	O
14	Data bus bit 13	I/O	34	PDIAG#	I
15	Data bus bit 1	I/O	35	SA0	O
16	Data bus bit 14	I/O	36	SA2	O
17	Data bus bit 0	I/O	37	CS0#	O
18	Data bus bit 15	I/O	38	CS1	O
19	Ground	NA	39	Active#	I
20	Key (Reserved)	NA	40	Ground	NA

Diskette drive connector

Figure 23. Diskette Drive Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Drive 2 installed #	I	2	High density select	O
3	Not connected	NA	4	Not connected	NA
5	Ground	NA	6	Data rate 0	NA
7	Ground	NA	8	Index#	I
9	Reserved	NA	10	Motor enable 0#	O
11	Ground	NA	12	Drive select 1#	O
13	Ground	NA	14	Drive select 0#	O
15	Ground	NA	16	Motor enable 1#	O
17	MSEN1	I	18	Direction in#	O
19	Ground	NA	20	Step#	O
21	Ground	NA	22	Write data#	O
23	Ground	NA	24	Write enable#	O
25	Ground	NA	26	Track0#	I
27	MSEN0	I	28	Write protect#	I
29	Ground	NA	30	Read data#	I
31	Ground	NA	32	Head 1 select#	O
33	Data rate 1	NA	34	Diskette change#	I

Power supply connector

Figure 24. Power supply connector pin assignments

Pin	Signal	Function	Pin	Signal	Function
1	3.3 V dc	+3.3 V dc	11	3.3 V dc	+3.3 V dc
2	3.3 V dc	+3.3 V	12	–12 V dc	–12 V dc
3	COM	Ground	13	COM	Ground
4	5 V dc	+5 V dc	14	PS–ON	DC Remote Enable
5	COM	Ground	15	COM	Ground
6	5 V dc	+5 V dc	16	COM	Ground
7	COM	Ground	17	COM	Ground
8	POK	PWR GOOD	18	Reserved	Reserved
9	5 VSB	Standby Voltage	19	5 V dc	+5 V dc
10	12 V dc	+12 V dc	20	5 V dc	+5 V dc

Wake on LAN connectors

Figure 25. J14 Wake on LAN connector pin assignments	
Pin	**Description**
1	+5v AUX
2	Ground
3	Internal Wake on LAN

USB port connectors

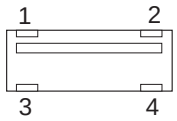


Figure 26. USB Port Connector Pin Assignments	
Pin	**Signal**
1	VCC
2	-Data
3	+Data
4	Ground

Mouse and keyboard port connectors

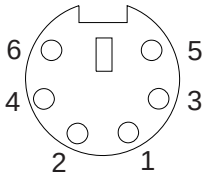


Figure 27. Mouse port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Data	I/O	2	Reserved	I/O
3	Ground	NA	4	+5 V DC	NA
5	Clock	I/O	6	Reserved	NA

Figure 28. Keyboard port connector pin assignments					
Pin	**Signal**	**I/O**	**Pin**	**Signal**	**I/O**
1	Keyboard data	I/O	2	Mouse data	I/O
3	Ground	NA	4	+5 V DC	NA
5	Keyboard clock	I/O	6	Mouse clock	I/O

Serial port connector

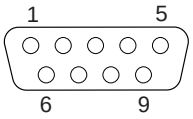


Figure 29. Serial Port Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground	NA	6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Parallel port connector

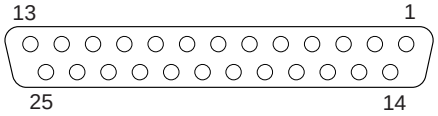


Figure 30. Parallel port connector pin assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE#	I/O	2	Data bit 0	I/O
3	Data bit 1	I/O	4	Data bit 2	I/O
5	Data bit 3	I/O	6	Data bit 4	I/O
7	Data bit 5	I/O	8	Data bit 6	I/O
9	Data bit 7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	NA
19	Ground	NA	20	Ground	NA
21	Ground	NA	22	Ground	NA
23	Ground	NA	24	Ground	NA
25	Ground	NA			

Appendix B. System address maps

System memory map

The first 640 KB of system board RAM is mapped starting at address hex 0000000. A 256 byte area and a 1 KB area of this RAM are reserved for BIOS data areas. Memory can be mapped differently if POST detects an error.

Figure 31. System memory map

Address range (decimal)	Address range (hex)	Size	Description
0 K – 512 K	00000–7FFFF	512 KB	Conventional
512 K – 639 K	80000–9FBFF	127 KB	Extended conventional
639 K – 640 K	9FC00–9FFFF	1 KB	Extended BIOS data
640 K – 767 K	A0000–BFFFF	128 KB	Dynamic video memory display cache
768 K – 800 K	C0000 to C7FFF	32 KB	Video ROM BIOS (shadowed)
800 K – 896 K	C8000–DFFFF	96 KB	PCI space, available to adapter ROMs
896 K – 1 MB	E0000–FFFFF	128 KB	System ROM BIOS (main memory shadowed)
1 MB – 16 MB	100000–FFFFFF	15 MB	PCI space
16 MB – 4095.872 MB	1000000–FFDFFFF	4079.8 MB	PCI space (positive decode)
	FFFE0000 –FFFFFFFF	128 KB	System ROM BIOS

Input/output address map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Figure 32 (Page 1 of 3). I/O Address Map

Address (hex)	Size	Description
0000–000F	16 bytes	DMA 1
0010–001F	16 bytes	General I/O locations — available to PCI bus
0020–0021	2 bytes	Interrupt controller 1
0023–003F	30 bytes	General I/0 locations — available to PCI bus
0040–0043	4 bytes	Counter/timer 1
0044–00FF	28 bytes	General I/0 locations — available to PCI bus
0060	1 byte	Keyboard controller byte — reset IRQ
0061	1 byte	System port B
0064	1 byte	Keyboard controller, CMD/STAT byte
0070, bit 7	1 bit	Enable NMI
0070, bits 6:0	1 bit	Real-time clock, address
0071	1 byte	Real-time clock, data
0072–007F	14 bytes	General I/O locations — available to PCI bus
0080	1 byte	POST checkpoint register during POST only

Figure 32 (Page 2 of 3). I/O Address Map

Address (hex)	Size	Description
008F	1 byte	Refresh page register
0080–008F	16 bytes	ICH1, DMA page registers
0090–0091	15 bytes	General I/O locations — available to PCI bus
0092	1 byte	PS/2 keyboard controller registers
0093–009F	15 bytes	General I/O locations
00A0–00A1	2 bytes	Interrupt controller 2
00A2–00BF	30 bytes	APM control
00C0–00DF	31 bytes	DMA 2
00E0–00EF	16 bytes	General I/O locations — available to PCI bus
00F0	1 byte	Coprocessor Error Register
00F1–016F	127 bytes	General I/O locations — available to PCI bus
0170–0177	8 bytes	Secondary IDE channel
01F0–01F7	8 bytes	Primary IDE channel
0200–0207	8 bytes	Available
0220–0227	8 bytes	Serial port 3 or 4
0228–0277	80 bytes	General I/O locations — available to PCI bus
0278–027F	8 bytes	LPT3
0280–02E7	102 bytes	Available
02E8–02EF	8 bytes	Serial port 3 or 4
02F8–02FF	8 bytes	COM2
0338–033F	8 bytes	Serial port 3 or 4
0340–036F	48 bytes	Available
0370–0371.	2 bytes	SIO planar Plug and Play index/data registers
0372–0375	4 bytes	Available
0376–0377	2 bytes	IDE channel 1 command
0378–037F	8 bytes	LPT2
0380–03B3	52 bytes	Available
03B4–03B7	4 bytes	Video
03BA	1 byte	Video
03BC–03BE	16 bytes	LPT1
03C0–03CF	16 bytes	Video
03D4–03D7	4 bytes	Video
03DA	1 byte	Video
03D0–03DF	11 bytes	Available
03E0–03E7	8 bytes	Available
03E8–03EF	8 bytes	COM3 or COM4
03F0–03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Diskette channel 1 command
03F7, bit 7	1 bit	Diskette disk change channel
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8–03FF	8 bytes	COM1
0400–047F	128 bytes	Available

Figure 32 (Page 3 of 3). I/O Address Map		
Address (hex)	**Size**	**Description**
0480–048F	16 bytes	DMA channel high page registers
0490–0CF7	1912 bytes	Available
0CF8–0CFB	4 bytes	PCI Configuration address register
0CFC–0CFF	4 bytes	PCI Configuration data register
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + hex 400
0CF9	1 byte	Turbo and reset control register
0D00–FFFF	62207 bytes	Available

DMA I/O address map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Figure 33 (Page 1 of 2). DMA I/O address map			
Address (hex)	**Description**	**Bits**	**Byte pointer**
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register [3]	00–07	
0082	Channel 3, Page Table Address register [3]	00–07	
0083	Channel 1, Page Table Address register [3]	00–07	
0087	Channel 0, Page Table Address register [3]	00–07	
0089	Channel 6, Page Table Address register [3]	00–07	
008A	Channel 7, Page Table Address register [3]	00–07	
008B	Channel 5, Page Table Address register [3]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes

Figure 33 (Page 2 of 2). DMA I/O address map

Address (hex)	Description	Bits	Byte pointer
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

PCI configuration space map

Bus number (hex)	Device number (hex)	Function number (hex)	Description
00	00	00	VIA VT 82C694X (north bridge)
00	01	00	VIA VT 82C694X (north bridge)
00	02	00	VIA VT 82C596B south bridge
00	02	01	VIA VT 82C596B south bridge
00	02	02	VIA VT 82C596B south bridge
00	02	03	Intel 82371AB power management
00	0x12	00	ESS 1930 audio controller
01	00	00	S3 Trio3D AGP video
00	0 x 10	NA	Slot 1
00	0 x 0F	NA	Slot 2
00	0 x 0E	NA	Slot 3

[3] Upper byte of memory address register.

Appendix C. IRQ and DMA channel assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Figure 34. IRQ channel assignments

IRQ	System resource
NMI	Critical system error
SMI	System management interrupt — power management
0	Reserved (interval timer)
1	Reserved (keyboard)
2	Reserved, cascade interrupt from slave PIC
3	COM2 [4]
4	COM1 [4]
5	LPT2/audio (if present)
6	Diskette controller
7	LPT1 [4]
8	Real-time clock
9	ACPI
10	Available to user
11	Available to user
12	Mouse port
13	Reserved (math coprocessor)
14	Primary IDE (if present)
15	Secondary IDE (if present)

Figure 35. DMA channel assignments

DMA channel	Data width	System resource
0	8 bits	Open
1	8 bits	Open
2	8 bits	Diskette drive
3	8 bits	Parallel port (for ECP or EPP)
4	–	Reserved (cascade channel)
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

[4] Default, can be changed to another IRQ.

Appendix D. Error codes

A complete list of POST error codes is provided in *PC 300GL and PC 300PL User Guide* and in *Hardware Maintenance Manual*.

POST error codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages.

Beep codes

A complete list of beep codes is provided in *Hardware Maintenance Manual*.

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References

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  Source: Intel Corporation
- *AT Attachment Interface with Extensions*
  Source: American National Standard of Accredited Standards Committee
- *Extended Capabilities Port: Specification Kit*
  Source: Microsoft Corporation
- *Intel Microprocessor and Peripheral Component Literature*
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- *PCI BIOS Specification 2.0*
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- *PCI Local Bus Specification 2.1*
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  Source: Microsoft Corporation
- *Universal Serial Bus Specifications*
  Source: *http://www.usb.org*
- *Video Electronics Standards Association 1.2*
  Source: *http://www.vesa.org*
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