FEB 1992

VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

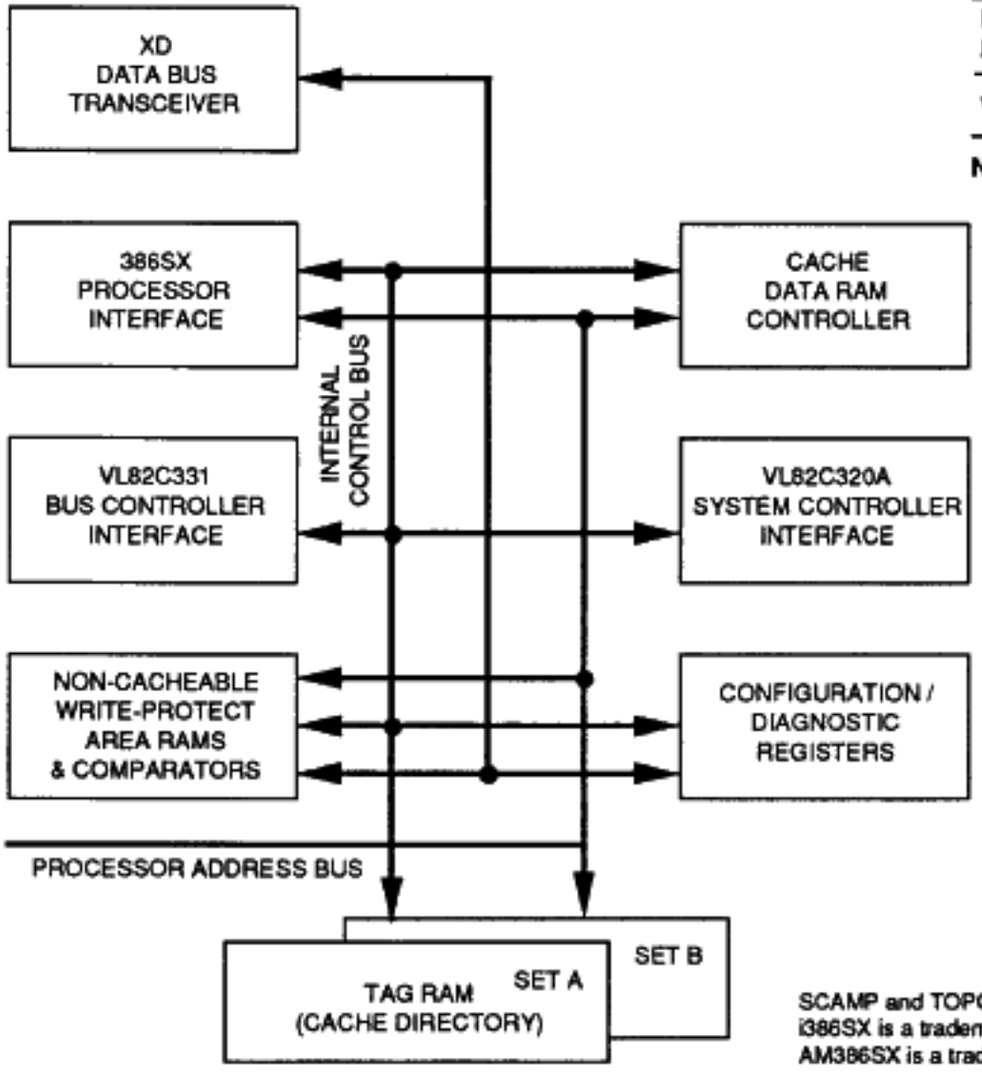
VL82C325

VL82C386SX SYSTEM CACHE CONTROLLER

FEATURES

- Optimized for TOPCAT™ 386SX and SCAMP™-LT chip sets
- Improved i386SX™ and AM386SX™ system performance
  - Fast look-aside architecture
  - Zero wait state read-hit access
  - Reduces average processor wait states to near zero
- Multiple cache organizations
  - Two-way set associative: 16KB
  - Two-way set associative: 32KB
- Memory update strategy
  - Write-thru
- Least recently used (LRU) replacement algorithm
- Integrates complete cache directory on-chip
- Supports memory configurations to 16 MB
- Programmable cache architecture
  - Block size: 8 or 16 bytes
  - Line size: 2 bytes
  - Update strategies: single cycle (one line)
- Write-protect region support
  - Write-protect regions (#): 256
  - Write-protect region size: 2KB between 512K and 1M
- Non-cacheable region support
  - Non-cache regions (#): 504
  - Non-cacheable region size: 64KB below 512K, 2KB between 512K and 1M, 64KB above 1M
- 25 MHz operation
- Optimized for one or two dual 4K x 8 cache data RAMs
- Operates both in pipelined and in non-pipelined modes
- Built-in self-test and cache data RAM testability features
- Auto-flush on EMS-update events
- 100-lead MQFP

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package
VL82C325-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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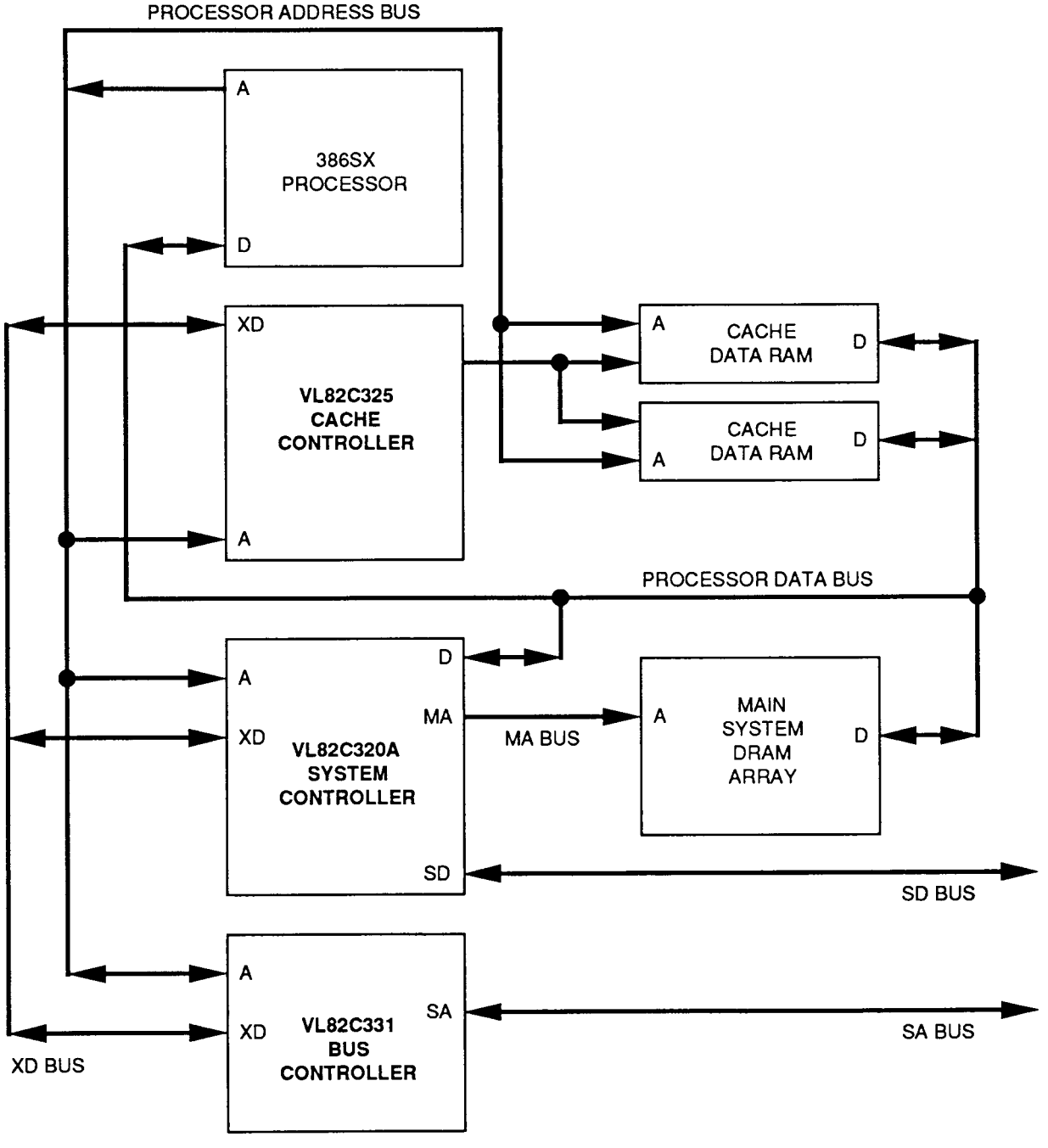
i386SX is a trademark of Intel Corp.
AM386SX is a trademark of AMD Corp.

OVERVIEW

The VL82C325 Memory Cache Controller is a high performance, highly integrated cache controller for systems based on the VLSI Technology, Inc.'s TOPCAT 386SX or SCAMP-LT chip sets. To implement a 32KB two-way set associative cache subsystem, all that is required is the VL82C325 and two 8K x 16 cache data RAMs. The VL82C325 has been designed to be an integral part of the TOPCAT386SX chip set. This feature improves the overall system performance by reducing the number of wait states during non-cache cycles when compared to cache controllers which must pipeline all cycles which can not be serviced by reading from the cache data RAM. The VL82C320A TOPCAT System Controller or the VL82C310 SCAMP Controller, and the VL82C325 operate in parallel to decode 386SX requests. The controller starts decoding the 386SX cycle simultaneously with the VL82C325 and is therefore able to actually start a memory cycle before a miss indication is generated by the VL82C325.

TOPCAT WITH CACHE SYSTEM BLOCK DIAGRAM



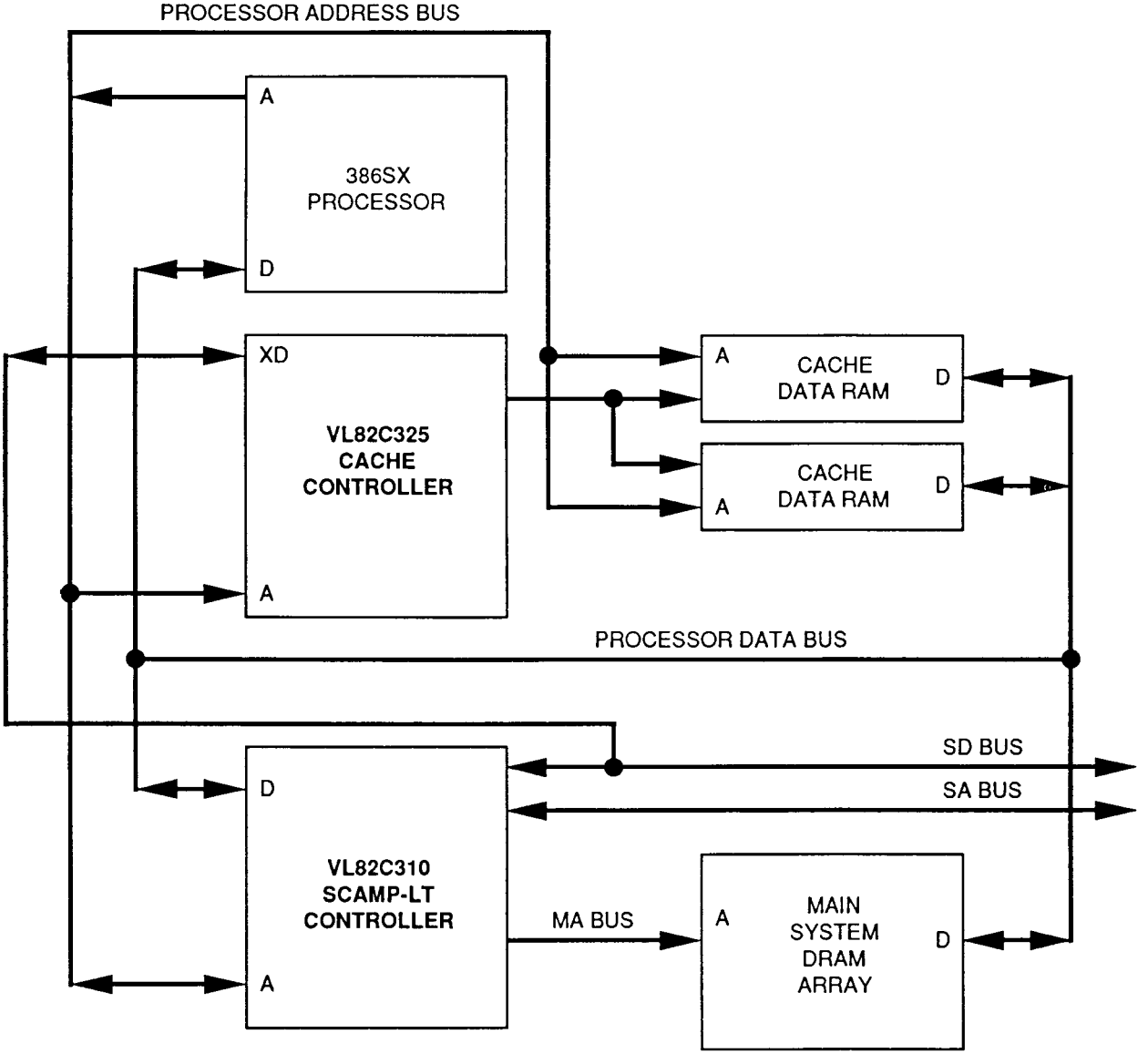
The VL82C325 is a read allocate, write-thru cache. It maintains cache coherency during non-386SX cycles by monitoring the VL82C320A/VL82C331 interface or VL82C310 SCAMP-LT interface and the system address bus. Any HLDA cycle which writes to a memory location which is also cached will invalidate the line. HLDA read cycles which result in a hit within the cache data have no effect. Read data for these cycles is not supplied by the cache data RAM.

The VL82C325 supports 16KB or 32KB two-way set associative caches. On-chip high speed SRAM is used for the cache directory which is organized as two 1024 entry directories. The line size is two bytes. Each cache directory entry defines the storage allocation for a block which is set to be four lines for 16KB cache configurations or eight lines for 32KB caches. Each line or sub-block has its own valid bit within the cache directory entry.

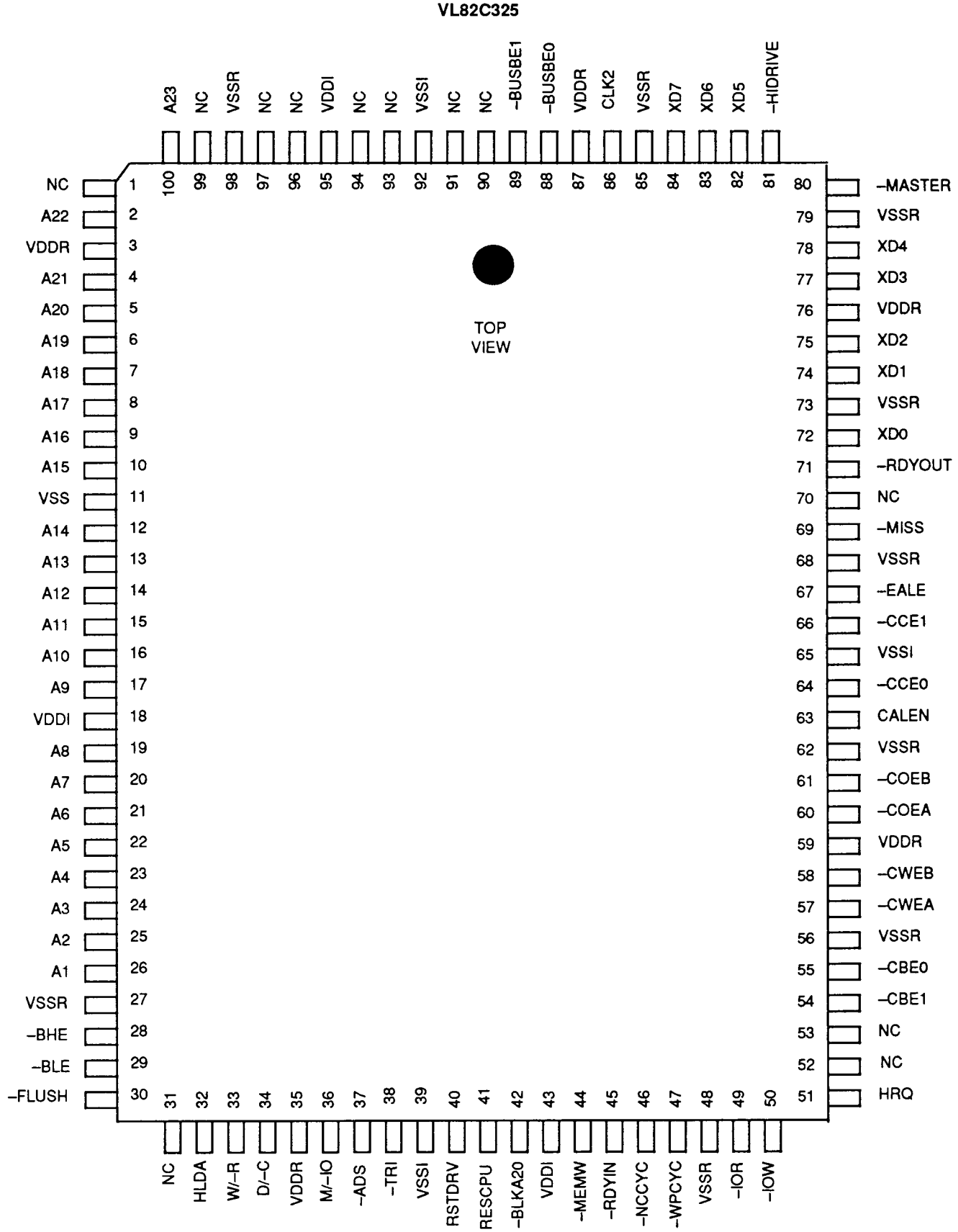
System memory can be declared as cacheable or non-cacheable by setting or clearing entries in the Non-Cache Table (NCT). The NCT has 504 entries which cover all of system memory (memory controlled by the system controller). In the area 512KB to 1MB, system memory is divided into 2KB regions. Each individual region can be declared cacheable or non-cacheable. In the remaining areas of system memory, each 64KB region of memory can be individually selected as cacheable or non-cacheable.

System memory can be declared as write-protected (e.g., ROM space) by setting entries in the Write-Protect Table (WPT). The WPT has 256 entries which cover the area of system memory from 512KB to 1MB. Each individual 2KB region in this area can be declared write-protected. Writes to a write-protected region which result in a cache-hit will not update the contents of cache data RAM.

SCAMP-LT WITH CACHE SYSTEM BLOCK DIAGRAM



PIN DIAGRAM


VL82C325
TOP VIEW
1 NC
2 A22
3 VDDR
4 A21
5 A20
6 A19
7 A18
8 A17
9 A16
10 A15
11 VSS
12 A14
13 A13
14 A12
15 A11
16 A10
17 A9
18 VDDI
19 A8
20 A7
21 A6
22 A5
23 A4
24 A3
25 A2
26 A1
27 VSSR
28 -BHE
29 -BLE
30 -FLUSH
31 NC
32 HLDA
33 W/-R
34 D/-C
35 VDDR
36 M/-IO
37 -ADS
38 -TRI
39 VSSI
40 RSTDRV
41 RESCPU
42 -BLKA20
43 VDDI
44 -MEMW
45 -RDYIN
46 -NCCYC
47 -WPCYC
48 VSSR
49 -IOR
50 -IOW
51 HRQ
52 NC
53 NC
54 -CBE1
55 -CBE0
56 VSSR
57 -CWEA
58 -CWEB
59 VDDR
60 -COEA
61 -COEB
62 VSSR
63 CALEN
64 -CCE0
65 VSSI
66 -CCE1
67 -EALE
68 VSSR
69 -MISS
70 NC
71 -RDYOUT
72 XD0
73 VSSR
74 XD1
75 XD2
76 VDDR
77 XD3
78 XD4
79 VSSR
80 -MASTER
81 -HIDRIVE
82 XD5
83 XD6
84 XD7
85 VSSR
86 CLK2
87 VDDR
88 -BUSBE0
89 -BUSBE1
90 NC
91 NC
92 VSSI
93 NC
94 NC
95 VDDI
96 NC
97 NC
98 VSSR
99 NC
100 A23

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU AND TIMING INTERFACE PINS			
A23-A1	2, 4-9, 10, 12-17 19-26, 100	I-TTL	Address bus bits 23 through 1 - These signals are tied to the processor's address bus bits 23-1.
–BHE	28	IO-TTL (8 mA)	Byte High Enable - This signal is tied to the processor's byte high enable output. It is used to select the upper byte of a 16-bit wide memory or I/O location.
–BLE	29	IO-TTL (8 mA)	Byte Low Enable - This signal is tied to the processor's byte low enable output. It is used to select the lower byte of a 16-bit wide memory or I/O location.
–ADS	37	I-TTL	Address Status - This signal is tied to the processor's –ADS output.
W/–R	33	I-TTL	Write and not Read - This signal is tied to the processor's W/–R output.
M/–IO	36	I-TTL	Memory and not I/O Cycle - This signal is tied to the processor's M/–IO output.
D/–C	34	I-TTL	Data and not Code - This signal is tied to the processor's D/–C output.
HLDA	32	I-TTL	Hold Acknowledge - This input is generated by the 386SX CPU, and indicates that the current hold acknowledge cycle is for the DMA controller or other Bus Master. When active, the VL82C325 ignores the CPU's status signals and monitors –MEMW to determine if the cycle will invalidate any cached item.
–BLKA20	42	I-TTL	Address Bit 20 Enable - This active low input is tied to the –BLKA20 output of the VL82C320A System Controller and is used to deactivate A20. It is a decode of the A20GATE signal from the keyboard controller and Port A bit 1. Port A bit 1 may be written directly or set by a dummy read of I/O port EEh. Refer to the VL82C320A specification for more details.
–NCCYC	46	I-TPU	Non-Cache Cycle - This active low input may be driven by external circuitry during access to regions of memory which should not be cached. It is ignored during memory write, I/O, and halt/shutdown cycles.
–WPCYC	47	I-TPU	Write-Protect Cycle - This active low input may be driven by external circuitry during access to regions of memory for which cache data RAM should be write-protected. It is ignored during memory read, I/O, and halt/ shutdown cycles.
–RDYOUT	71	IO-TTL (8 mA)	VL82C325 Ready - This output is driven active for all cache read-hits and diagnostic operations. It is an input in the In-Circuit Test (ICT) Mode.
–RDYIN	45	I-TTL	Processor's Ready - This input is tied directly to the processor's READY input pin.
–FLUSH	30	I-TPU	Flush - This input is used to generate hardware-flush requests. When this input is driven active while the VL82C325 is enabled, the cache directory is flushed.
HRQ	51	I-TTL	Hold Request - This input is tied to the processor's HOLD input.
CACHE DATA RAM INTERFACE PINS			
–CWEA	57	IO-TTL (8 mA)	Cache RAM Write Enable A - This output is active low and is tied to the write enable(s) of the first set (A) of cache data RAMs. It is an input in the In-Circuit Test (ICT) Mode.
–CWEB	58	IO-TTL (8 mA)	Cache RAM Write Enable B - This output is active low and is tied to the write enable(s) of the second set (B) of cache data RAMs. It is an input in the In-Circuit Test (ICT) Mode.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–COEA	60	IO-TTL (8 mA)	Cache RAM Output Enable A - An active low signal which is tied to the output enable(s) of the first set (A) of cache data RAMs. It is an input in the In-Circuit Test (ICT) Mode.
–COEB	61	IO-TTL (8 mA)	Cache RAM Output Enable B - This active low signal which is tied to the output enable(s) of the second set (B) of cache data RAMs. It is an input in the In-Circuit Test (ICT) Mode.
CALEN	63	IO-TTL (8 mA)	Cache RAM Address Latch Enable - An active high signal which opens the input address latches on all of the cache data RAMs. It is an input in the In-Circuit Test (ICT) Mode.
–CCE0	64	O (8 mA)	Cache RAM Chip Enable 0 - An active low signal which is tied to the chip enable(s) of the least significant 16KB of cache data memory.
–CCE1	66	O (8 mA)	Cache RAM Chip Enable 1 - An active low signal which is tied to the chip enable(s) of the most significant 16KB of cache memory. This pin is not connected in the 16KB configuration.
–CBE0	55	O (8 mA)	Cache RAM Byte Enable 0 - An active low signal which is tied to the chip select(s) of the cache data RAMs corresponding to data bits 0-8.
–CBE1	54	O (8 mA)	Cache RAM Byte Enable 1 - An active low signal which is tied to the chip select(s) of the cache data RAMs corresponding to data bits 8-15.
SYSTEM AND BUS CONTROLLER INTERFACE PINS			
XD7- XD0	72, 74, 75, 77, 78, 82-84	IO-TTL (12/24 mA)	X Data Bus - These signals are tied to the XD bus in TOPCAT systems and the SD bus in SCAMP systems. This bus is used to read and write the VL82C325's internal configuration registers.
–MISS	69	IO-TTL (8 mA)	Miss - This active low output indicates that the current memory cycle request can not be serviced by the VL82C325. It is an input in the In-Circuit-Test (ICT) Mode.
–EALE	67	O (8 mA)	Bus ALE - This output is tied to the –EALE input of the VL82C331 Bus Controller. It is used to strobe the byte enables into the bus controller.
RSTDRV	40	I-TTL	Power-on Reset Input - This active high input is driven by the VL82C331 Bus Controller's RSTDRV output. It indicates that a hardware reset signal has been activated. This is the same signal which is output to the ISA bus. This signal is used as the power-on reset source and is used to reset all internal logic.
RESCPU	41	I-TTL	Reset CPU - This input signal is tied directly to the processor's RESET input. It is used by the VL82C325 to synchronize its internal clock to the processor's clock. The internal configuration registers are not initialized from RESCPU.
CLK2	86	I-CMOS	Clock - This signal is tied to the processor's clock input.
–TRI	38	I-TPU	Three-state - This input is used to put all of the VL82C325's outputs and bidirectional pins into the three-state mode for testing.
–MEMW	44	I-TTL	Memory Write - This input is driven by the –MEMW signal from the VL82C331 Bus Controller. When it is active during hold acknowledge, it indicates that a write operation is taking place to system memory during DMA or Bus Master operations.
–IOR	49	I-TTL	I/O Read - This input is driven by the –IOR signal from the bus controller. It indicates that an I/O read operation is taking place. The VL82C325's internal configuration registers are accessed via I/O reads and writes.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–IOW	50	I-TTL	I/O Write - This input is driven by the –IOW signal from the bus controller. It indicates that an I/O write operation is taking place. The VL82C325's internal configuration registers are accessed via I/O reads and writes.
–HIDRIVE	81	I-TPU	High Drive - This input is a wire-strap option. When low, the XD7-XD0 outputs will sink the full 24 mA. When high, they sink 12 mA. Note that all AC specifications are specified at 24 mA drive. –HIDRIVE has an internal pull-up and can be left open if 12 mA drive is desired.
–BUSBE0	88	IO-TTL (8 mA)	Bus Byte Enable 0 - An active low output which drives the –BE0/A0 input of the VL82C331 Bus Controller. It indicates that the low byte of the processor's data bus (D7-D0) is to be used in this cycle.
–BUSBE1	89	IO-TTL (8 mA)	Bus Byte Enable 1 - An active low output which drives the –BE1/–BHE input of the VL82C331 Bus Controller. It indicates that the high byte of the processor's data bus (D15-D8) is to be used in this cycle.
–MASTER	80	I-TPU	Master - This input is tied to the bus controller's –MASTER input. It permits Master Mode DMA access to the VL82C325's internal configuration registers. If Master Mode access is not desired, then this pin can be left unconnected or pulled up.
POWER SUPPLIES AND "NO CONNECT" PINS			
VDDR	3, 35, 59, 76, 87	PWR	I/O Ring Power Supply inputs, nominally +5 V.
VSSR	27, 48, 56, 62, 68, 73, 79, 85	GND	I/O Ring Ground returns, nominally 0 V.
VDDI	18, 43, 95	PWR	Internal Power Supply inputs, nominally +5 V.
VSSI	1, 11, 39 65, 92	GND	Internal Ground returns, nominally 0 V.
NC	31, 52, 53, 70, 90, 91, 93, 94, 96 97, 99		No Connects - All "no connects" must be left unconnected. Never connect these pins to signal nets or to power nets.

SIGNAL LEGEND

Signal Type	Description	Signal Type	Description
I-TTL	TTL level input	O-OD	Open drain
I-TPD	Input with 30k ohm pull-down resistor	O	CMOS and TTL level compatible output
I-TPU	Input with 30k ohm pull-up resistor	O-TTL	TTL level output
I-TSPU	Schmitt-trigger input with 30k ohm pull-up resistor	O-TS	Three-state level output
I-CMOS	CMOS level input	I1	Input used for testing
IO-TTL	TTL level input/output	GND	Ground
IT-OD	TTL level input/open drain output	PWR	Power
IO-OD	Input/open drain, slow turn-on		

DEFINITION OF TERMS

For the sake of consistency, a set of definitions is included here. These terms are organized in a top-down manner as they are typically used to describe the hierarchy of the VL82C325's internal tag storage.

Associativity The number of entries in a cache to which one address could possibly be mapped, e.g., in a one-way controller each address maps to one location only, while in a two-way controller, each address could be in one of two locations.

Set The set of tags is the highest level of the cache memory organization hierarchy. There is one set for each degree of associativity, so a two-way set associative cache has two sets of tags which are all accessed in parallel in the controller. Each set is made of a number of blocks and sub-blocks.

Block This is the second level of hierarchy, it consists of a number of items (sub-blocks or lines) which all share the same values in the upper bit of their addresses. Typically there is one tag RAM entry for each block, and there are multiple sub-blocks/block.

Sub-block This is the third level (lowest) of the hierarchy. It is the smallest amount of memory which is updated at once. In single-chip cache controllers this is the same as a line, since there can be fewer bits of total tag storage required with this third level of hierarchy.

Line Same as sub-block for integrated caches (three levels of hierarchy), for direct mapped caches with external tag storage (two levels), it is the same as a block. A line may be longer than the data bus width of the processor.

Write-thru This policy forces a write cycle to external memory (DRAM) for each write performed by the processor. The cache data RAM (SRAM) might or might not be updated with the contents of the write.

Read-allocate An update policy which allows cache blocks to be allocated only on read-miss cycles. Write-miss cycles do not allocate space in the cache directory.

Look-aside This policy enables a cycle to be started in the system controller, in parallel with the VL82C325, even before cache hit-miss has been determined. This can reduce average cache-miss cycle times.

LRU Leat Recently Used refers to the algorithm which is used to replace items in the cache. In a two-way set associative cache there are two candidates for replacement (one in each set). That candidate which least recently generated a cache-hit (read or write) will be chosen for replacement.

FUNCTIONAL DESCRIPTION

RESPONSE TO CYCLE TYPES

The VL82C325 will cache only the memory which exists in the main memory controlled by the VL82C320A System Controller and VL82C310 SCAMP Controller. This includes all memory segments which have been shadowed as well as memory (ROM or RAM) which exists on the ISA bus.

The VL82C325 is a look-aside cache controller. It operates in conjunction with the system controller. The system controller is able to begin a cycle in main memory while the VL82C325 simultaneously determines whether the cycle hit or missed in the cache data memory.

If a cache-miss occurs and the cycle is cacheable, then the VL82C325 disables the cache data RAMs outputs, and allows the system controller to complete the cycle. This is accomplished by asserting the –MISS signal to the system controller. The system controller is responsible for terminating miss cycles with READY.

If the cycle was a read, then the VL82C325 allocates a block for the new data in the cache directory. At the end of the cycle, the VL82C325 writes the new data into the cache data RAMs.

If the cycle was a write, then the VL82C325 does nothing, because directory space is only allocated on read-miss cycles (read-allocate).

If a cache-hit occurs, then the VL82C325 must complete the cycle in the cache data RAMs, i.e., it reads from or writes to cache data memory.

If the cycle was a read, then the cycle in the system controller must be aborted. This is accomplished by negating the –MISS signal to the system controller (indicating a hit). In this case, the VL82C325 must terminate the cycle with READY because the aborted cycle in the system controller will not provide a READY.

If the cycle was a write, then the cycle in the system controller is allowed to complete as normal (write-thru), and the data is simultaneously written into the cache data RAMs. This maintains coherency between main memory and cache data memory. In this case, the state of the –MISS signal is ignored by the system controller. The system controller provides the READY.

The VL82C325 will assert –MISS during non-cacheable read cycles. All such cycles must complete in the system controller. Data is not read from cache data RAMs, and the cache directory is unaltered. Write cycles are always considered to be cacheable.

The VL82C325 never allocates cache space for HLDA cycles. However, if a HLDA write hits in the cache, then some action must be taken to prevent the cache data memory from becoming stale. Therefore, the cache directory valid bit for that line is invalidated. The remaining valid bits for the other lines in the same block are unaltered.

Tables 1 and 2 summarize the VL82C325's and system controller's responses to all cycle types.

TABLE 1. RESPONSE TO CPU CYCLES

Bus Cycle Type					Cache Response				
M/–IO	D/–C	W/–R	386 Cycle	Conditions	–MISS	Cnfig Reg	Data RAM	Direc RAM	VL82C320A Response
0	0	0	INTA		0				INTA to '331
0	0	1	Undefined		0				Halt/Shutdown
0	1	0	I/O Read	'325 Reg Other	0 0	Read			I/O Read to '331
0	1	1	I/O Write	'325 Reg Other	0 0	Write			I/O Write to '331
1	0	0	Memory Code Read	Hit Miss Non-cache	1 0 0		Read Write	Update	Aborted Memory Read Memory Read (16, 2x8)
1	0	1	Halt/Shutdown		0				Halt/Shutdown
1	1	0	Memory Data Read	Hit Miss Non-cache	1 0 0		Read Write	Update	Aborted Memory read Memory Read (16, 2x8) Memory Read (8, 16, 2x8)
1	1	1	Memory Data Write	Hit/writeable Hit/write-prot Miss	0 0 0		Write		Memory Write (8, 16, 2x8)

TABLE 2. RESPONSE TO HLDA CYCLES

Bus Cycle Type		Cache Response			
386 Cycle	Conditions	–MISS	Cnfig Reg	Data RAM	Direc RAM
Memory Read		0			
Memory Write	Hit Miss	0 0			Invalidate
I/O Read		0			
I/O Write		0			

CACHE ORGANIZATION

The VL82C325 is a two-way set associative cache controller. It supports cache sizes of either 16KB or 32KB, arranged as 2 x 4K x 16-bit or 4 x 4K x 16-bit respectively (refer to Figure 4). Table 3 gives a summary of the cache directory structure in each mode.

Figure 1 depicts the manner in which main memory maps to the cache data memory. Main memory is divided into pages, each page being the size of one set of cache data memory. Pages are further divided into 1024 blocks each. A block of main memory at offset X in page W always maps to a block at offset X in either of set A or set B of cache data memory. Because there are two sets, two such block Xs (each from a different page) may reside in cache data memory simultaneously. However, if a third access is made to yet another block having offset X in a third and different page, then one of the original blocks is discarded to make space for the new one. A least recently used (LRU) algorithm is used to determine whether it will map to set A or to set B.

The page number associated with each cached block is retained in the cache directory. The directory contains one entry per block. Thus, there are two directories (one for each set) each containing 1024 entries.

Blocks are further divided into sub-blocks or lines. Each directory entry also contains a valid bit per sub-block. The sub-block valid bits reduce the number of accesses to main store by allowing the VL82C325 to fetch only those lines which have been requested by the processor.

Hit/miss is determined as follows:

The block number of the memory address is used to extract an entry from each of the set directories. The memory address is then compared to each entry in parallel. If either entry compares true, then a hit has occurred. It is not possible for both entries to compare true. The look-up function is depicted in Figures 2 and 3.

TABLE 3. CACHE DIRECTORY CONFIGURATIONS

Cache Size (KB)	# of Sets	Block Size (B)	Sub-Block Size (Line) (B)	Page Size (KB)	# of Pages	# of Directory Entries per Set
16	2	8	2	8	2048	1024
32	2	16	2	16	1024	1024

FIGURE 1. TWO-WAY SET ASSOCIATIVE CACHE ORGANIZATION

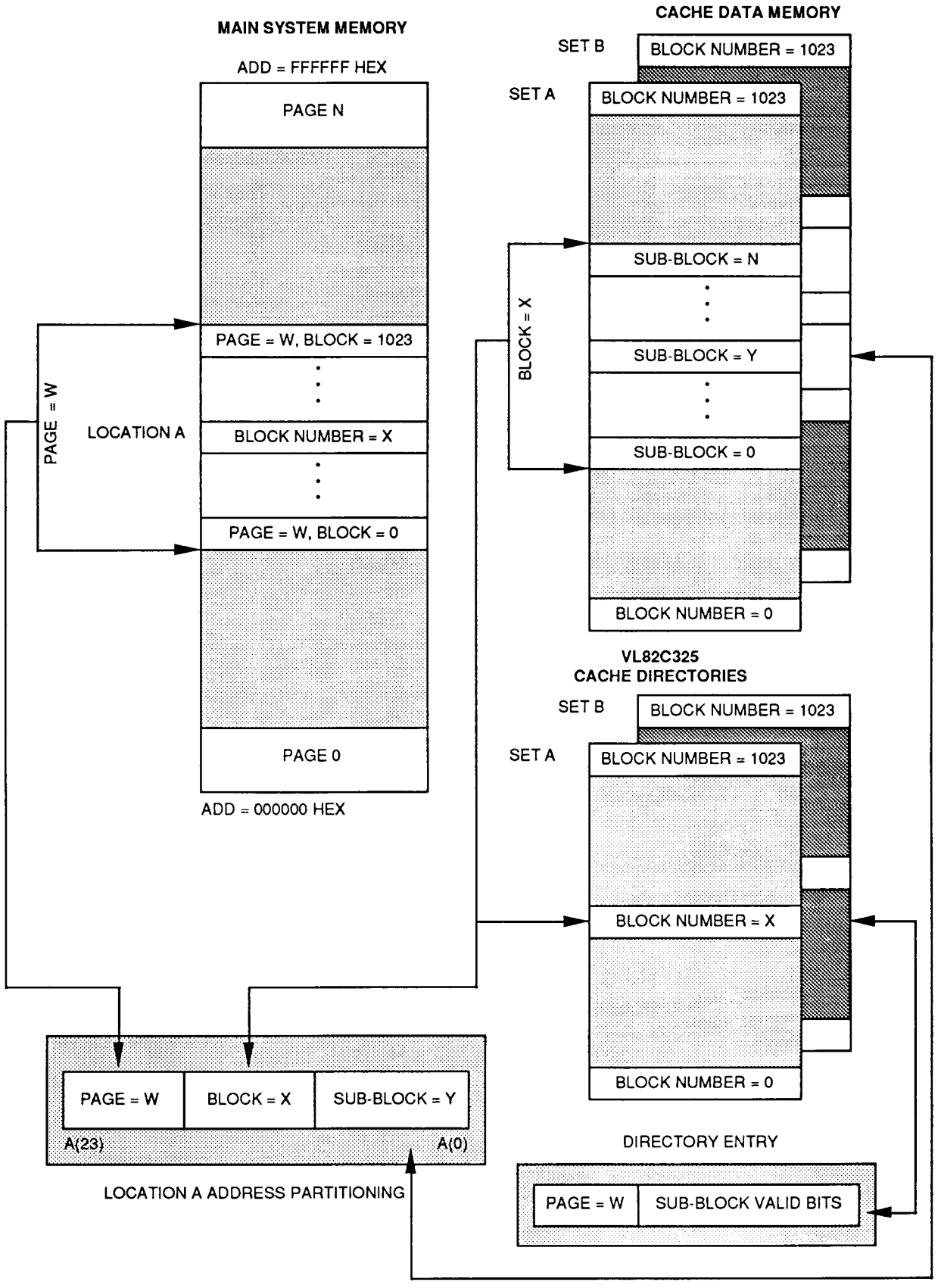


FIGURE 2. 16KB CACHE LOOK-UP

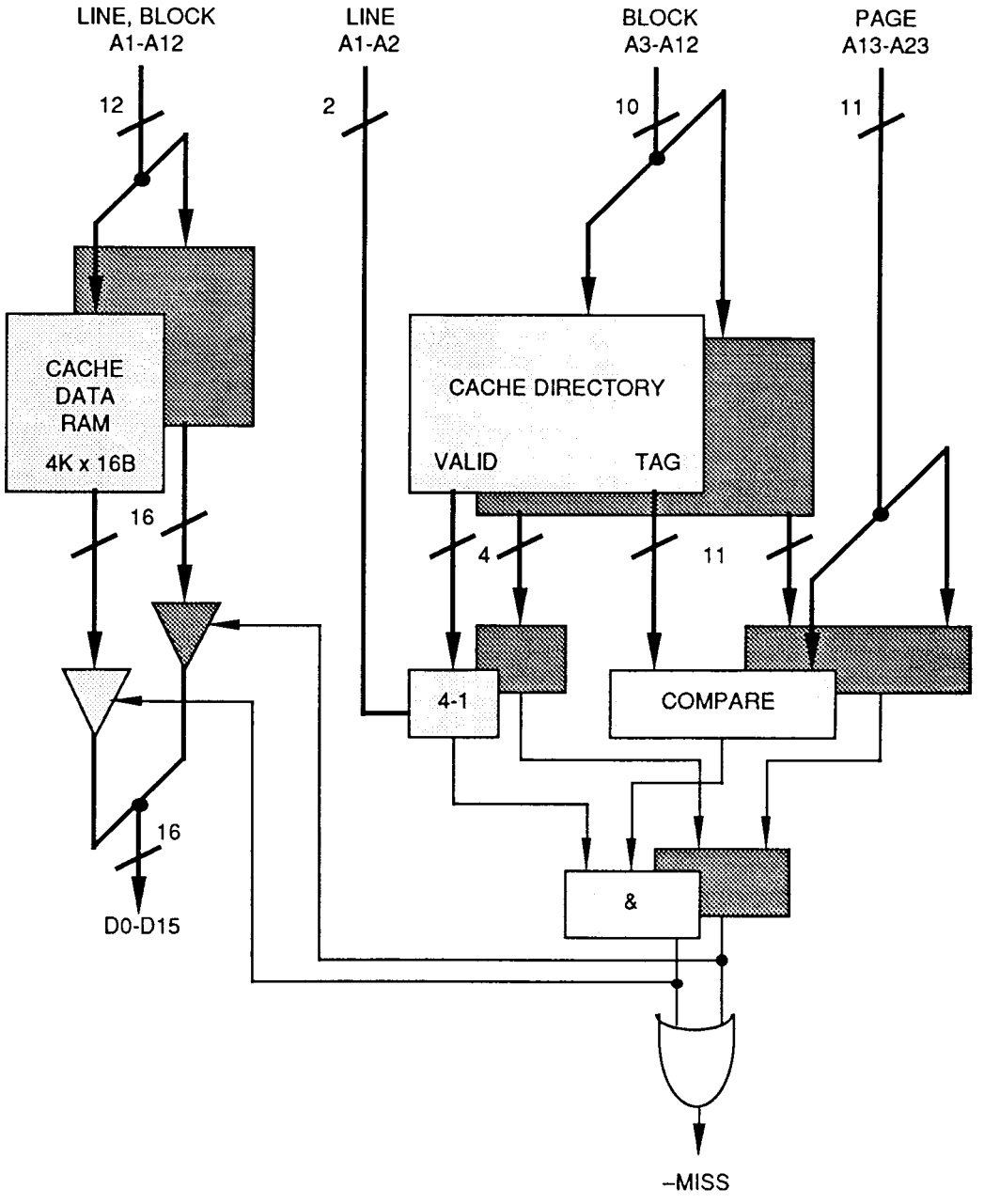
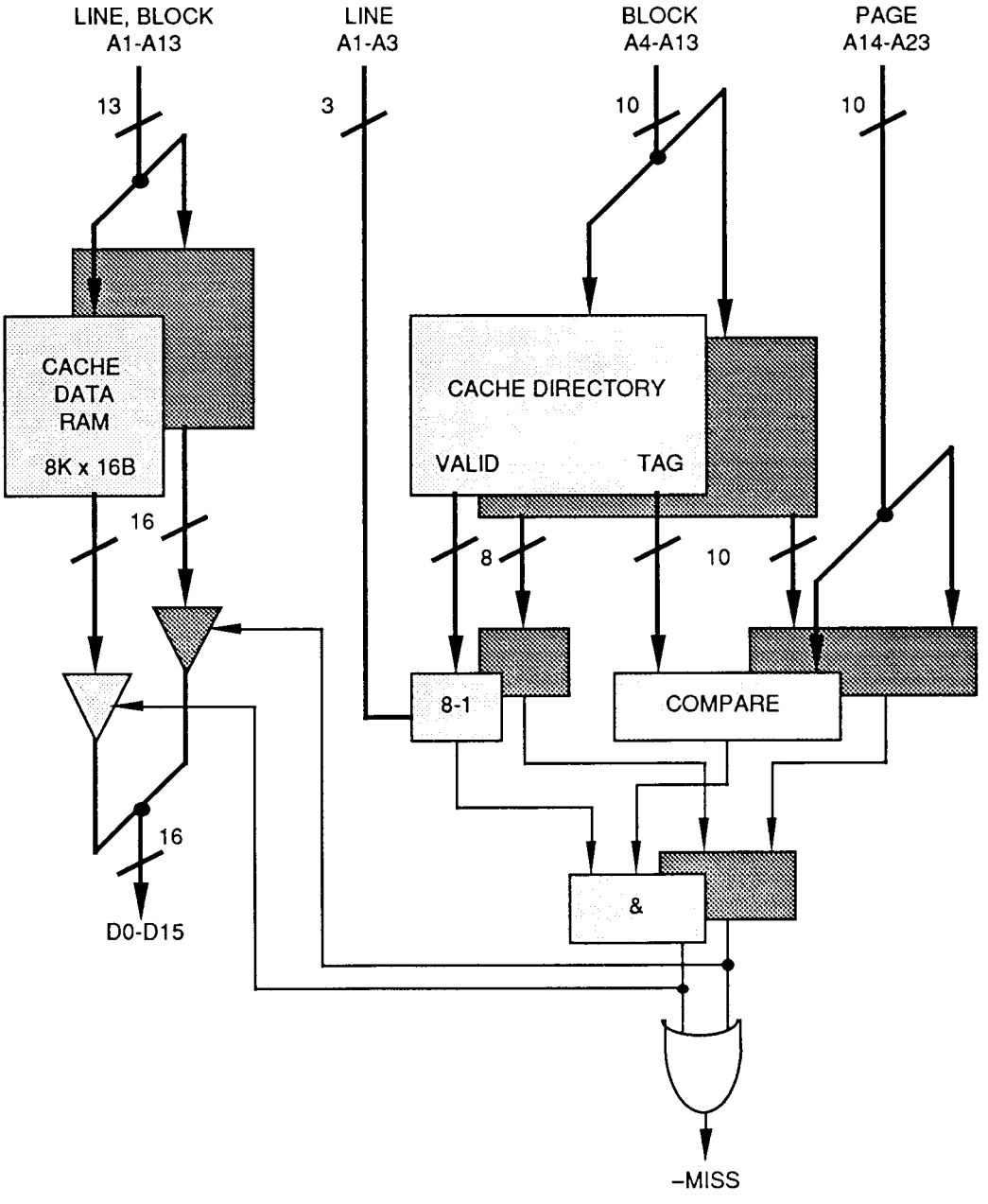


FIGURE 3. 32KB CACHE LOOK-UP



NON-CACHEABLE & WRITE-PROTECT REGIONS

Sometimes it is undesirable to cache certain areas of memory, e.g., areas who's contents may change invisibly to the processors local bus. Examples are I/O controllers or dual ported memories in multi-processor systems. Two mechanisms are provided for the definition of non-cacheable regions.

The first is a dedicated input signal to the controller. The user may decode non-cacheable addresses outside the controller, and provided that the –NCCYC signal is asserted with the correct timing, then the cycle will be treated as non-cacheable.

In addition, non-cacheable regions can be user-defined in a look-up table within the VL82C325. Non-cacheable regions can be established in 2KB increments in area A (between 512KB and 1MB), and in 64KB increments in area B (below 512KB or above 1MB). Immediately following power-on reset, all of memory is configured to be cacheable.

It may also be necessary to declare certain areas of memory write-protected. For example, when caching ROM. Two mechanisms are provided for the definition of write-protected regions.

The first is a dedicated input signal to the controller. The user may decode write-protected addresses outside the controller, and provided that the –WPCYC signal is asserted with the correct timing, then the cycle will be treated as write-protected.

In addition, write-protected regions can be user-defined in a look-up table within the cache controller. Write-protect regions can be established in 2KB increments in area A (between 512KB and 1MB). Write-protect regions cannot be established in area B of system memory. Immediately following power-on reset, all of memory is configured to be non-write-protected.

Prior to enabling the VL82C325 by setting the CENA bit, in the Cache Configuration Register the bits corresponding to the non-cacheable regions and to write-protect regions should be set, as desired, in the Non-Cache Table (NCT) and in the Write-Protect Table (WPT) respectively.

Prior to setting up the NCT/WPT, the NCTPGM bit in the Cache Control Register (CCTRL) must be set to a 1 to enable programming of the tables. After all non-cache areas and write-protect areas are defined, NCTPGM should be cleared and the NCTENA, bit of the CCTRL, should be set to enable the NCT/WPT comparators. Table 4 shows how the NCT/WPT tables interact with the W/–R, –NCCYC, and –WPCYC pins and with the NCTENA bit in the CCTRL Register.

TABLE 4. NCT/WPT INTERACTION WITH OTHER SIGNALS

W/–R	–NC CYC	–NCT ENA	NCT	Cacheable (?)	–WP CYC	NCT ENA	WPT	Writeable (?)
1	X	X	X	Y	0	X	X	N
0	0	X	X	N	1	0	X	Y
0	1	0	X	Y	1	1	0	Y
0	1	1	0	Y	1	1	1	N
0	1	1	1	N				

TABLE 5. NCT/WPT (AREA A) DEFINITION

512KB ≤ MAIN MEMORY ADDRESS < 1M

Offset (hex)	Non-Cache Region Starting Address in hex, A23-A0							
	D7	D6	D5	D4	D3	D2	D1	D0
00	081800		081000		080800		080000	
01	083800		083000		082800		082000	
•	•		•		•		•	
•	•		•		•		•	
•	•		•		•		•	
3E	0FD800		0FD000		0FC800		0FC000	
3F	0FF800		0FF000		0FE800		0FE000	
							WPT	NCT

TABLE 6. NCT (AREA B) DEFINITION

MAIN MEMORY ADDRESS < 512KB or ≥ 1M

Offset (hex)	Non-Cache Region Starting Address in hex, A-23-A16							
	D7	D6	D5	D4	D3	D2	D1	D0
00	07	06	05	04	03	02	01	00
01	Not Used (see Area A)							
02	17	16	15	14	13	12	11	10
03	1F	1E	1D	1C	1B	1A	19	18
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1E	F7	F6	F5	F4	F3	F2	F1	F0
1F	FF	FE	FD	FC	FB	FA	F9	F8

CPU AND TOPCAT INTERFACES

386SX PROCESSOR INTERFACE

The VL82C325 monitors the 386SX bus cycle definition signals to determine which cycles it can service totally (memory reads from cache data RAM) or must participate in (cache-miss, etc.). Figure 4 illustrates the interconnect between the processor and the VL82C325. The processor and the VL82C325 share the same CLK2 signal.

The VL82C325 has two reset input signals. RSTDRV is used as the global power-on reset signal within the VL82C325 and when it is asserted, it causes all the internal registers and state machines to assume their initialization state. Any data stored in an internal register, directory, or NCT will be lost and must be restored after RSTDRV has been negated. RSTCPU is used to synchronize the VL82C325's internal processor state machines to CLK2 and the 386SX processor. Asserting RSTCPU with RSTDRV not asserted does not initialize the VL82C325's Configuration/Control Registers, directory or NCT.

The 386SX processor's Next Address Request (–NA) input may be driven according to the rules of the 386SX CPU. The VL82C325 does not control –NA, but it will operate both in pipelined and in non-pipelined modes.

When one of the VL82C325's internal registers is referenced by the 386SX, the peripheral data bus is used for the data transfer (XD bus). I/O read and write cycles are used for these transfers; all of which execute with slot bus type cycle timing.

VL82C320A SYSTEM CONTROLLER INTERFACE

The system controller is responsible for executing all on-board cycles (DRAM). When a cycle misses in the cache, the system contoller may have to complete the cycle. In order to minimize the average wait states of miss cycles, the VL82C320A System Controller starts to decode the cycle even before the VL82C325 indicates a miss. The VL82C325 issues the –MISS signal to the system controller which then aborts the cycle on a cache-hit or allows the system controller to continue on miss and write cycles.

During a read-hit, the VL82C325 will provide the READY to terminate the cycle. However, for cycles which complete in the system controller, the system controller must terminate the cycle. The CPU's READY input signal indicates to the VL82C325 that the cycle is complete and that the data is available on the data bus (read cycles). The VL82C325 can then negate the write strobe to the cache data memories to update the cache during cacheable read-misses.

The VL82C325's internal configuration registers are accessed via I/O reads and writes. During these cycles, the data is transferred to/from the CPU by means of the peripheral data bus (XD7-XD0 bus). The VL82C325's Configuration Registers are not accessible during DMA cycles, but may be made accessable in Master Mode DMA cycles by connecting the –MASTER input signal.

VL82C331 BUS CONTROLLER INTERFACE

The bus controller is responsible for executing all off-board cycles (includes ROM and I/O cycles which are considered off-board). When a cycle misses in the cache, the bus controller may have to complete the cycle. The bus controller is not connected to the VL82C325's –MISS signal, so it can not tell whether the cycle was a hit or a miss. However, it is "slaved" to the system controller, and so the system controller will not command the bus controller on cache-hit cycles.

During read-miss cycles the VL82C325 requires that a full 16-bit line be fetched, even if the CPU asked only for a single byte. The bus controller's byte enable inputs are generated by the VL82C325 (–BUSBE1 and –BUSBE0). The VL82C325 converts 8-bit read-misses to 16-bit reads by manipulating the bus controller's byte enables. The cycle is converted to 16-bit only if the address of the cycle is determined to be in a cacheable region. Tables 7 and 8 summarizes the conversions for various cycle types.

The VL82C325 also supplies the –EALE signal to the bus controller. This ensures that the bus controller samples the VL82C325 generated byte enables with the correct timing.

During HLDA cycles, the bus controller must control the CPU's byte enables. Therefore, the VL82C325 reverses the direction on its –BHE, –BLE, –BUSBE1, and –BUSBE0 pins; allowing the bus controller to drive the byte enables through the VL82C325.

HLDA writes which hit into the cache invalidate the cached line. The VL82C325 uses the –MEMW signal from the bus controller to detect these cycles. On the rising edge of –MEMW (when HLDA true), if the memory address hits in the cache, the cached line is invalidated.

FIGURE 4. CPU AND TOPCAT INTERFACES

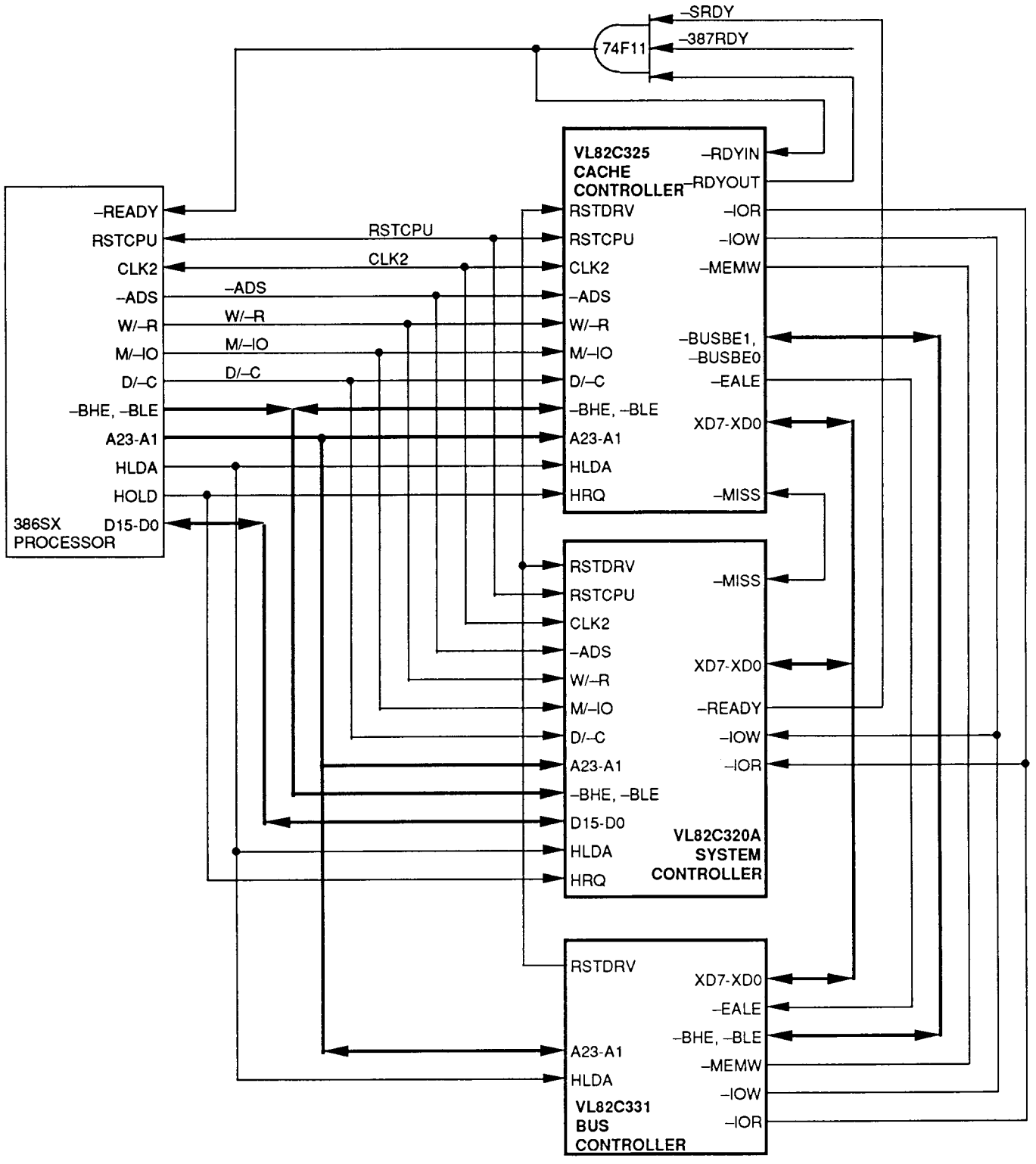


TABLE 7. 8-BIT TO 16-BIT CONVERSION - CPU CYCLES

Bus Cycle Type					
M/–IO	D/–C	W/–R	386 Cycle	Conditions	Size
0	0	0	INTA		
0	0	1	Undefined		
0	1	0	I/O Read		
0	1	1	I/O Write		
1	0	0	Memory Code Read	Code Fetch is Always 16-bit	16
1	0	1	Halt/Shutdown		
1	1	0	Memory Data Read	Non-Cache Cache	 Convert to16-bit
1	1	1	Memory Data Write		

TABLE 8. 8-BIT TO 16-BIT CONVERSION - HLDA CYCLES

Bus Cycle Type		
386 Cycle	Conditions	Size
Memory Read		
Memory Write		
I/O Read		
I/O Write		

CACHE DATA RAM INTERFACE

The VL82C325 directly controls the cache data RAMs with no external logic required. The interface is optimized for use with dual 4K x 16 cache data RAMs. Each RAM is capable of operating in a two-way set associative mode, with each set being 4K x 16-bit. Therefore, a 16KB cache can be implemented using only one RAM chip, or two chips for a 32KB cache.

The VL82C325 produces two chip enable signals, –CCE1 and –CCE0, one each for the least significant and most significant 16KB of RAM. –CCE1 is not used in the 16KB configuration.

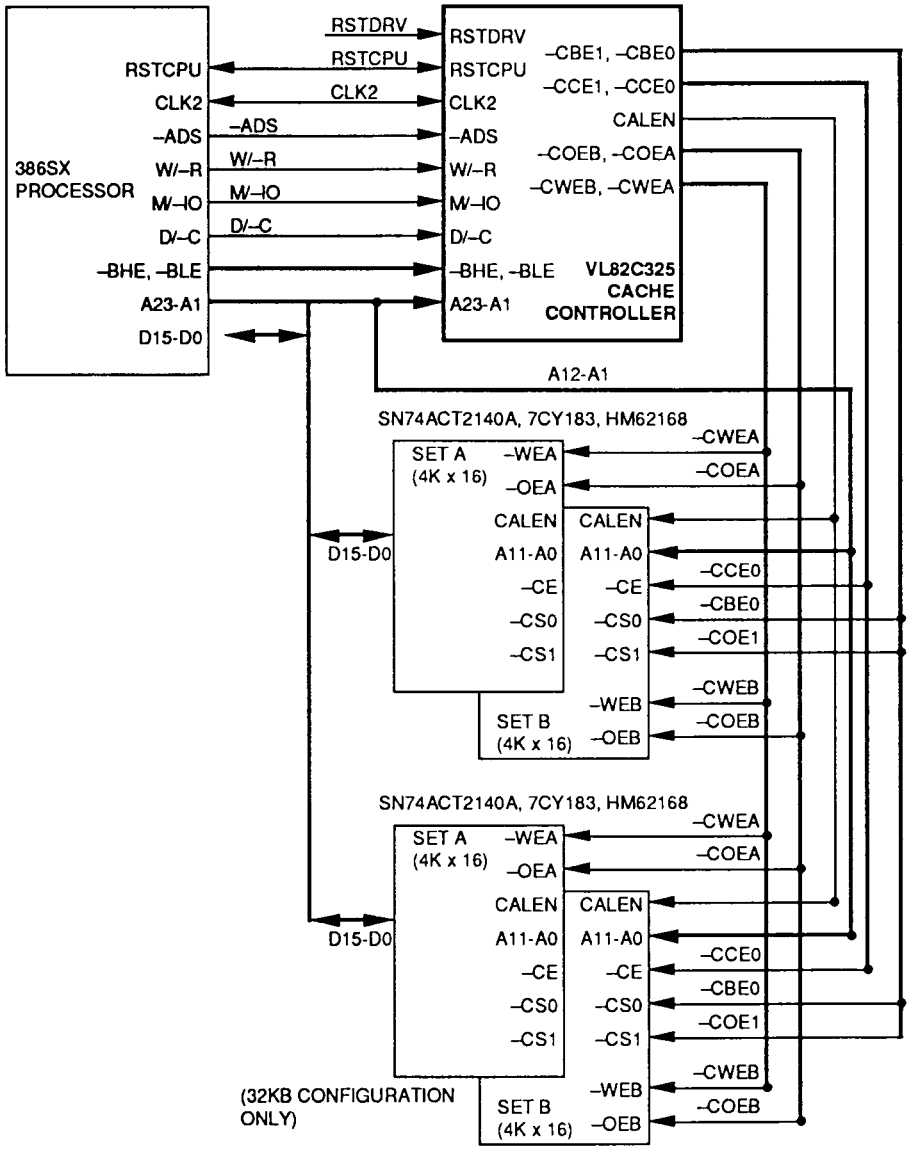
Two byte enables, –CBE1 and –CBE0, allow the cache data RAMs to perform byte write operations. –CBE0 is connected to the chip select inputs corresponding to the least significant byte of each cache data RAM (bits 0-7). –CBE1 enables the most significant byte (bits 8-15).

A read- or write-hit into set A causes set A to be read or written with –COEA or –CWEA respectively. Similarly for set B using –COEB or –CWEB.

The cache data RAMs have on-chip address latches which must be strobed. The processor's –ADS signal is unsuitable for this due to the pipelined mode of the 386SX. The VL82C325 produces the signal CALEN which is used to latch the cache data RAM addresses.

The data input/outputs of the RAMs are tied directly to the processor's data bus. This provides for the fastest possible access time to the data RAMs. Only during a read-hit are the data outputs enabled. The remainder of the time they are disabled, thus allowing normal operation of the processor data bus.

FIGURE 5. CACHE DATA RAM INTERFACE 16KB/32KB TWO-WAY SET ASSOCIATIVE



EMS/MEMORY MANAGEMENT WITH CACHE

Hardware EMS or other memory management schemes are commonly used to extend the physical memory capacity of computing systems. The VL82C320A System Controller and the VL82C310 SCAMP Controller include such an EMS capability. It is important to note the impact of hardware EMS upon a cached system.

EMS hardware resides between the CPU's address bus and that of physical memory. It translates the CPU's address before applying it to the physical memory. The CPU's address bus is often referred to as the physical address bus (particularly in CPU's such as the 386SX which have on-chip memory management). However, when hardware EMS is employed, the CPU's address bus is actually a virtual address bus.

The VL82C325 caches physical data, while the cache directory contains CPU addresses (virtual addresses if EMS employed). This is not a problem until, or unless, the virtual to physical translation algorithm is altered (reprogramming EMS Registers). This can cause the data in the cache data RAMs to become stale. It is therefore advised that either of the following strategies be used when hardware EMS is employed:

1. Ensure that the cache is flushed each time that memory is reconfigured. Note that to avoid spurious effects, it may be necessary to first disable the cache, then reconfigure memory, flush the cache, and then re-enable the cache.
2. Define EMS-controlled virtual memory regions to be non-cacheable (using NCT or the –NCCYC pin).
3. Enable the Auto-EMS Flush feature by setting the A_EMS bit in the Cache Configuration Register (CCR). This feature will cause the cache directory to automatically flush any time that a change to EMS Registers occurs (see the section titled "Flushing").

If two or more EMS pages map to the same physical memory page, then the cache data may become stale because the VL82C325 will not recognize that the addresses are equivalent. Data which is cached at one address may be written to another address and the cached data will not be updated. Avoid multiple mapped pages, or define such pages as non-cacheable.

If memory is managed using only the 386SX's on-chip memory management schemes, then the CPU's address is truly a physical bus and the above precautions are unnecessary.

Other less obvious factors can also disturb the cache. For example, changing the DRAM Configuration Registers RAMMAP and RAMMOV (in the system controller) will invalidate the cache contents. In general, never reconfigure memory without considering the cache. If in doubt, follow procedure #1 outlined above.

FLUSHING

A cache flush empties the cache. The next memory access is therefore guaranteed to miss. A flush does not alter the contents of cache data RAM, but simply invalidates all of cache data by clearing all of the VALID bits in the tag RAMs. A flush can be caused in any of the following three ways.

1) The –FLUSH input signal is driven low while the cache is enabled.
2) The software flush bit (FLUSH) in the Cache Control Register (CCR) is set to 1.
3) An EMS-update event occurs while the Auto-EMS-Flush enable bit (A_EMS) in the CCR is set to 1.

Flushing requires approximately 12 CLK2 cycles to complete. While the cache is flushing, it is automatically disabled and will issue a miss for any cycle which executes during the flush. If the cache was previously enabled, then it will automatically re-enable when the flush is completed.

If the cache is disabled at the time when the flush request occurs, then the flush will commence immediately. If, however, the cache is enabled, then the request pends until the next end of a T2 state (non-pipelined), the next end of a T1 state (non-pipelined) or the next end of a T1P state (pipelined). This ensures that the cache look-up for the cycle in progress is not interrupted. An interruption in the look-up could cause a false result.

–FLUSH: Hardware Flush Signal

The –FLUSH pin operates only when the cache is enabled. When the cache is disabled, the tag RAMs are available for the various tag RAM diagnostics operations (see the section titled "Testing"). This ensures that the –FLUSH pin will not interfere with testing.

The –FLUSH pin may be asserted synchronously or asynchronously. If asserted synchronously, it must meet the setup and hold requirements which are defined in the section titled "AC Characteristics". If asserted asynchronously, then it must meet the minimum pulse width requirement which is defined in the same section.

If –FLUSH is sampled low by the rising edge of CLK2 on or before the middle of state T2, then the flush will commence at the end of that T2 state. Otherwise, it will pend until the end of the next T2, T1, or T1P. Similarly for pipelined cycles, –FLUSH must be sampled low on or before the middle of T1P.

Software Flush

A software flush is initiated by setting the FLUSH bit in the CCR to a 1. Software flushes can be issued regardless of whether the cache is enabled or disabled. However, FLUSH will be ignored if the tag RAM is busy executing a diagnostic test. Issuing software flushes while running diagnostics is not recommended. First wait for the diagnostics test to complete.

FLUSH is a return-to-zero bit, i.e. when the flush operation is complete FLUSH will automatically return to 0.

Auto-EMS Flush

An Auto-EMS Flush will occur if an EMS-update event occurs while the Auto-EMS Flush enable bit (A_EMS) in the CCR is set to 1. This feature can be disabled by setting A_EMS to 0.

Updates to EMS Registers can require that the cache be flushed (see the section titled "EMS / Memory Management with Cache"). Hardware accomplishes an Auto-EMS Flush by automatically forcing the software FLUSH bit in CCR to a 1. Therefore, the

discussion on software flush given above applies here also. The following is a list of the EMS-update events which can cause an Auto-EMS Flush to occur.

1) An I/O read of E9 hex (EMS Active Set) register. This operation selects the standard EMS Register set.
2) An I/O write to E9 hex (EMS Active Set) register. This operation selects the alternate EMS Register set.
3) An I/O write to any of the following registers with Configuration Registers write-enabled.
   3.1) EMSEN1, EMS Enable 1 (ED hex with configuration index of 0B hex).
   3.2) EMSEN2, EMS Enable 2 (ED hex with configuration index of OC hex).
   3.3) EA hex (EMS data port low byte).
   3.4) EB hex (EMS Data port high byte).

TESTING

IN-CIRCUIT MODE

The –TRI input pin is provided to aid in the in-circuit testing of board-level designs. This is an active low input, which when true, causes all of the VL82C325's outputs to become three-stated. The in-circuit tester can then drive the VL82C325's pins to test other devices on the board.

In addition, the VL82C325 can be placed in a special In-Circuit Test (ICT) Mode. In this mode, input pins are mapped directly to output pins. This provides a relatively simple means of determining whether all pins have been correctly soldered and whether the component orientation is correct. There are many more inputs than outputs, so three maps (A, B, and C) are required to cover all inputs. The three inputs –NCCYC, –WPCYC, and –FLUSH select the map. Table 9 defines the map selection and the mapping of input pins to output pins in each map. All ICT input to ICT output paths invert so, e.g., in map A, XD0 gets the inverse of A16. Also RESCPU is ORed with –MASTER in map A, and HLDA is ANDed with HRQ in map C.

TABLE 9. ICT PIN MAP

Map A	Map B	Map C	ICT Inputs
1	0	0	–NCCYC
0	1	0	–WPCYC
0	0	1	–FLUSH

ICT Inputs	ICT Inputs	ICT Inputs	ICT Outputs
–IOW	–M/IO	–CWEA	–CBE1
–IOR	–ADS	–CWEB	–CBE0
–BUSBE1	–HIDRIVE	–COEA	–BHE
–BUSBE0	–CLK2	–COEB	–BLE
RESCPU or –MASTER	–BLKA20	CALEN	–CCE0
W/–R	–MEMW	–MISS	–CCE1
D/–C	–RDYIN	–RDYOUT	–EALE
A23	A15	A7	XD7
A22	A14	A6	XD6
A21	A13	A5	XD5
A20	A12	A4	XD4
A19	A11	A3	XD3
A18	A10	A2	XD2
A17	A9	A1	XD1
A16	A8	HLDA and HRQ	XD0

The following sequence is used to set or clear the ICT Mode.

1) Set the –TRI pin low.
2) Set XD0 high to set ICT Mode or set XD0 low to clear ICT Mode.
3) Simultaneously pulse –IOR and –IOW low for a minimum of 100 ns.

A hardware reset (RSTDRV) will also clear the ICT Mode.

TESTING MAIN MEMORY

Main memory can be tested with the VL82C325 installed. Simply disable the VL82C325 with the CENA bit in the Cache Configuration Register (CCR) (see the section titled "Summary of Programming Model" for more information). With the VL82C325 disabled, all accesses go directly to main memory.

TESTING NCT/WPT RAMS

The non-cacheable region table and write-protect region table are accessable through the VL82C325's programming registers NCT_INDX and NCT/WPT. These are read/write registers, so the tables may be tested through these ports. See the section titled "Summary of Programming Model" for more details.

TESTING CACHE DIRECTORY RAMS

The VL82C325 provides hardware to assist in the in-system testing of the on-chip cache directory RAMs. Built-in test logic automatically cycles through the tag RAMs performing data writes and read verify operations. The VL82C325 must be disabled (by clearing the CENA bit in the CCR Register) before attempting to run any of the tag RAM diagnostics tests. Six tests are available, of which four run in the background, i.e., once initiated they require no further user action to complete. Foreground tests require user action to complete (user must read RAMDATA). To run one of the tests, use the following procedure:

1) Disable the cache by clearing the CENA bit in CCR.
2) Select from the six tests by programming the TR_OPCODE field in TSR.
3) If required, write 20-bit data pattern to RAMDATA.
4) Start the test by setting the TRDIAG bit in CCTRL.
5) For background tests: Poll the TRDIAG bit in CCR. When it returns to 0, the test is complete.

   For foreground tests: Read 20-bit data pattern from RAMDATA, and repeat until TRDIAG returns to 0.
6) If required, read the test-passed bits TPA and TPB in CCTRL. A 1 in TPA indicates that directory A passed the test; similarly a 1 in TPB indicates that directory B passed.

Background tests can be left running while the system is performing other tasks such as testing the main system memory. Table 10 summarizes the six available tests, and gives approximate execution times for background tests.

Write

Writes RAMDATA to every location of each directory. This test in conjunction with the following (read-verify) is used to test the cache flush mechanism. "Write" is used to preload the directory RAMs with RAMDATA, then a software flush should be executed by setting the FLUSH bit in CCR.

A flush invalidates every line in the cache by clearing all of the VALID bits (four or eight depending on the mode).

TABLE 10. CACHE DIRECTORY TESTS

TR_OPCODE (Bin)	Description	Time (μs)	
		20 MHz	25 MHz
00100	Write: Writes RAMDATA to every location.	77	62
00010	Read-verify: Read every location and verify that the contents are equal to RAMDATA with the MS 10 bits "flushed".	77	62
00110	Writes and Read-verify: Writes and verifies RAMDATA and the inverse of RAMDATA to every location.	410	330
00111	Write Checkerboard and Read-verify: Similar to previous test but alternates the pattern at adjacent addresses.	410	330
01000	Dump Tag Directory A: A diagnostic dump of the contents of tag directory RAM A.		
01000	Dump Tag Directory B: A diagnostic dump of the contents of tag directory RAM B.		

The VALID bits are active low so they are flushed to high. In fact, the most significant (MS) 10 bits of each location in each directory are flushed.

Then a "read-verify" test should be executed. That test will read every location of each directory and verify that the MS 10 bits were flushed and that the LS (least significant) 10 bits are still equal to the LS 10 bits of RAMDATA.

Read-Verify
This test will read every location of each directory and verify that the MS 10 bits were flushed and that the LS 10 bits are equal to the LS 10 bits of RAMDATA. This test, in conjunction with the previous, (write) is used to test the cache flush mechanism.

Write and Read-Verify
Writes and verifies RAMDATA and the inverse of RAMDATA to every location of each directory according to the flow diagram in Figure 6.

Write Checkerboard and Read-Verify
Writes and verifies RAMDATA and the inverse of RAMDATA to every location of each directory according to the flow diagram in Figure 7.

Directory Dump (A or B)
Dumps the contents of one directory RAM. This is a foreground test, i.e., it does not operate totally automatically like the background tests do. The user is required to read the directory data from the RAMDATA Register. Three reads are required to obtain all 20 bits of a single RAM location (see the section titled "Summary of Programming Model"). 1024 locations must be dumped (3072 reads). ALL 3072 reads must be performed or the test will not complete.

FIGURE 6. WRITE & READ-VERIFY, FLOW DIAGRAM

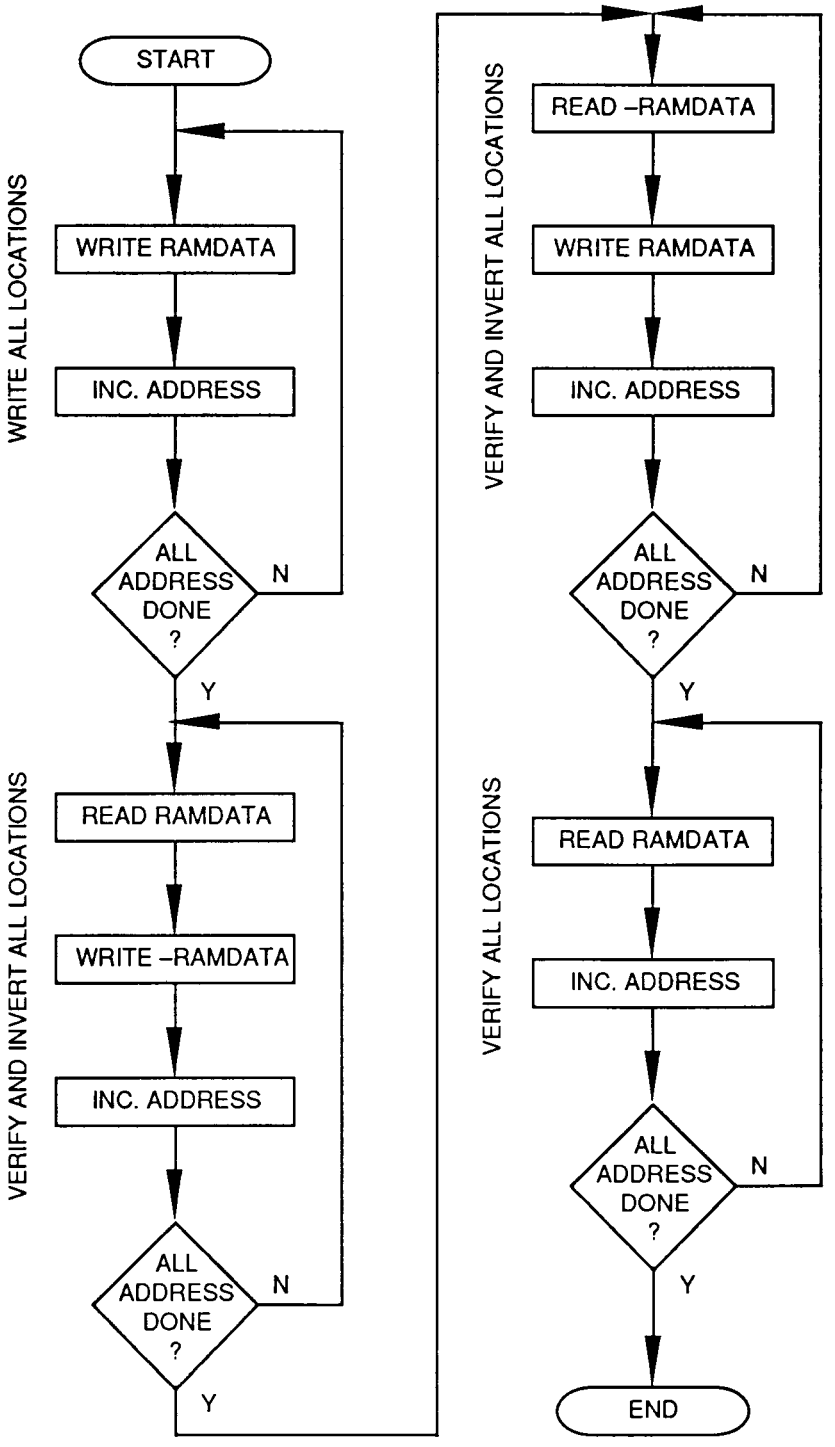
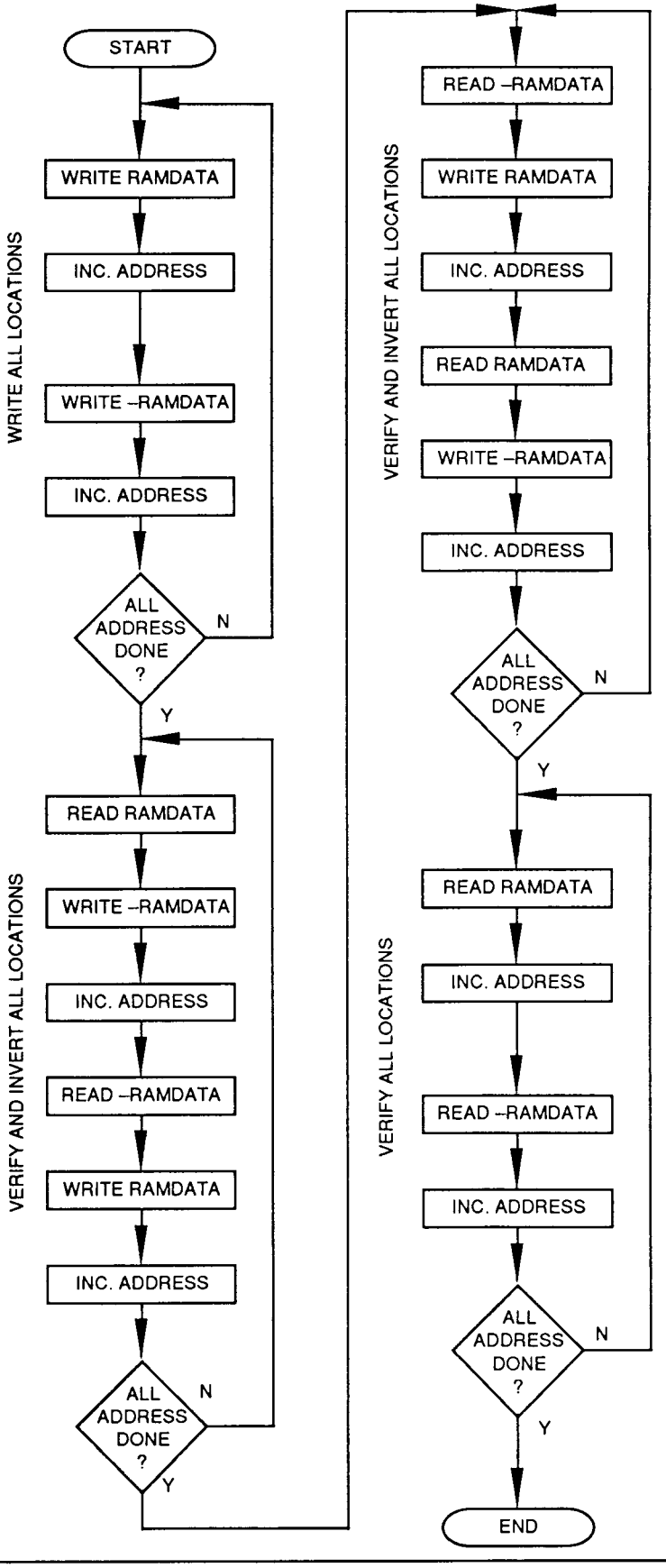


FIGURE 7. WRITE CHECKERBOARD & VERIFY, FLOW DIAGRAM



TESTING CACHE DATA RAMS

Before testing the cache data RAMs, first flush the cache with the FLUSH bit in the CCR. This ensures that all of the VALID bits are cleared and that the LRU table is cleared. This enables the test to determine whether the failure occurred in set A or in set B. Blocks will first be allocated to set A, and then to set B, and then to the least recently used. Diagnosing to set A or B, is of course, only necessary if the cache data memory was created using different physical RAMs for each set.

It is important that the code which is executing the test of the cache data RAMs not interfere with the allocation of space in the RAMs. This code should therefore be located in a non-cacheable region. Similarly, any stack or variable space should be non-cacheable. A contiguous region of system memory space equal to or greater than the total cache data size should be set aside for the testing of the cache data RAMs. This region should be defined as cacheable.

Having flushed the cache, if the test routine then sequentially reads every location in the cacheable region, starting at offset 0 and ending at offset Cache Data Size-1, then an image of the cacheable region will be copied directly into the cache. If the test now makes no further references to cacheable memory outside this region, then the VL82C325 will not re-allocate any of the cache data RAM space (because space can be allocated only on read-misses to cacheable regions). If this rule is obeyed, then the cache data RAM can be tested just like any normal static RAM. Figure 8 depicts the mapping of main memory to cache data RAM (for 16KB configuration) when the above rules are followed. Figure 9 depicts the mapping for the 32KB configuration.

FIGURE 8. TESTING CACHE DATA RAMS (16KB)

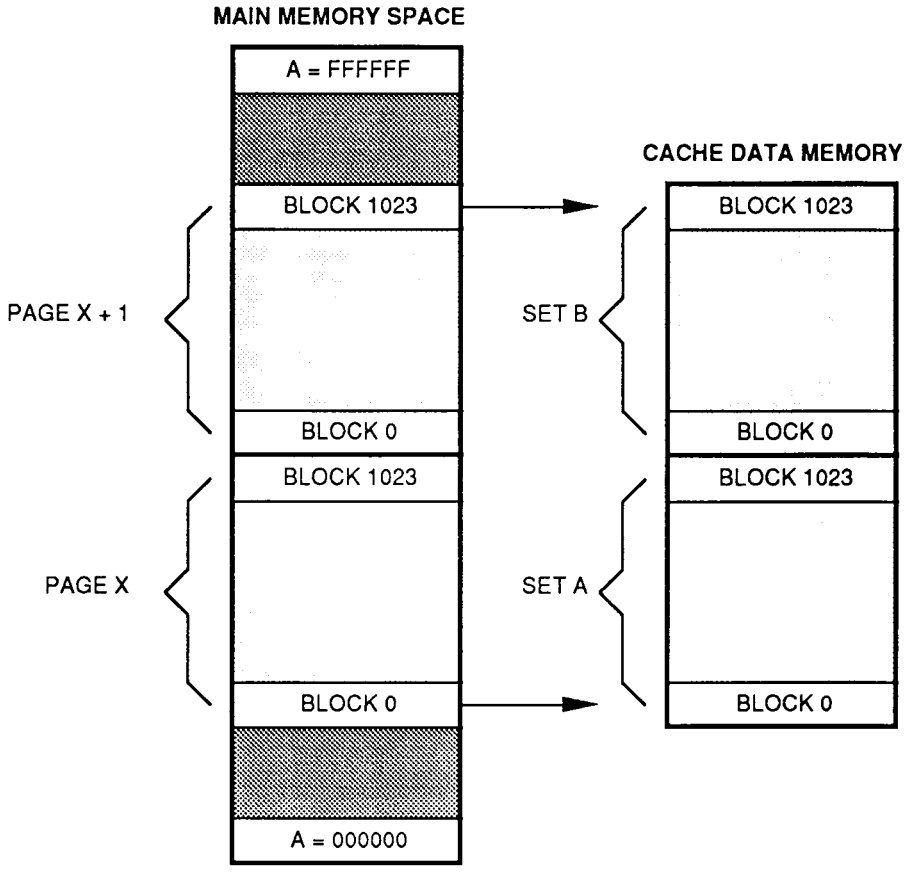
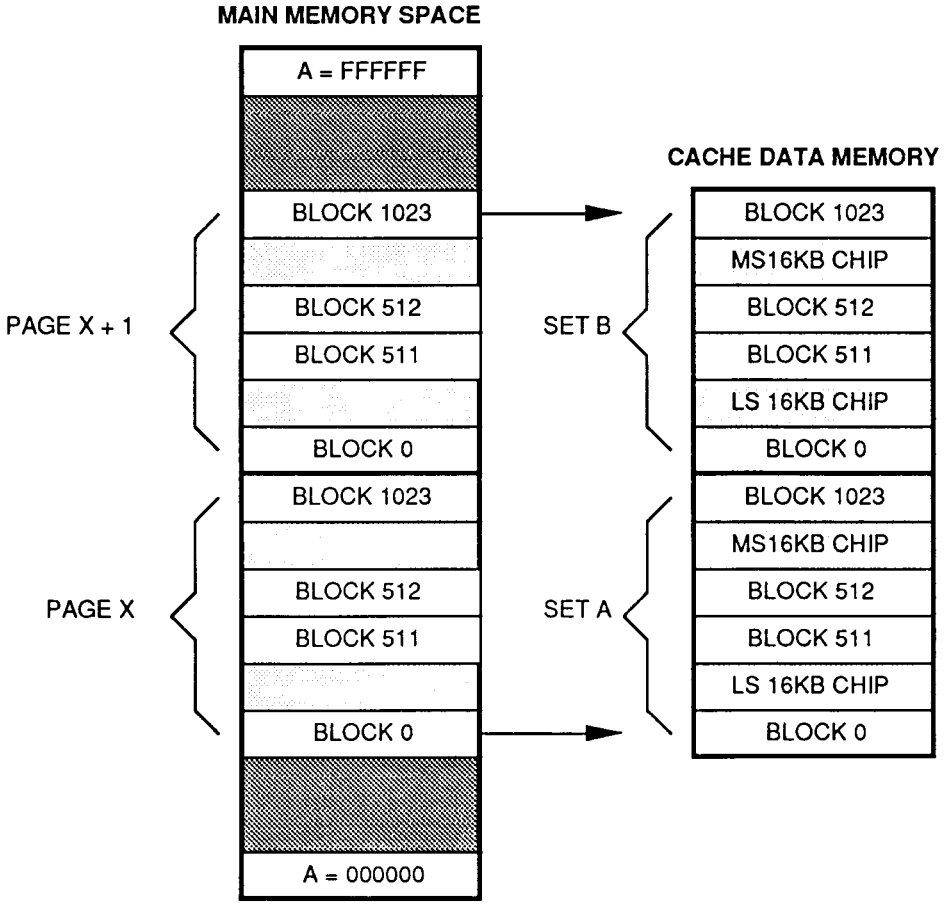


FIGURE 9. TESTING CACHE DATA RAMS (32KB)



DUMPING CACHE DATA RAMS

The current contents of the cache data RAMs can be dumped for diagnostic purposes. First, disable the cache by clearing the CENA bit in the CCR Register. No further allocation of cache can occur, so the cache data memory is now "frozen". Then set the BLOCK_CWE bit in the TSR Register. This blocks the cache write-enable outputs, preventing further writes to cache data RAM. Next re-enable the cache, then beginning with a cache flush, follow the directions in the section titled "Testing Cache Data RAMs" to re-allocate the cache directory map. The cache data RAMs can now be read using one of the memory maps depicted in Figures 8 and 9. A cache data RAM dump is most useful when preceded by a cache directory RAM dump. See the section titled "Testing Cache Directory RAMs".

SUMMARY OF PROGRAMMING MODEL

The VL82C325 is configured via ten 8-bit I/O registers. Four other 8-bit I/O ports (Access Control Registers) are required to control the access to the Configuration Registers. Finally, three other TOPCAT/SCAMP Registers are monitored for the Auto-EMS Flush feature, but no data is retained in the VL82C325 for these registers.

Except where otherwise noted, all accesses to these registers must be 8-bit accesses. Cycles complete with slot bus timing. A register indexing scheme allows many Configuration Registers to occupy only a very small region of I/O space. It is the same mechanism which is employed in the VL82C320A System Controller, VL82C310 SCAMP Controller, and VL82C331 Bus Controller and is an extension of their register spaces.

Table 11 is a summary of the Access Control Registers. Eight Configuration Registers are mapped to the TOPCAT/SCAMP Indexed Configuration Register Table and two (NCT_INDX, NCT/WPT) are mapped to the TOPCAT/SCAMP Indexed EMS Register Table. The Access Control Registers allow the user to select the appropriate indices into these two register tables. They also permit the write-protection of the VL82C325's Configuration Registers. They are all write-only registers.

Note that before accessing any VL82C325 register in indexed EMS space, the correct index value (24 hex) must be written into EMS_INDX. Similarly, before accessing any VL82C325 register in indexed configuration space, the correct index value (06, 14, 28-2F hex) must be written into CFG_INDX.

When the configuration is complete, it is recommended that the registers be write-protected by writing to CFG_DIS. This helps to prevent inadvertent changes to the VL82C325's setup parameters. Write-protection can be removed by writing to CFG_EN.

Table 12 lists those VL82C325 registers which reside in indexed EMS space, and Table 13 lists those which reside in indexed configuration space. Table 14 lists the additional Auto-EMS Flush Registers (no data is retained in these registers; see the section titled ("Auto-EMS Flush").

TABLE 11. ACCESS CONTROL REGISTER MAP

I/O Addr (hex)	R/W	Name	Description
E8*	W	EMS_INDX	EMS Index Register - 24 (hex) to access registers NCT_INDX and NCT/WPT. Other values access other TOPCAT/SCAMP EMS Registers.
EC*	W	CFG_INDX	Configuration Index Register - 06, 14, 28-2F (hex) to access VL82C325 registers. Other values access other TOPCAT/SCAMP Configuration Registers.
F9*	W	CFG_DIS	Configuration Disable - If special features are enabled, then any write will write-protect the registers in indexed configuration space and those in indexed EMS space.
FB*	W	CFG_EN	Configuration Enable - If special features are enabled, then any write will write-enable the registers in indexed configuration space and those in indexed EMS space.

*Shadow (local copy) of identical register in system controller.

TABLE 12. INDEXED EMS REGISTER MAP

EMS_INDX (hex)	R/W	Name	I/O Addr (hex)	Description
24	R/W	NCT_INDX	EA	NCT Index Register
	R/W	NCT/WPT	EB	Non-Cache and Write-Protect Tables

TABLE 13. INDEXED CONFIGURATION REGISTER MAP

EMS_INDX (hex)	R/W	Name	I/O Addr (hex)	Description
06*	W	REFCTL	ED	Refresh Control Register
14*	W	MISCSET		Miscellaneous Set Register
28	R/W	CCR		Cache Configuration Register
29	R/W	CCTRL		Cache Control Register
2A	R/W	TSR		Test Status Register
2B	R/W	RAMDATA		Tag RAM Data Register
2C	R	EMS_IMG		EMS_INDX Image Register
2F	R	VER		Version Register

*Shadow (local copy) of identical register in system controller.

TABLE 14. MONITORED AUTO-EMS REGISTERS

EMS_INDX (hex)	R/W	Name	I/O Addr (hex)	Description
		EMS_SET	E9 **	EMS Active Set Register
0B **		EMSEN1	ED	EMS Enable1 Register
0C **		EMSEN2		EMS Enable2 Register

**System controller registers (see the section titled "Auto-EMS Flush").

The following sections describe the individual registers and bit functions. In the tables, the "RSTDRV/INTRST" column indicates how that bit or field is affected by a hardware reset (RSTDRV pin) and a software reset (INTRST bit in the CCTRL Register) operation. That is, 0/0 indicates that the bit is set to 0 by either operation, while 1/- indicates that the bit is set to 1 by hardware resets but is unaffected by software resets.

TABLE 15. EMS INDEX REGISTER (EMS_INDX) (I/O Address E8 (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
5-0	W	0/-	INDEX-EMS (5-0)	Index into Indexed-EMS Register table. Must be 24 (hex) to access the VL82C325's registers NCT_INDX or NCT/WPT.
6	W	0/-	A_INC-EMS	Auto-increment INDEX-EMS (5-0). When 1, each access (read or write) to I/O address EB (hex) (the EMS data port) will increment INDEX-EMS (5-0) at the end of the cycle. Since the VL82C325 occupies only one index in the Indexed-EMS Register Table, this bit will usually be set to a 0 when accessing the VL82C325.
7	W		Reserved	Unused.

TABLE 16. CONFIGURATION INDEX REGISTER (CFG_INDX) (I/O Address EC (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
7-0	W	0/-	INDEX-CF (7-0)	Index into Indexed Configuration Register Table. Must be 06, 14, 28-2F (hex) to access the VL82C325's registers.

INDEXED-EMS REGISTERS

The non-cacheable region and write-protect region tables are accessed through a single Indexed EMS Register. Indexed EMS Registers are 16-bit registers. They may be accessed as 16-bit word-aligned registers or as two separate 8-bit registers. The VL82C325's Indexed EMS Register is comprised of the two 8-bit registers NCT_INDX (EA hex) and NCT/WPT (EB hex). These two registers are used to implement a second level of indexing within the VL82C325.

When accessing the NCT through these registers, the value in the Index Register (NCT_INDX) determines the offset within the tables (see Table 17), while the register NCT/WPT represents the value of the table entry at that offset. NCT_INDX should be programmed with the desired index value prior to accessing NCT/WPT. NCT_INDX can be configured to auto-increment on each access to the NCT/WPT Register (by setting the A_INC_EMS bit in the CCR). This speeds-up operations which read or write contiguous regions of the tables. (Note that writes will not auto-increment NCT_INDX if the Configuration Registers have been write-protected.) Alternately, it is possible to perform a single 16-bit I/O write to EA/EB while providing both the index and the data simultaneously. This latter mechanism is most useful when only a few scattered entries in NCT/WPT need to be programmed.

A hardware reset (RSTDRV pin) will reset all of NCT/WPT to 0. A software reset (INTRST bit in the CCTRL) will do the same.

Warning! The VL82C325 must be disabled (by setting CENA to 0 in the CCR) before attempting to write or read the NCT. Accessing the NCT with the cache enabled may produce unpredictable results.

TABLE 17. INDEXED NCT/WPT MAP

NCT_INDX (hex)	Which Table	Offset (hex)
00	NCT/WPT	00
:	Area A	:
:	512KB - 1MB	:
3F		3F
40	NCT	00
:	Area B	:
:	< 512KB or ≥ 1MB	:
5F		1F
60	Not used	N/A
:		
:		
FF		

INDEXED CONFIGURATION REGISTERS

TABLE 18. REFRESH CONTROL REGISTERS (REFCTL) (Configuration Index 06 (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
2-0	W			Not used in VL82C325. See system controller specification.
3	W	0/0	TENBIT	10/16-bit I/O address. When 1, only the least ten I/O address bits are decoded (A9-A0). When 0, A15-A0 are decoded. This bit shadows the identical bit in the REFCTL Register of the system controller.
7-4	W			Not used in VL82C325. See system controller specification.

TABLE 19. MISCELLANEOUS SET (MISCET) (Configuration Index 14 (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
6-0	W			Not used in VL82C325. See system controller specification.
7	W	0/0	FX_EN	Special features enable. When 1, special features are enabled. Special features must be enabled in order to utilize the Access Control Registers CFG_DIS and CFG_EN (configuration write-protect and configuration write-enable, respectively). This bit shadows the identical bit in the MISCSET Register of the system controller.

TABLE 20. CACHE CONFIGURATION REGISTER (CCR) (Configuration Index 28 (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
1-0	R/W	0/0	CS1, CS0	Cache Size 1, Cache Size 0. These two bits select the cache size. 0,0 = 16 KB; 0,1 = 32 KB; 1,0 = reserved; 1,1 = reserved. Warning: Never reconfigure cache size with cache enabled. Always disable the cache by setting CENA to 0.
2	R/W	1/1	FLUSH	Cache Flush. This bit, when set, clears all the VALID and LRU bits in the cache directories. This effectively empties the cache. Setting this bit to a 1 initiates the flush operation. Once the cache directories are cleared, this bit is returned to 0.
3	R/W	0/0	CENA	Cache Enable. The VL82C325 is enabled by setting this bit to a 1 and is disabled by writing this bit with a 0. Warning: If the cache is not empty, or if tag RAM diagnostic tests have been run, then the cache should be flushed before re-enabling.
4	R/W	0/0	A_INC_NCT	Auto-increment NCT_INDX. When 1, an access to the NCT/WPT Register (includes reads and writes) will auto-increment the Index Register NCT_INDX at the end of the access. Note that writes will not auto-increment NCT_INDX if Configuration Registers have been write-protected. Reads will auto-increment NCT_INDX regardless of write-protection.
5	R/W	0/0	A_EMS	Auto-EMS Flush. When 1, the Auto-EMS flush feature is enabled. (See the section titled "Auto-EMS Flush".)
6	R		TENBIT	10-Bit I/O. A read-only bit returning the state of the TENBIT bit in the REFCTL Register.
7	R		FX_EN	Special Features. A read-only bit returning the state of the FX_EN bit in the MISCSET Register.

TABLE 21. CACHE CONTROL REGISTER (CCTRL) (Configuration Index 29 (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
0	R/W	0/0	NCTPGM	Non-Cacheable Table Program Enable. Setting this bit to a 1 enables the NCT/WPT Registers to be written into. Clearing this bit, locks the NCT/WPT Registers. NCT/WPT can be read regardless of the state of bit NCTPGM. Warning: The VL82C325 must be disabled (by setting CENA to 0 in the CCR) before attempting to write or read the NCT. Accessing the NCT with the cache enabled may produce unpredictable results.
1	R/W	0/0	NCTENA	Non-Cache Table Enable. Setting this bit to a 1 enables the NCT/WPT to be used to exclude regions of memory from the cacheable memory space or to write-protect regions of memory. When this bit is cleared, and the CENA bit in the CCR is set, all system memory is cached and no memory is write-protected. Warning: The VL82C325 must be disabled (by setting CENA to 0 in the CCR) before attempting to write this bit. Changing the state of NCTENA with the cache enabled may produce unpredictable results.
2	R/W	1/-	INTRST	Internal Reset. This bit is used to reset the VL82C325. The reset operation commences when INTRST is set a 1. When the reset operation is completed, this bit is automatically returned to 0. Notice that INTRST causes a cache flush to occur (by setting the FLUSH bit in the CCR to 1). INTRST should not reset the EMS STD/Alternate-Set circuit. This circuit mimics TOPCAT/SCAMP and so should not be reset when a software reset is applied to only the cache. Always select the STD EMS-Set before software resetting the cache.
3	R/W	0/0	TRDIAG	Cache Internal Tag RAM Diagnostic Enable. If the cache is disabled, then the cache internal tag RAM diagnostic mode is entered when TRDIAG is set to a 1. As long as this bit remains a 1, then the diagnostic test is running. When the test completes, this bit is automatically returned to 0. Upon completion of the test, pass/fail results can be obtained from the TPA/TPB bits of this register. TRDIAG is ignored while the cache is enabled. INTRST does not terminate tag RAM diagnostics.
4	R		TPB	Test Passed B. This is a read-only bit. TPB returns the result of the tag RAM diagnostic test for set B. A 1 indicates that the test passed, a 0 indicates a fail. TPB is not valid until TRDIAG has returned to 0 (indicating that the test has completed.
5	R		TPA	Test Passed A. TPA returns the result of the tag RAM diagnostic test for set A. See TPB.
6	R		Reserved	Always returns 0 on read.
7	R		Reserved	Always returns 0 on read.

TABLE 22. TEST STATUS REGISTER (TSR) (Configuration Index 2A (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
4-0	R/W	0/0	TR_OPCODE	Tag RAM Diagnostic Opcode. The value in this field selects from one of the six tag directory RAM diagnostics test available. **Opcode (Bin) Test** 00100 Write 00010 Read-verify 00110 Write and read-verify 00111 Write checkerboard and read-verify 01000 Dump tag RAM, set A 10000 Dump tag RAM, set B Must be set to 00000 for normal cache operation. See the section titled "Testing Cache Directory RAMs" for more information.
5	R/W	0/0	BLOCK_CWE	Block CWE. When 1, the cache data RAM write-enables –CWEA and –CWEB are inhibited (forced high). This mode is used when generating a diagnostic dump of the cache data RAMs (see the section titled "Dumping Cache Data RAMs"). Must be 0 for normal cache operation.
6	R/W	0/0	Reserved	Must always write 0.
7	R/W	0/0	Reserved	Must always write 0.

TABLE 23. TAG RAM DATA REGISTER (RAMDATA) (Configuration Index 2B (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
7-0	R/W	-/-	TAGDATA	An 8-bit slice of the tag directory RAM data port. The data which is written to this port is written to the tag RAMs during the tag RAM diagnostics tests. Data is read from this port during tag RAM dump operarations. The tag RAMs are 20 bits wide. Three accesses to this register are required to access all 20 bits. Following a hardware reset (RSTDRV) or software reset (INTRST) this port will point to tag RAM data bits 7-0. Subsequent accesses will rotate through the data bus as follows: First access 07-00 Second 15-08 Third 23-16 (MS four bits not used) Fourth 07-00 Etc. ..... Alway access RAMDATA in triplets and in that way it will remain aligned on 7-0. See the section titled "Testing Cache Directory RAMs" for more information.

TABLE 24. EMS_INDX IMAGE REGISTER (EMS_IMG) (Configuration Index 2C (hex))

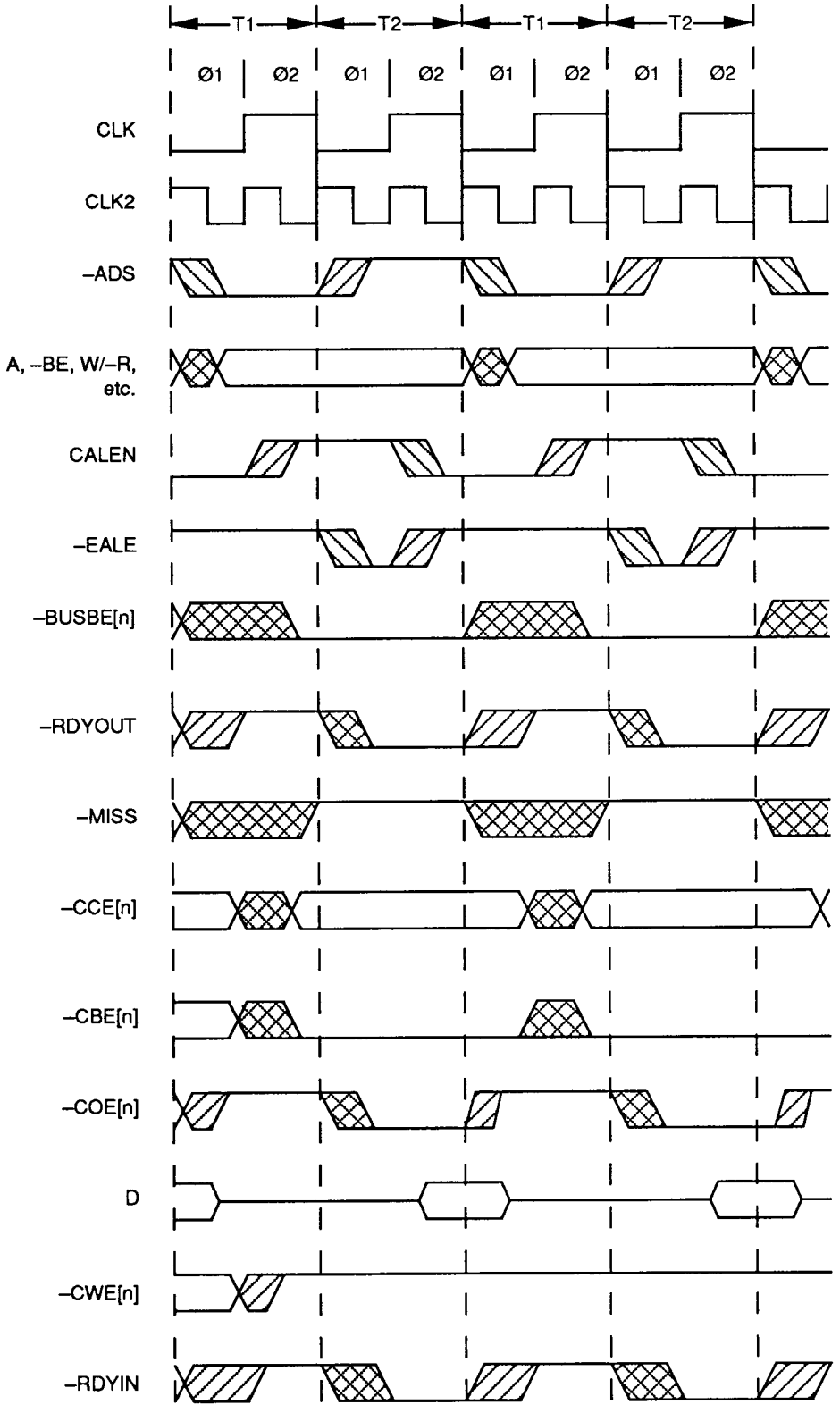
Bit	R/W	RSTDRV/ INTRST	Name	Description
5-0	R		INDEX-EMS (5-0)	Index into Indexed-EMS Register Table. A read-only field returing the state of the INDEX-EMS 5-0 field in the EMS_INDX Register.
6	R		A_INC-EMS	Auto-increment INDEX-EMS 5-0. A read-only bit returning the state of the A_INC-EMS bit in the EMS_INDX Register.
7	R		Reserved	Always returns 0.

TABLE 25. VERSION REGISTER (VER) (Configuration Index 2F (hex))

Bit	R/W	RSTDRV/ INTRST	Name	Description
7-0	R		VER	Version is a read-only register, returning the version code for this design revision. There is presently only one version code (0).

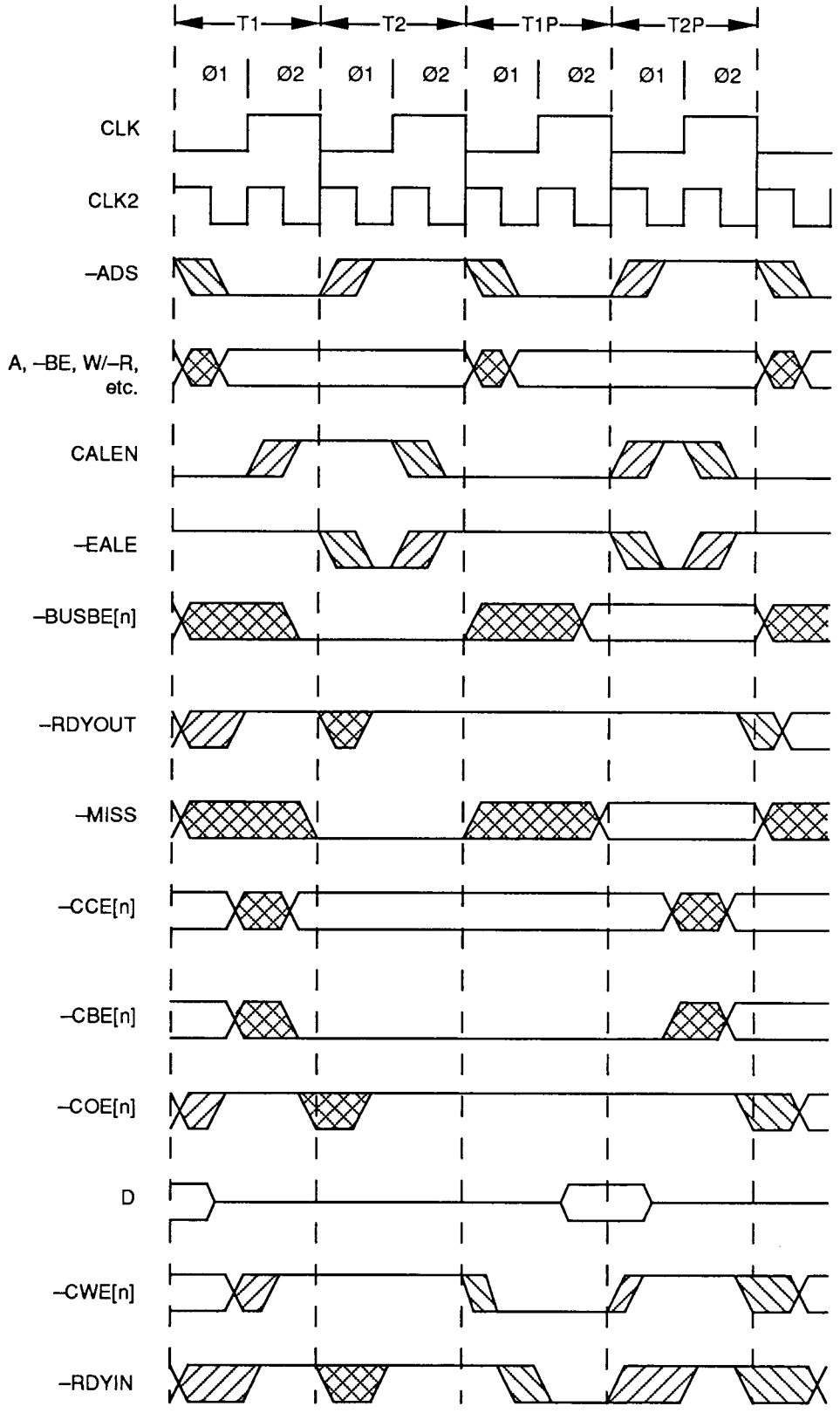
FUNCTIONAL TIMING DIAGRAMS

FIGURE 10. NON-PIPELINED READ-HIT



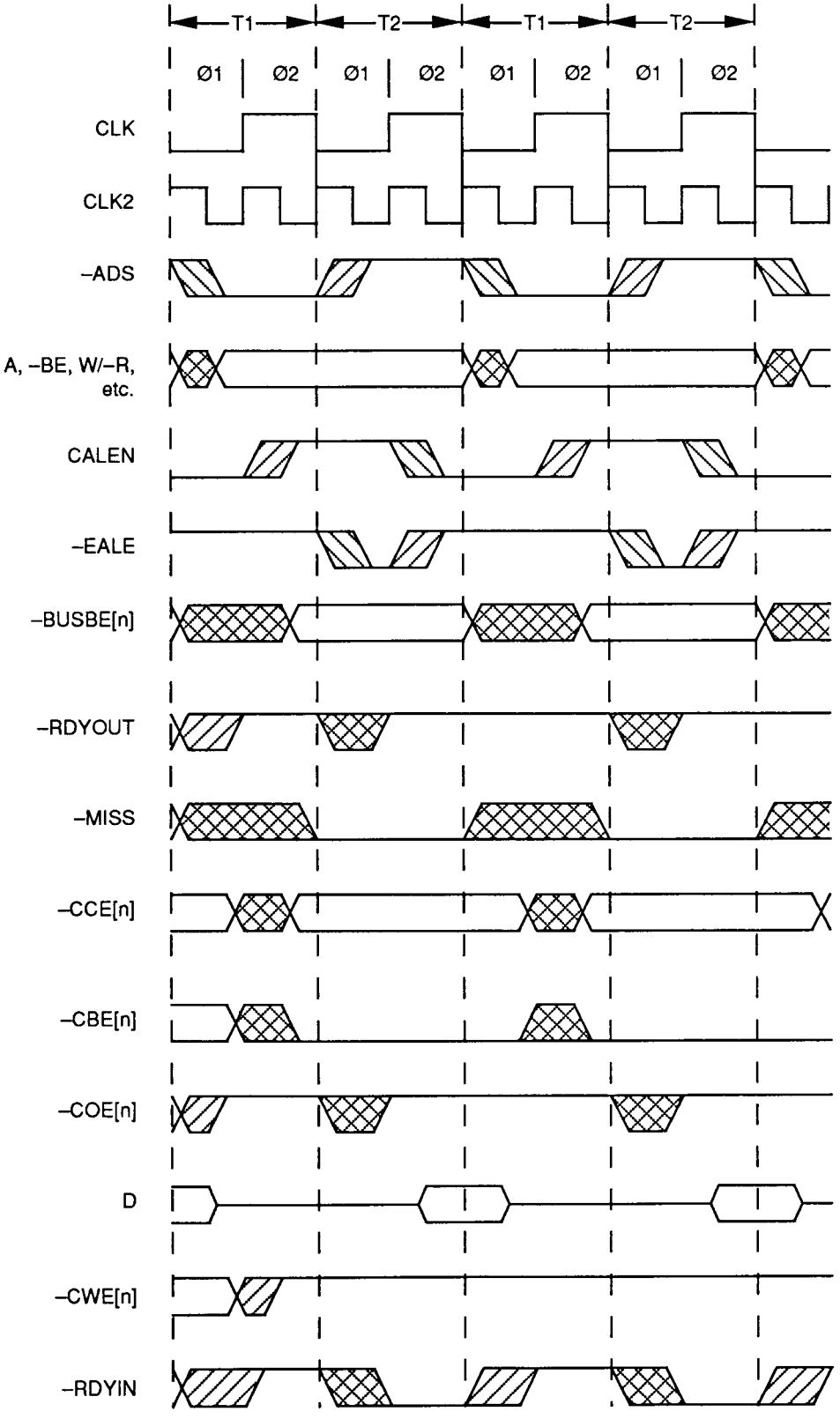
Note: Read-hits complete in zero wait states. –BUSBEs are low in cacheable read cycles. VL82C325 generates –READYOUT and one –COE on read-hits. –MISS is high (negated) on read-hits. –CBEs are low in all read cycles.

FIGURE 11. NON-PIPELINED READ-MISS CACHEABLE



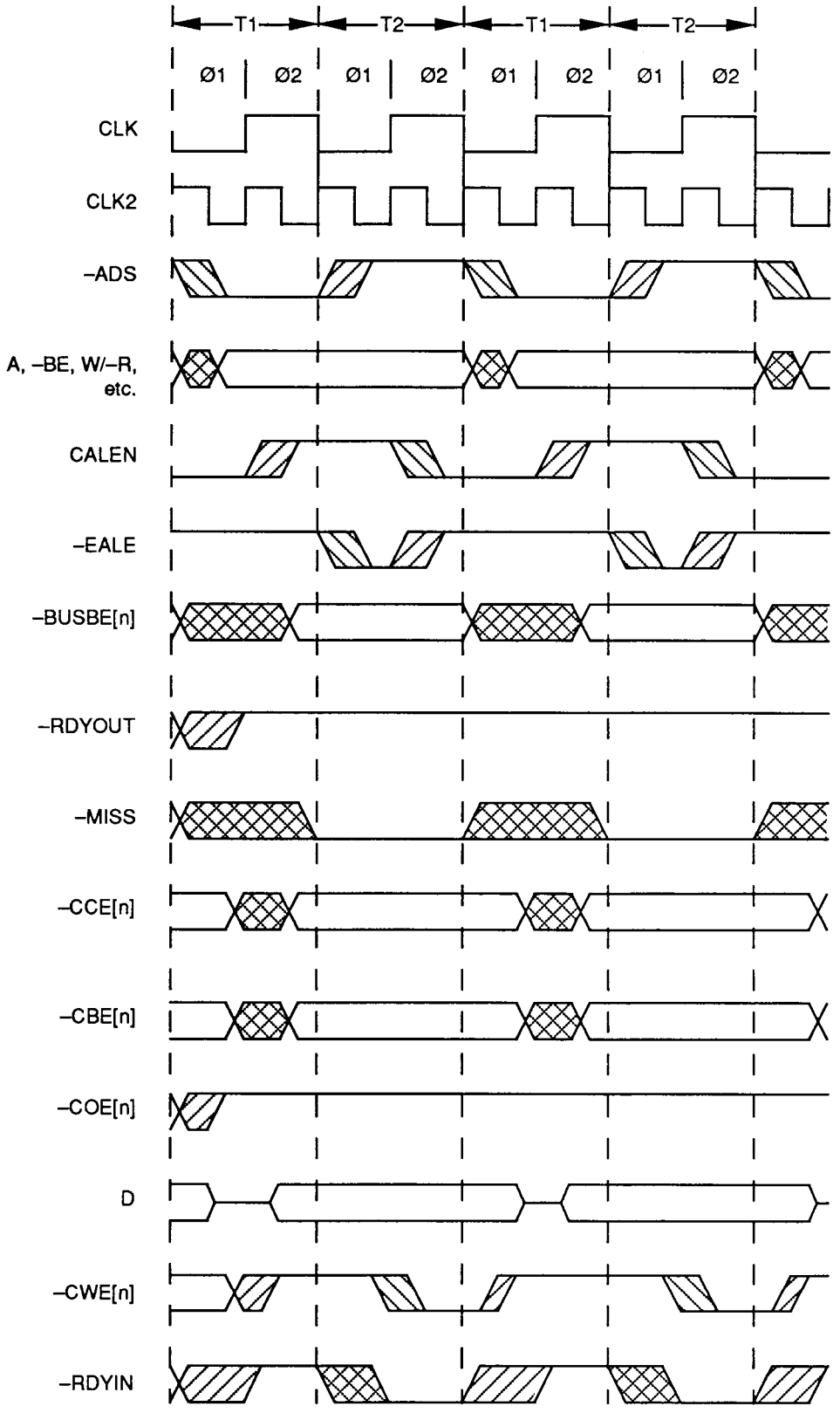
Note: Read-miss requires at least one wait state. –BUSBEs are low in cacheable read cycles. –READYOUT and –COE are undefined for a period in T2 before settling high. –MISS is low on read-miss. –CBEs are low in all read cycles. One –CWE is low after T2 (updates cache data RAM).

FIGURE 12. NON-PIPELINED READ NON-CACHEABLE



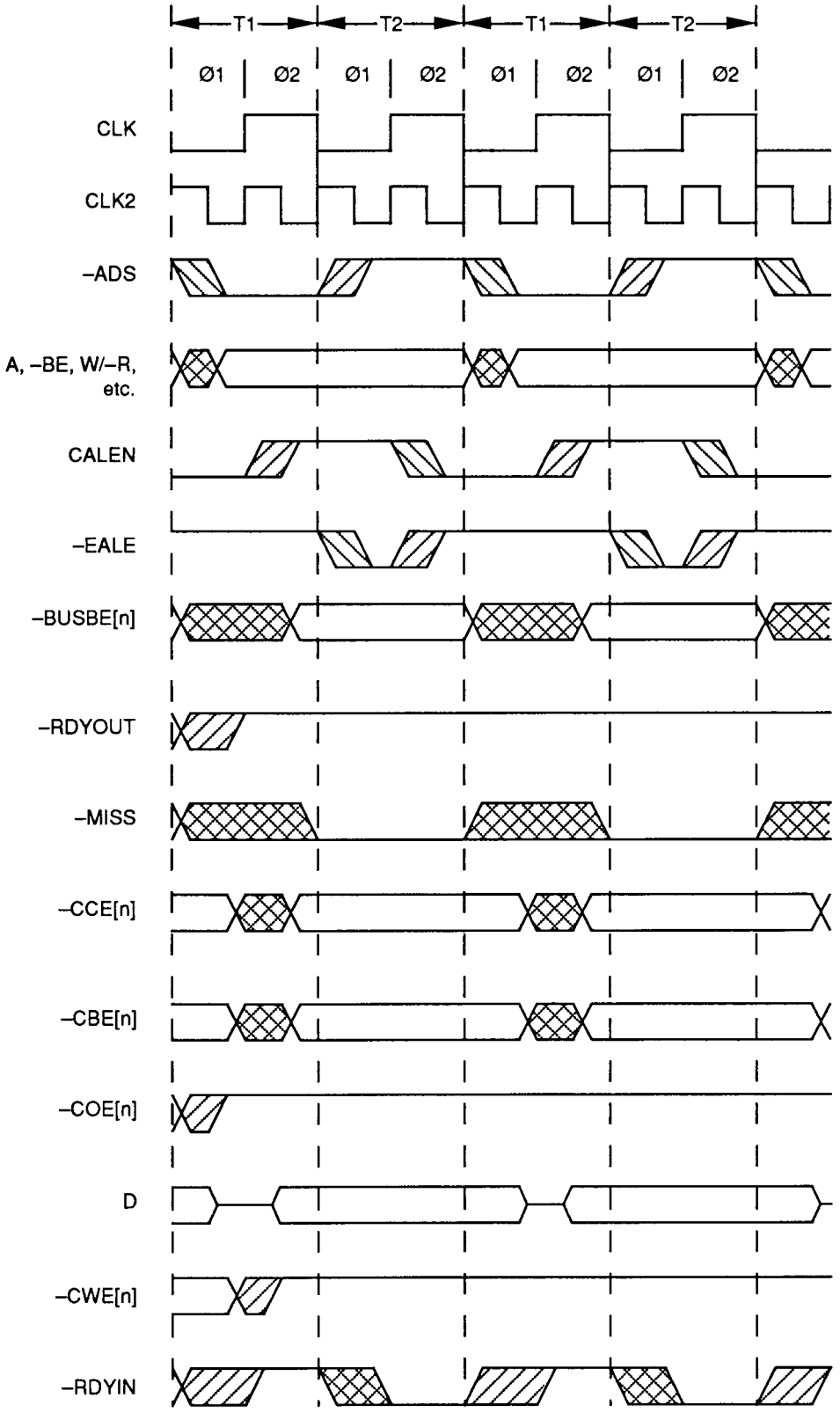
Note: Read non-cacheable may complete in zero wait states. –BUSBEs follow –BEs in non-cacheable cycles. –READYOUT and –COE are undefined for a period in T2 before settling high. –MISS is low in non-cacheable cycles. –CBEs are low in all read cycles.

FIGURE 13. NON-PIPELINED WRITE-HIT-WRITEABLE



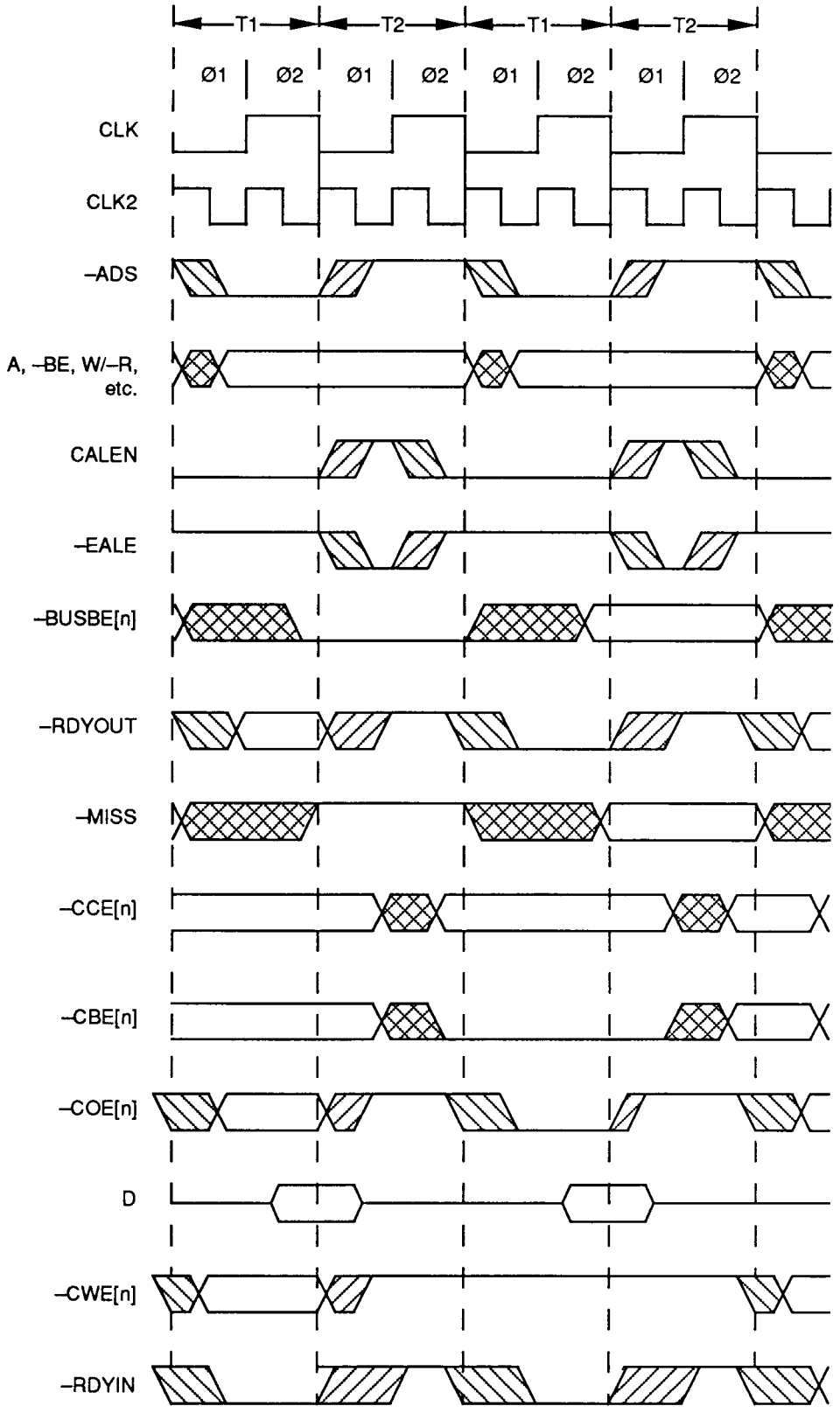
Note: Writes may complete in zero wait states. –BUSBEs follow –BEs in write cycles. –READYOUT and –COE are not generated. –MISS is low in write cycles. –CBEs follow –BEs in write cycles. One –CWE updates cache RAMs.

FIGURE 14. NON-PIPELINED WRITE-ALL-OTHERS



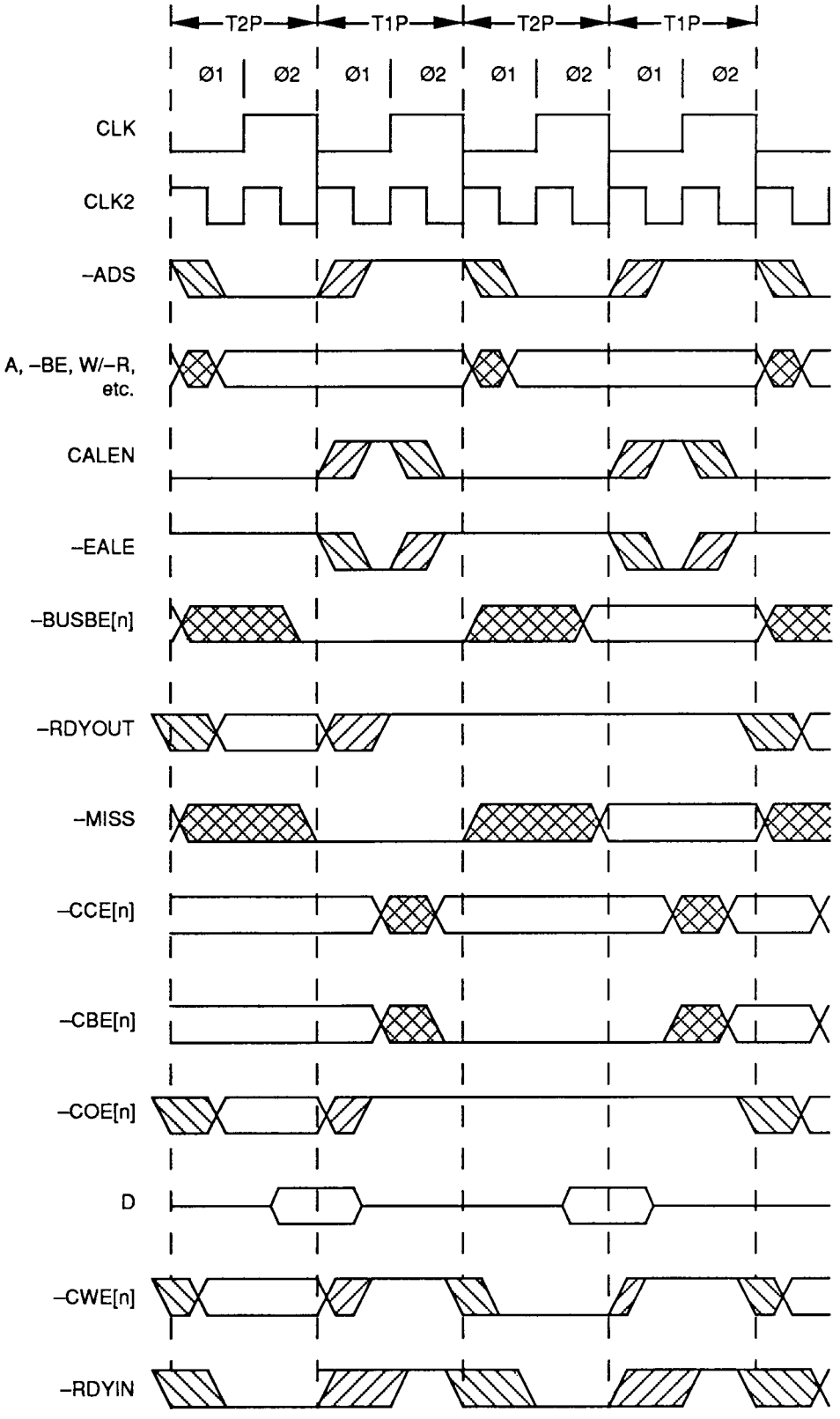
Note: Writes may complete in zero wait states. –BUSBEs follow –BEs in write cycles. –READYOUT, –COE, and –CWE are not generated. –MISS is low in write cycles. –CBEs follow –BEs in write cycles.

FIGURE 15. PIPELINED READ-HIT



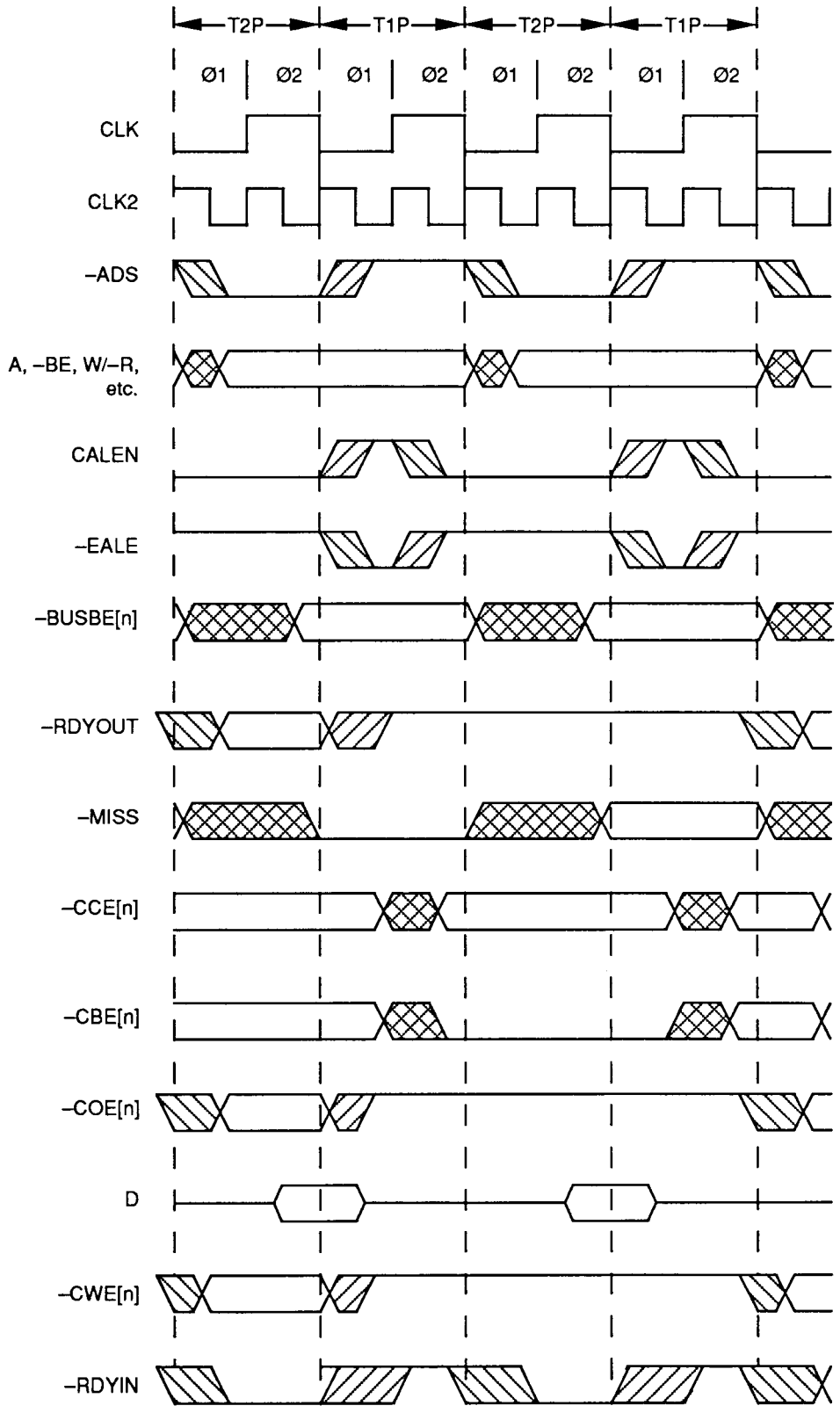
Note: Read-hits may complete in zero wait states. –BUSBEs are low in cacheable read cycles. VL82C325 generates –READYOUT and one –COE on read-hits. –MISS is high (negated) on read-hits. –CBEs are low in all read cycles.

FIGURE 16. PIPELINED READ-MISS CACHEABLE



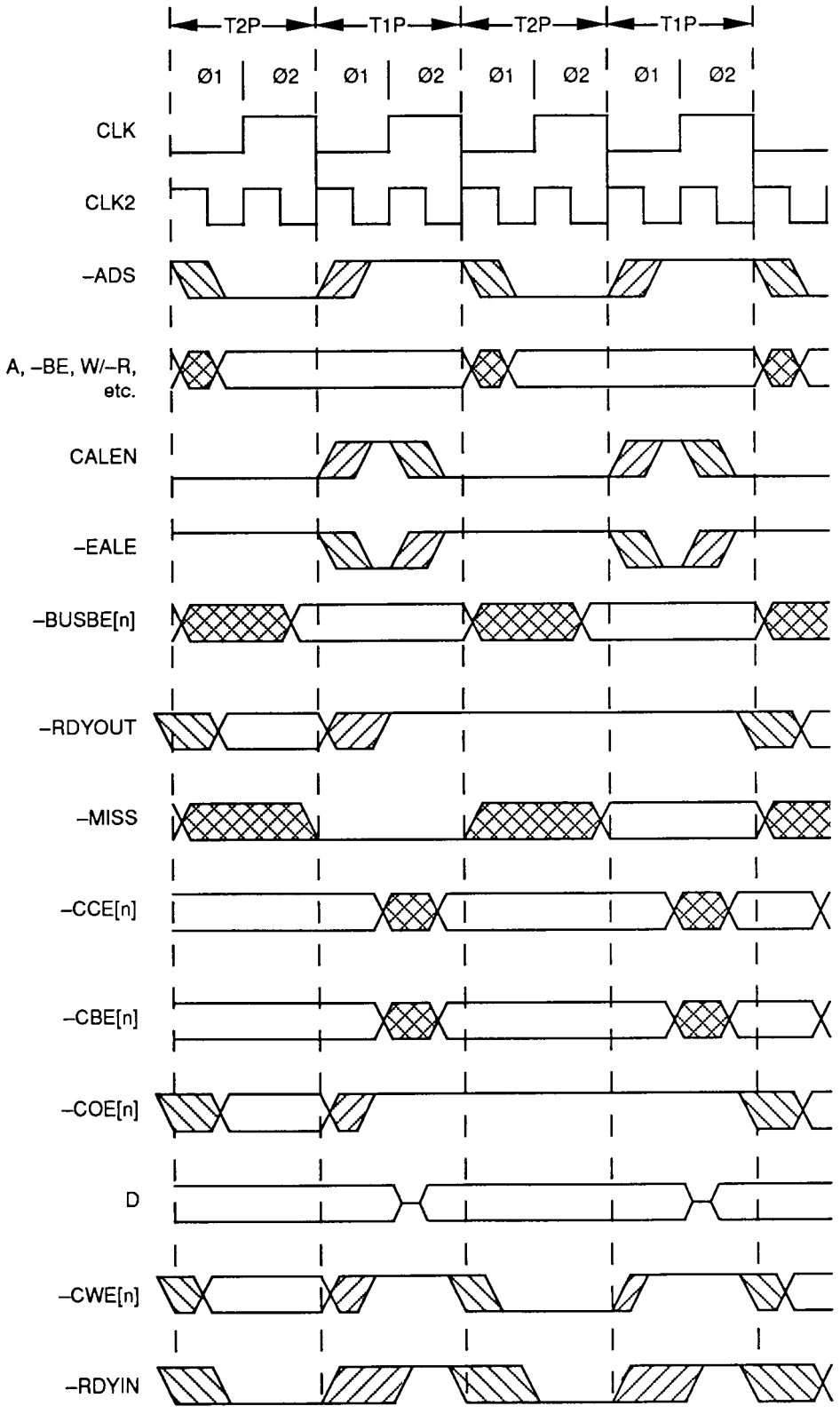
Note: Read-miss may complete in zero wait states. –BUSBEs are low in cacheable read cycles. –READYOUT and –COE are not generated. –MISS is low on read-miss. –CBEs are low in all read cycles. One –CWE is low after T1P (updates cache data RAM).

FIGURE 17. PIPELINE READ NON-CACHEABLE



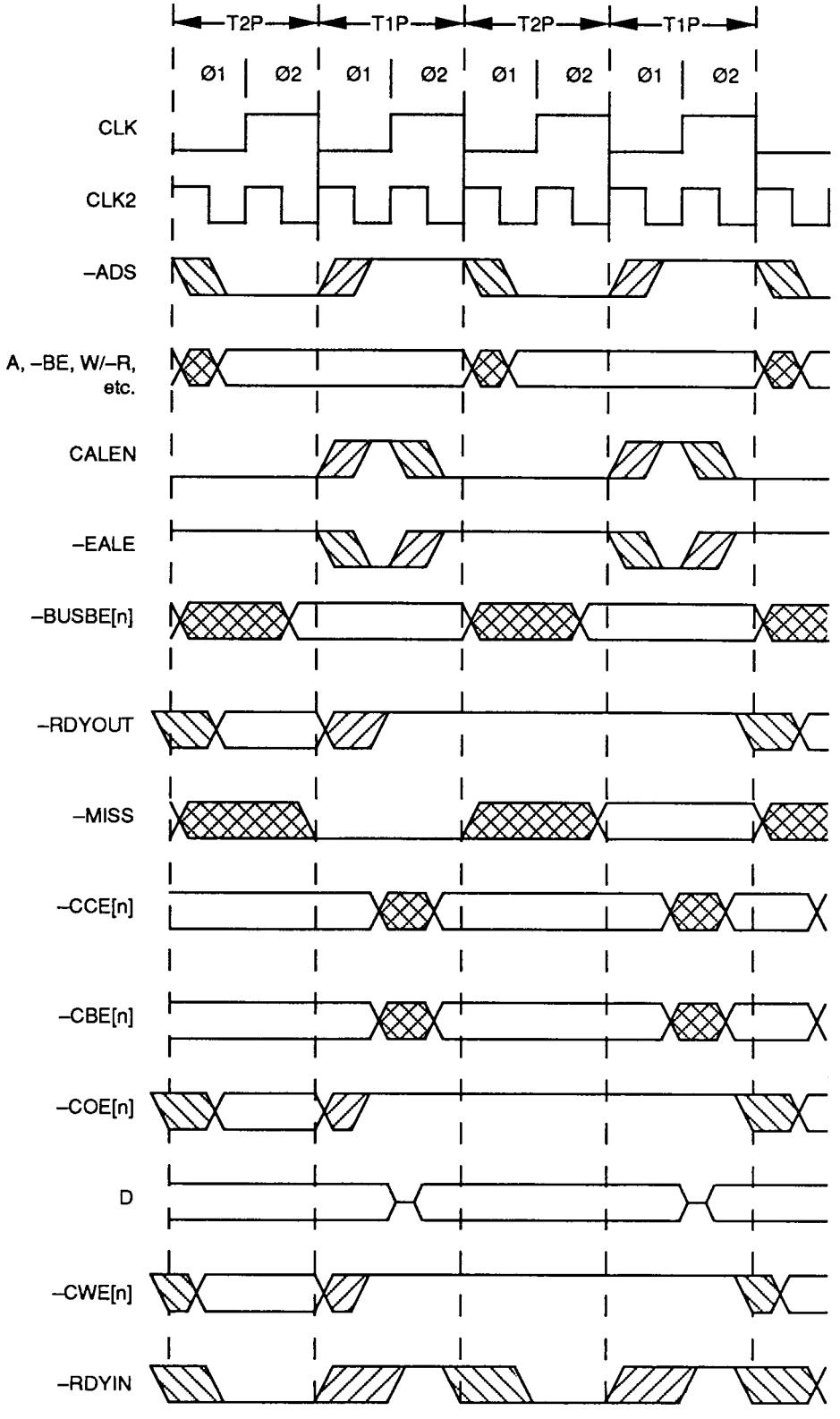
Note: Read non-cacheable may complete in zero wait states. –BUSBEs follow –BEs in non-cacheable cycles. –READYOUT and –COE are not generated. –MISS is low in non-cacheable cycles. –CBEs are low in all read cycles.

FIGURE 18. PIPELINED WRITE-HIT WRITEABLE



Note: Writes may complete in zero wait states. –BUSBEs follow –BEs in write cycles. –READYOUT and –COE are not generated. –MISS is low in write cycles. –CBEs follow –BEs in write cycles. One –CWE updates cache RAMs.

FIGURE 19. PIPELINED WRITE ALL OTHERS



Note: Writes may complete in zero wait states. –BUSBEs follow –BEs in write cycles. –READYOUT, –COE, and –CWE are not generated. –MISS is low in write cycles. –CBEs follow –BEs in write cycles.

AC CHARACTERISTICS

FIGURE 20. AC TEST LOADS

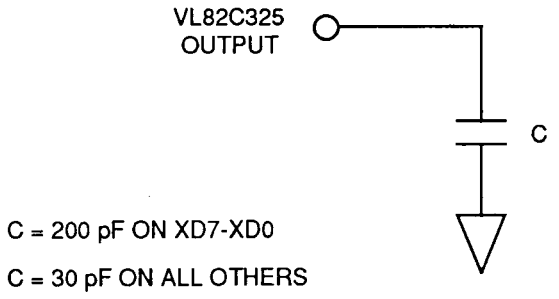


FIGURE 21. AC TEST WAVEFORMS

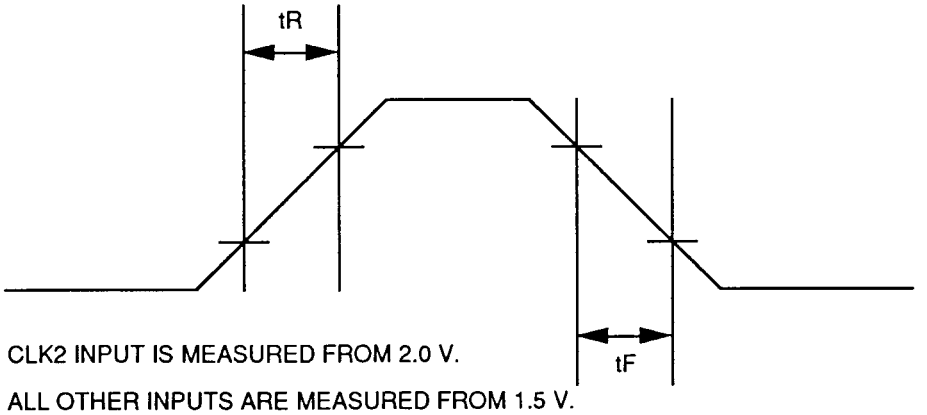
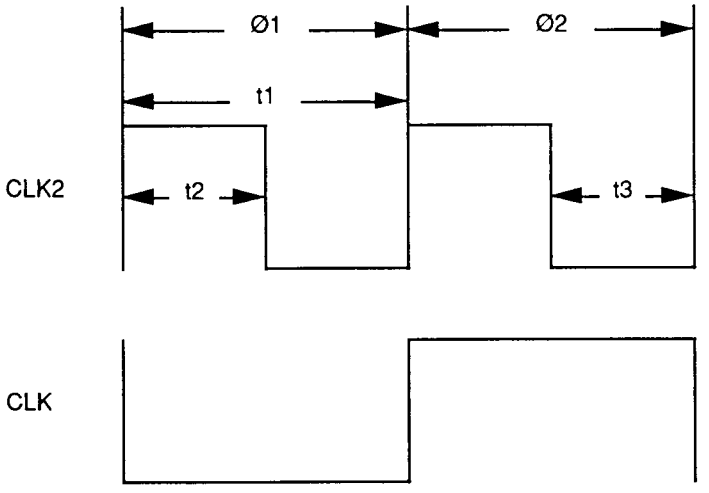


FIGURE 22. CLK2 TIMING



AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
fclk	Operating Frequency		25	MHz	
fclk2	CLK2 Frequency		50	MHz	
tR	CLK2 Rise Time		4	ns	
tF	CLK2 Fall Time		4	ns	
t1	CLK2 Period	20		ns	
t2	CLK2 Pulse Width High	8		ns	
t3	CLK2 Pulse Width Low	8		ns	
t5	A/–BLKA20 Valid to –RDYOUT Valid		31	ns	Note 10
t6	CLK2 High to –MISS Undefined	3	30	ns	
t7	A/–BLKA20 Valid to –MISS Valid		30	ns	
t8	CLK2 High to CALEN High	2	14	ns	
t9	CLK2 High to CALEN Low	2	14	ns	
t10	CLK2 High to –EALE Low	2	15	ns	
t11	CLK2 High to –EALE High	2	15	ns	
t12	A/–BLKA20 Valid to –COE Valid		30	ns	Notes 1 and 10
t14	CLK2 High to –COE High	3	12	ns	
t15	CLK2 High to –COE Low	0	13	ns	
t16	CLK2 High to –CWE High	2	8	ns	
t17	CLK2 High to –CWE Low	0	10	ns	
t18	CLK2 High to –CBE Invalid	0	15	ns	
t19	–BE Valid to –CBE Valid		15	ns	Note 2

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
t20	W/–R, M/–IO Valid to –CBE Valid		18	ns	
t21	–IOR Low to XD Low Impedance	0		ns	
t22	–IOR Low to XD Valid		50	ns	
t24	–IOR High to XD High Impedance		20	ns	
t25	–ADS Setup to CLK2 High	10		ns	
t26	–ADS Hold from CLK2 High	3		ns	
t27	A/–BLKA20 Setup to CLK2 High	30		ns	
t28	A/–BLKA20 Hold from CLK2 High	4		ns	
t29	–BE Setup to CLK2 High	30		ns	Note 2
t30	–BE Hold from CLK2 High	4		ns	Note 2
t31	M/–IO, D/–C, W/–R Setup to CLK2 High	15		ns	Note 12
t32	M/–IO, D/–C, W/–R Hold from CLK2 High	4		ns	
t33	–NCCYC Setup to CLK2 high	18		ns	
t34	–NCCYC Hold to CLK2 High	3		ns	
t35	–RDYIN Setup to CLK2 High	7		ns	
t36	–RDYIN Hold to CLK2 High	3		ns	
t37	XD Setup to –IOW High	30		ns	Note 6
t38	XD Hold to –IOW High	10		ns	Note 6
t39	CLK2 Low to –CWE High	2	8	ns	Note 3
t40	CALEN Pulse Width (t1 – 4)	(16)		ns	
t41	–EALE Pulse Width (Low) (t1 – 4)	(16)		ns	

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

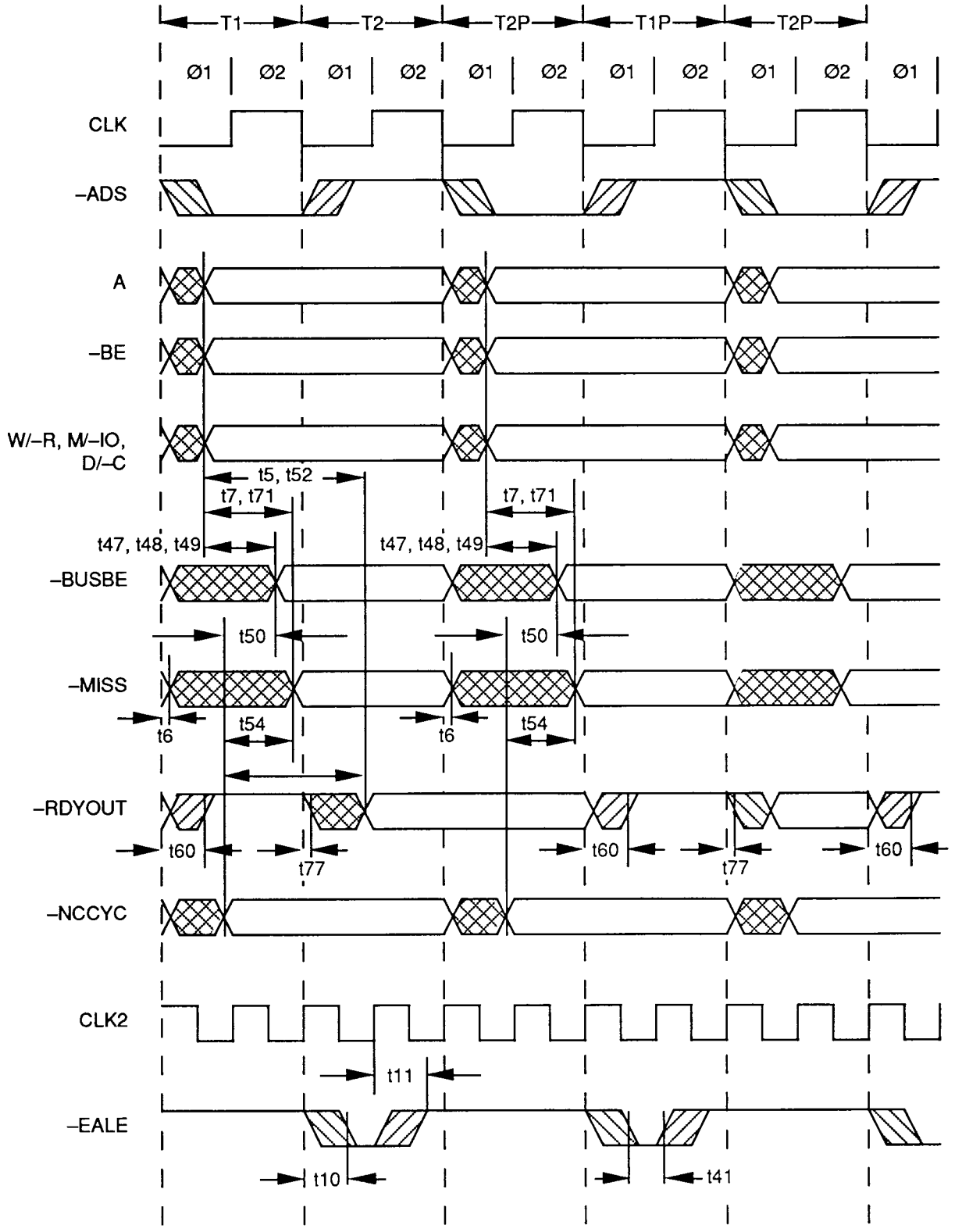
Symbol	Parameter	Min	Max	Unit	Conditions
t42	–CWE Pulse Width (Low) (t1 + t2 – 3)	(25)		ns	
t43	–CWE High to CALEN High Guaranteed Min	0		ns	
t44	CLK2 High to –CCE Invalid	0	16	ns	
t45	A/–BLKA20 Valid to –CCE Valid		16	ns	
t46	W/–R, M/–IO, D/–C Valid to –CCE Valid		16	ns	
t47	A/–BLKA20 to –BUSBE	0	28	ns	
t48	–BE to –BUSBE	0	15	ns	Note 2
t49	W/–R, M/–IO to –BUSBE	0	20	ns	Note 12
t50	–NCCYC to –BUSBE	0	12	ns	Notes 1 and 10
t51	–NCCYC Valid to –COE Valid		20	ns	Note 10
t52	R/–W, M/–IO Valid to –RDYOUT Valid		25	ns	Notes 10 and 12
t53	–NCCYC Valid to –RDYOUT Valid		20	ns	
t54	–NCCYC Valid to –MISS Valid		20	ns	
t55	–WPCYC Setup to CLK2 High	13		ns	
t56	–WPCYC Hold to CLK2 High	3		ns	
t57	A/–BLKA20 Setup to –MEMW Low	35		ns	Notes 4 and 12
t58	A/–BLKA20 Hold from –MEMW High	12		ns	Notes 4 and 12
t60	CLK2 High to –RDYOUT High	3	15	ns	
t61	–FLUSH Detup to CLK2 High	6		ns	Note 7
t62	–FLUSH Hold from CLK2 High	2		ns	Note 7
t63	–FLUSH Pulse Width (Low) (t1 + t61 + t62)	(28)		ns	Notes 8 and 12

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
t64	–BUSBE to –BE	0	10	ns	Notes 2 and 4
t65	HLDA High to –BE low Impedance	2	15	ns	Note 2
t67	HLDA low to –BUSBE low Impedance		15	ns	
t68	HLDA High to –BUSBE Float		12	ns	Note 11
t70	HRQ Low to –BE Float		12	ns	Notes 2 and 11
t71	W/–R, M/–IO, D/–C Valid to –MISS Valid		25	ns	Notes 12
t72	W/–R, M/–IO, D/–C Valid to –COE Valid		25	ns	Notes 10 and 12
t73	RSTDRV Setup to CLK2	7		ns	Notes 7 and 9
t74	RSTDRV Hold from CLK2	3		ns	Notes 7 and 9
t75	RESCPU Setup to CLK2	5		ns	
t76	RESCPU Hold from CLK2	2		ns	
t77	CLK2 High to –RDYOUT low	0	14	ns	

Notes:
1. Memory read cycles only. –COE remains high for all other cycles.
2. –BE refers to –BHE, –BLE.
3. Non-pipelined write-hits only.
4. HLDA cycles only.
5. Applies to I/O reads from the cache controller's internal registers.
6. Applies to I/O writes from the cache controller's internal registers.
7. For synchronous recognition.
8. For asynchronous recognition.
9. For asynchronous recognition: pulse width must exceed 2xt1 + t73 + t74. For synchronous recognition: must be sampled on two successive CLK2 rising edges.
10. Non-pipelined cycles only.
11. Three-state transition delay by sample measurement.
12. Validated by simulation.

FIGURE 23. TOPCAT INTERFACE TIMING



Note: The cycles depicted above are general. The first cycle depicted could have terminated in T2 (if it had been a hit). See functional timing for details of specific cycle types.

FIGURE 24. CACHE DATA RAM INTERFACE TIMING

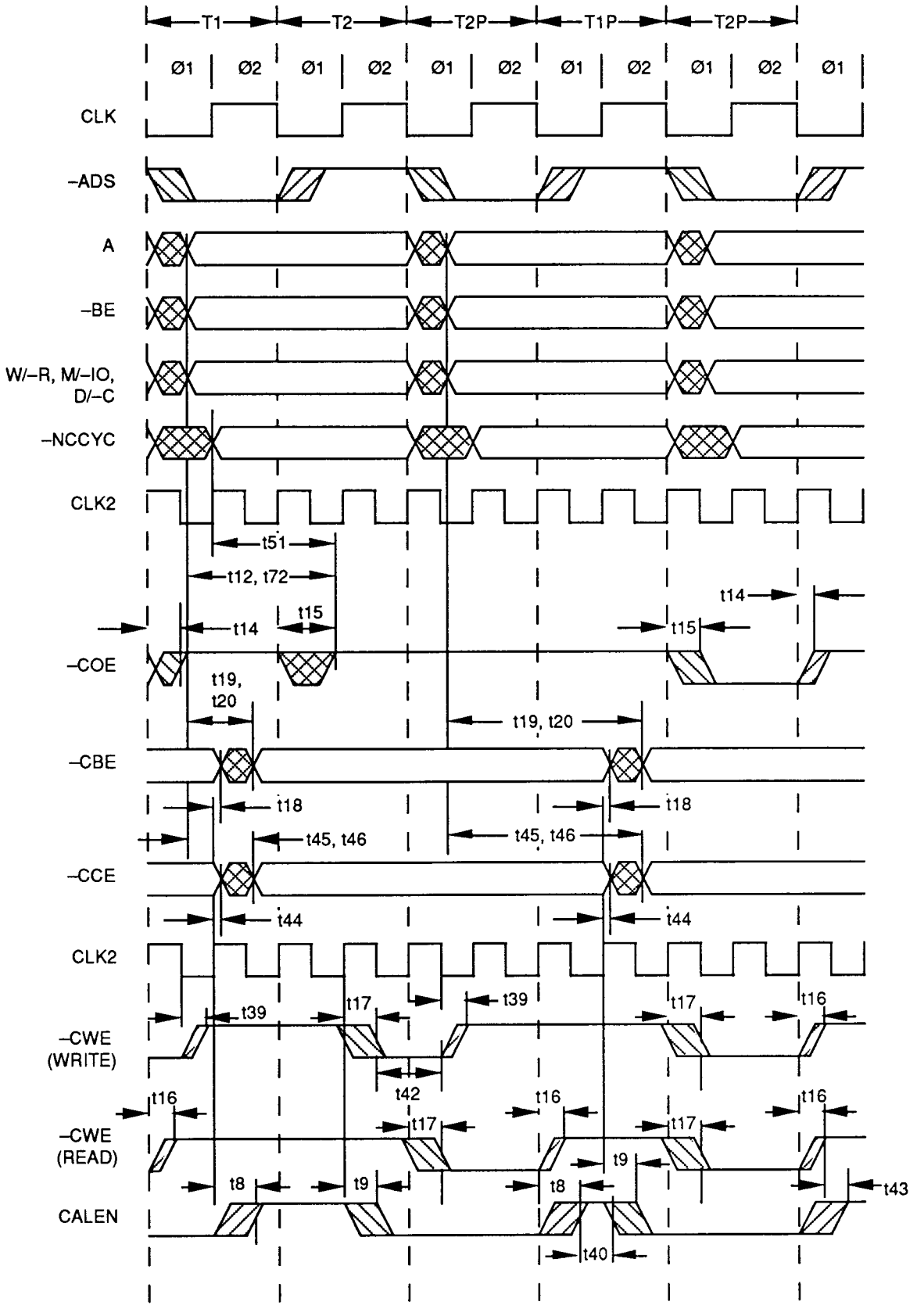


FIGURE 25. INPUT SU AND HO

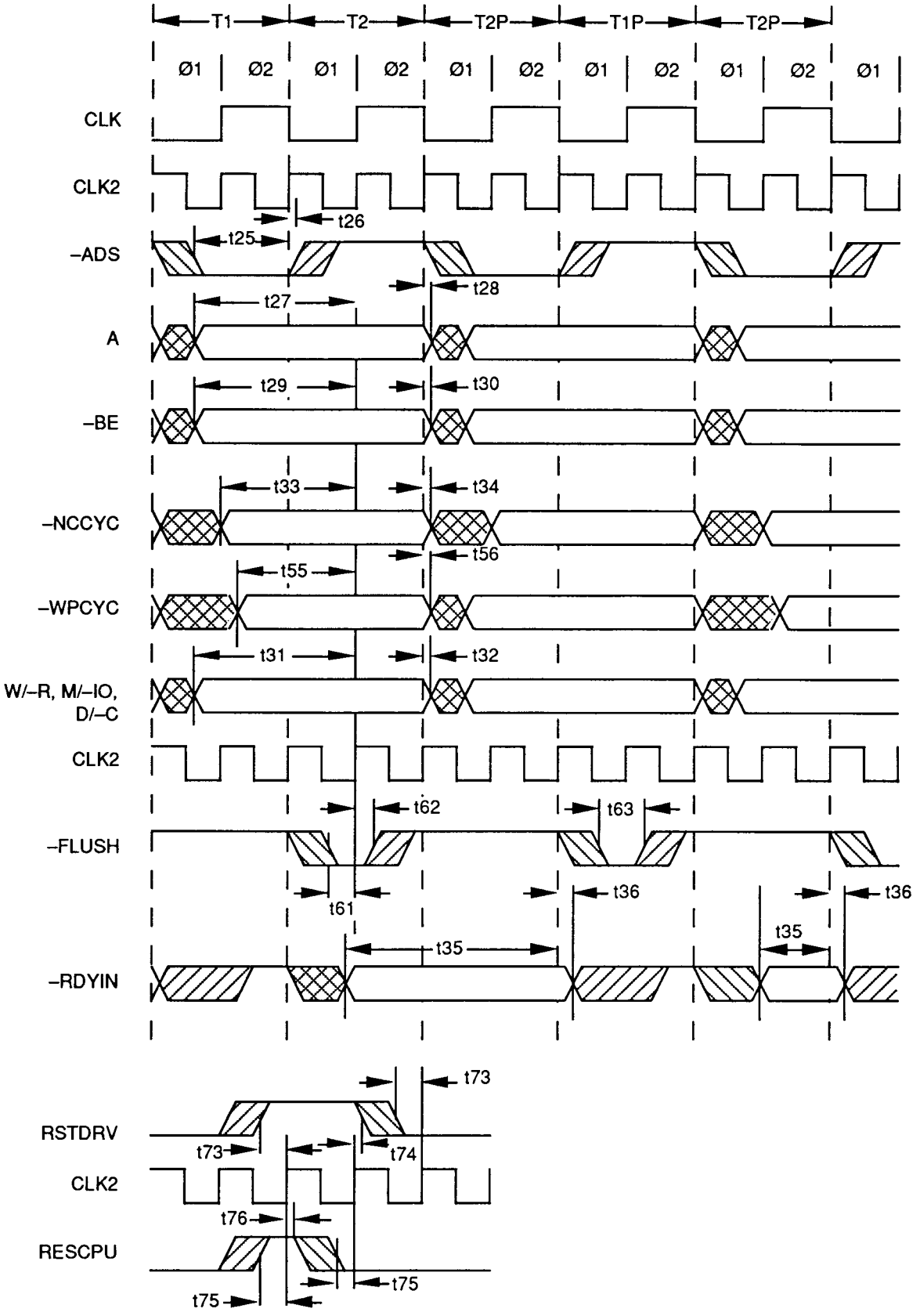


FIGURE 26. –IOR & –IOW TIMING

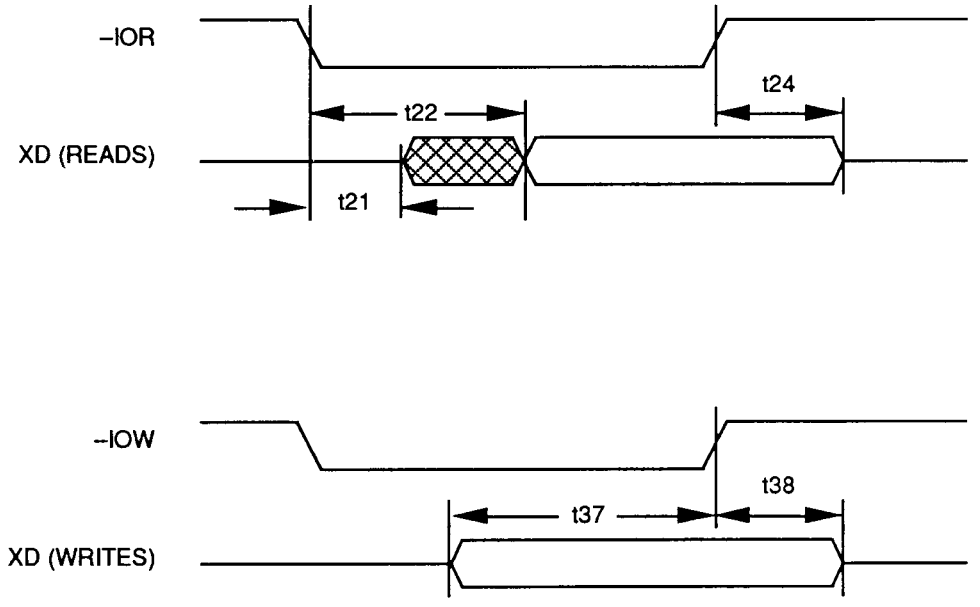
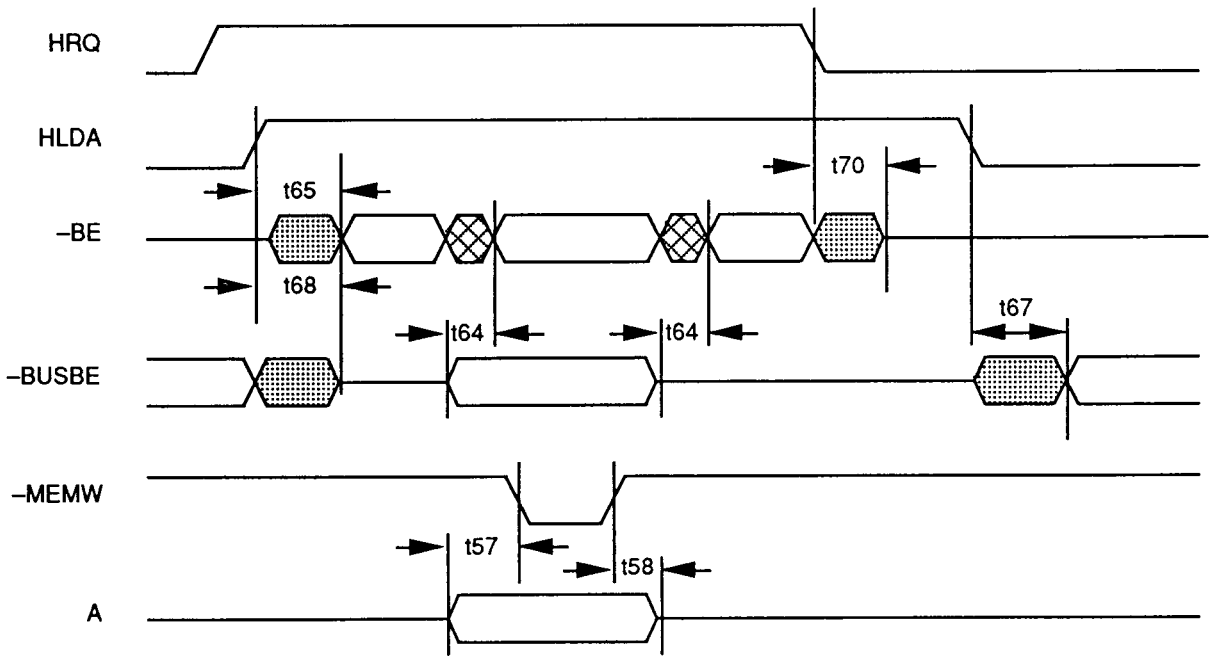


FIGURE 27. HLDA TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground –0.5 V to 7.0 V

Applied Output Voltage –0.5 V to VDD + 0.3 V

Applied Input Voltage –0.5 V to VDD + 0.3 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Conditions
VIL	Input Low Voltage		0.8	V	
VIH	Input High Voltage	2.0		V	
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL = 12 mA, –HIDRIVE = 1 IOL = 24 mA, –HIDRIVE = 0, Note 2
VOH1	Output High Voltage	VDD – 0.45		V	IOL –2 mA, Note 1
VOH2	Output High Voltage	2.4		V	IOL –6 mA, Note 2
ILI	Input Leakage Current	–10	10	µA	Note 3
IIL	Input Leakage Current	–500	10	µA	Notes 4
ILO	Output Leakage Current	–100	100	µA	
IDDSB	Static Supply Current		TBD	µA	
IDDOP	Dynamic Supply Current		1.5	mA/MHz	
CI	Input or I/O Capacitance		10	pF	
CO	Output Capacitance		10	pF	

Notes: 1. All outputs except XD7-XD0.

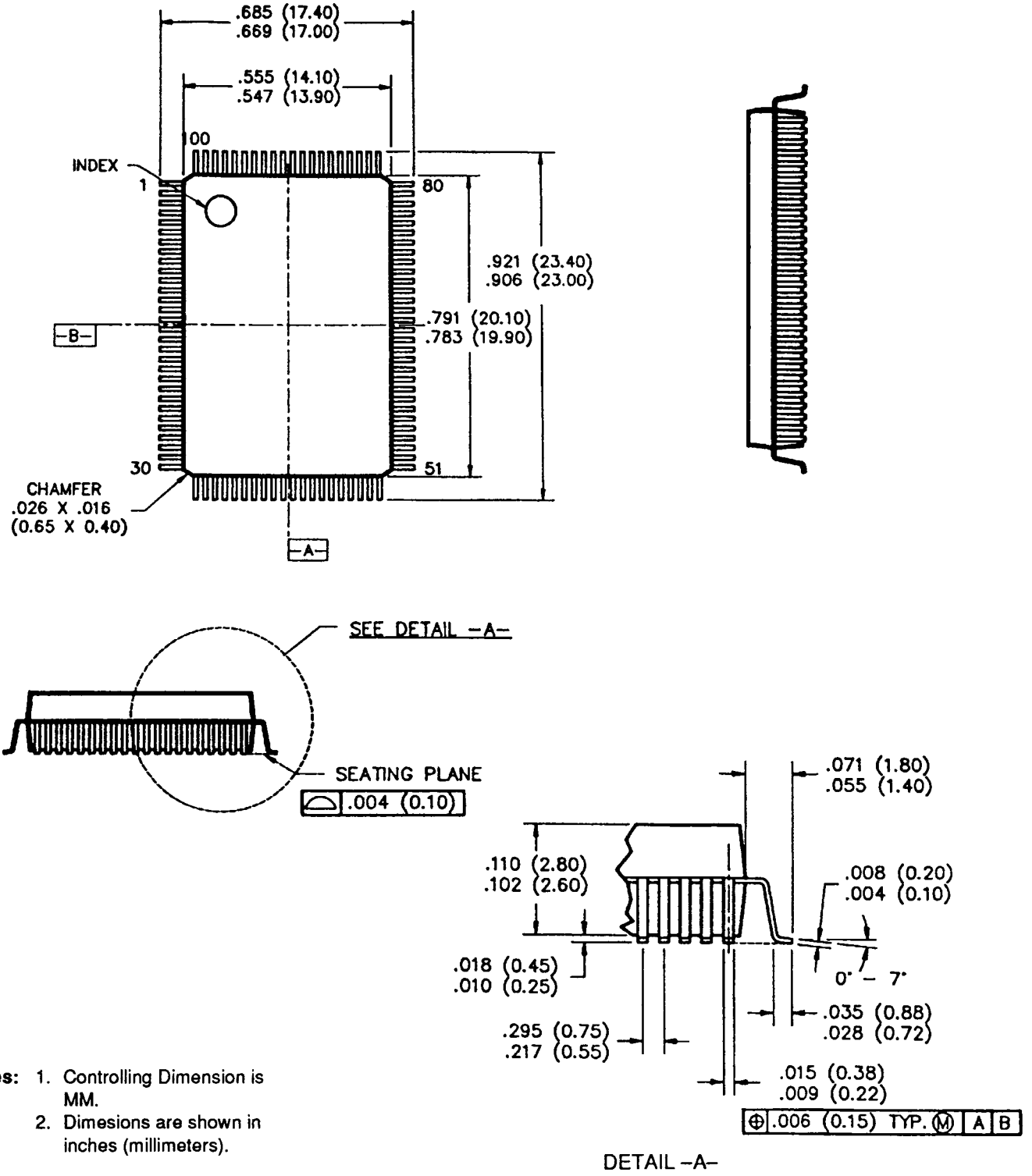
2. Pins: XD7-XD0

3. All inputs except those listed in Note 4.

4. Pins –NCCYC, –WPCYC, –FLUSH, –TRI, –HIDRIVE, and –MASTER.

PACKAGE OUTLINE

100-PIN METRIC (PLASTIC) QUAD FLAT PACK



Notes: 1. Controlling Dimension is MM.
2. Dimesions are shown in inches (millimeters).

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