PC/AT-COMPATIBLE ADDRESS BUFFER

FEATURES

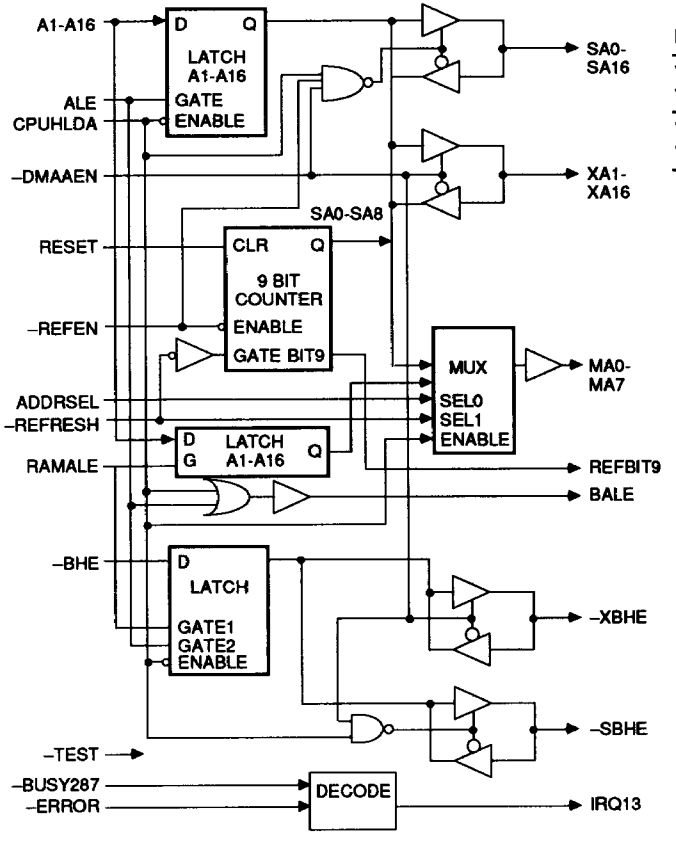
- Fully compatible with IBM PC/AT-type designs
- Completely performs address buffer function in IBM PC/AT-compatible systems
- Replaces several buffers, latches and other logic devices
- Supports up to 20 MHz system clock
- Device is available as "cores" for user-specific designs
- Designed in CMOS for low power consumption

DESCRIPTION

The VL82C203 PC/AT-Compatible Address Buffer provides the system with a 16-bit address bus input from the CPU to 41 buffered drivers. The buffered drivers consist of 17 bidirectional system bus drivers, each capable of sinking 24 mA (60 'LS loads) of current and driving 200 pF of capacitance on the backplane; 16 bidirectional peripheral bus drivers, each capable of sinking 8 mA (20 'LS loads) of current; and eight memory bus drivers, also capable of sinking 8 mA of current. On-chip refresh circuitry supports both 256K-bit and 1M-bit DRAMs. The VL82C203 provides addressing for the I/O slots as well as the system.

The device is manufactured with VLSI's advanced high-performance CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The VL82C203 is part of the PC/AT-compatible chip sets available from VLSI. Please refer to the Selector Guide in the front of this manual.

BLOCK DIAGRAM



ORDER INFORMATION

Part Number	System Clock Freq.	Package
VL82C203-16QC VL82C203-16QI	16 MHz	Plastic Leaded Chip Carrier (PLCC)
VL82C203-20QC VL82C203-20QI	20 MHz	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range:
QC = 0°C to +70°C
QI = –40°C to +85°C.

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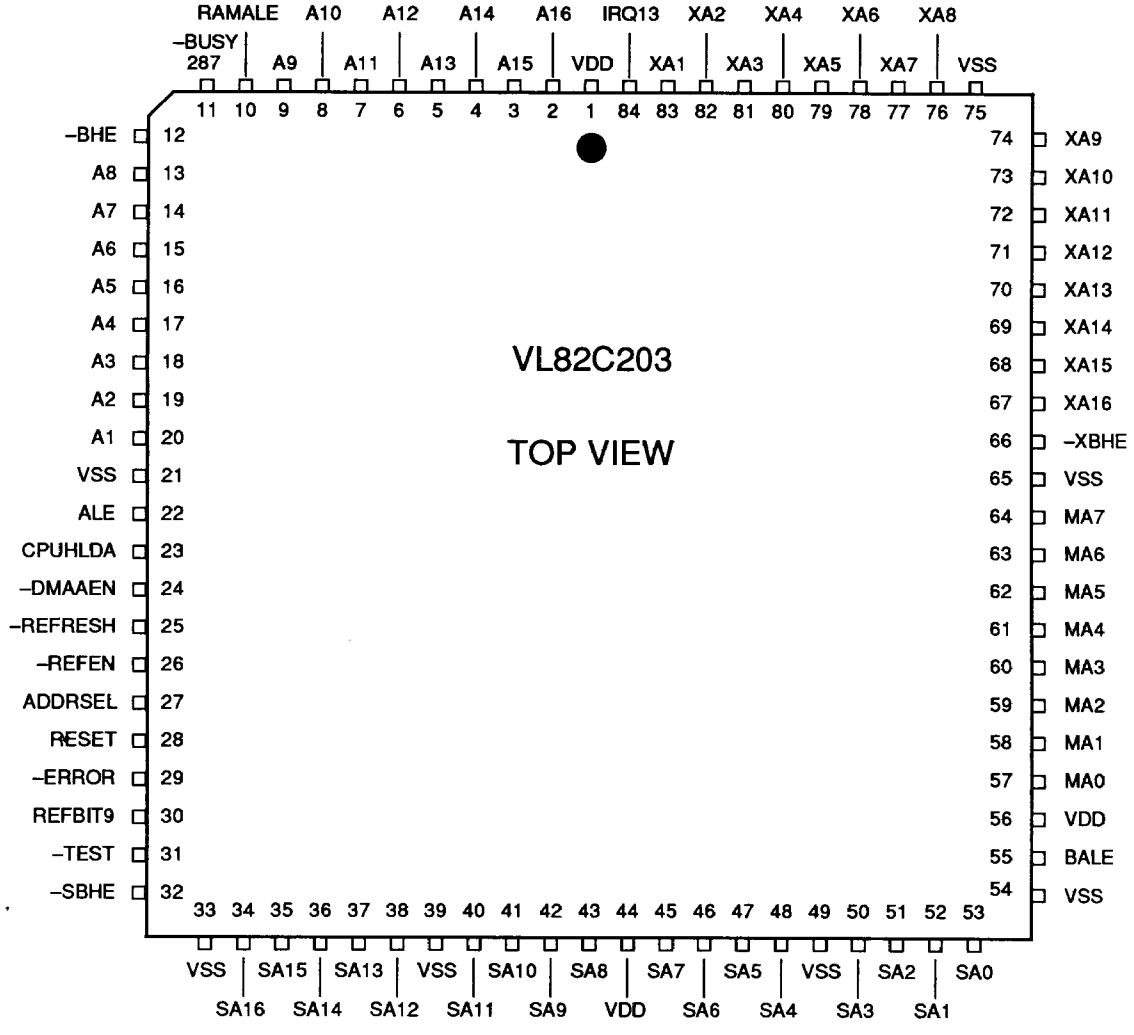
PIN DIAGRAM


RAMALE
A10
A12
A14
A16
IRQ13
XA2
XA4
XA6
XA8
-BUSY
287
A9
A11
A13
A15
VDD
XA1
XA3
XA5
XA7
VSS
11 10 9 8 7 6 5 4 3 2 1 84 83 82 81 80 79 78 77 76 75
-BHE 12
A8 13
A7 14
A6 15
A5 16
A4 17
A3 18
A2 19
A1 20
VSS 21
ALE 22
CPUHLDA 23
-DMAAEN 24
-REFRESH 25
-REFEN 26
ADDRSEL 27
RESET 28
-ERROR 29
REFBIT9 30
-TEST 31
-SBHE 32
74 XA9
73 XA10
72 XA11
71 XA12
70 XA13
69 XA14
68 XA15
67 XA16
66 -XBHE
65 VSS
64 MA7
63 MA6
62 MA5
61 MA4
60 MA3
59 MA2
58 MA1
57 MA0
56 VDD
55 BALE
54 VSS
VL82C203
TOP VIEW
33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
VSS
SA15
SA13
VSS
SA10
SA8
SA7
SA5
VSS
SA2
SA0
SA16
SA14
SA12
SA11
SA9
VDD
SA6
SA4
SA3
SA1

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
A1-A16	20-13, 9-2	I	CPU Address Bus Bits 1-16 - The lower 16 bits of the CPU address bits. These are multiplexed to the system address bus for the slots SA1-SA16, the memory address bus MA0-MA7, and the peripheral address bus XA1-XA16.
RAMALE	10	I	RAM Address Latch Enable - RAMALE is used to latch RAM address buffers. It is forced high at the end of any bus cycle. This allows the address for the next bus cycle to be passed to the system memory sooner than the ALE signal. RAMALE will go back low at the end of the status cycle for any bus cycle to latch the memory address until the end of the bus cycle. The memory address latches are open when RAMALE is in the high state.
–BUSY287	11	I	Busy 287 - This active low input is asserted by the 80287 to indicate that it is currenty executing a command.
–BHE	12	I	Bus High Enable - This is the active low input signal from the 80286 microprocessor which is used to indicate a transfer of data on the upper byte on the data bus, D8-D15.
ALE	22	I	Address Latch Enable - This positive edge input controls the address latches which hold the address during a bus cycle. ALE is not issued for a halt bus cycle. All latches are open when ALE is in the high state.
CPUHLDA	23	I	CPU Hold Acknowledge - This active high input indicates ownership of the local CPU bus. When high, this signal indicates that the CPU has three-stated its bus drivers in response to a hold request. When low, it indicates that the CPU bus drivers are active.
–DMAAEN	24	I	DMA Address Enable - This is an active low input which is active whenever an I/O device is making a DMA access to the system memory.
–REFRESH	25	I	Refresh - An active low input which is used to initiate a refresh cycle for the dynamic RAMs. It is used to clock a refresh counter which provides addresses during the refresh cycle.
–REFEN	26	I	Refresh Enable - An active low input that will be asserted when a refresh cycle is needed for the DRAMs.
ADDRSEL	27	I	Address Select - This is a multiplex select for the memory address bus drivers. When ADDRSEL is low, the lower order address bits are selected. When high, the high order address bits are selected.
RESET	28	I	Reset - This active high input signal is the system reset generated from a POWERGOOD. It is synchronized to PROCCLK and used to reset the refresh counter.
–ERROR	29	I	Error - This is an active low input which indicates an error has occurred within the 80287 coprocessor.
REFBIT9	30	I	Refresh Bit 9 - This is the MSB of the refresh counter. When used with the Memory Controller chip a refresh address will be generated for 1M byte DRAMs.
–TEST	31	I	Test - This is an active low input which is used to three-state all outputs of the VL82C203 device. This is for system level test where it is necessary to overdrive the outputs of the VL82C203. When –TEST is low, all outputs and bidirectional pins of the VL82C203 will be three-stated. This pin should be pulled up via a 10K Ω pull-up resistor in a standard system configuration.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
–SBHE	32	I/O	System Bus High Enable - This is the system I/O signal used to indicate transfer of local data on the upper byte on the local data bus, D8-D15. –SBHE is active low and will be in input mode during bus hold acknowledge.
SA0-SA16	53-50, 48-45 43-40, 38-34	O	System Address Bus Bits 0-16 - SA0 will be active only during a refresh cycle otherwise it will be three-stated (input mode).
BALE	55	O	Buffered Address Latch Enable - An active high output that is used to latch valid addresses and memory decodes from the 80286. System addresses SA0–SA16 are latched on the falling edge of BALE. During a DMA cycle BALE is forced active high.
MA0-MA7	57-64	O	DRAM Memory Address Bus Bits 0-7 - This 8-bit output is multiplexed using ADDRSEL to give a full 16-bit address.
XA1-XA16	83-76, 74-67	I/O	Peripheral Address Bus Bits 1-16 - These I/Os are used to control the coprocessor, keyboard, ROM memory and the DMA controllers.
–XBHE	66	I/O	Transfer Byte High Enable - This is an active low I/O used to allow the upper data byte to be transferred through the bus transceivers.
IRQ13	84	O	This is an active high output which indicates an error has occurred within the 80287 coprocessor.
VDD	1, 44, 56		System Supply: 5 V
VSS	21, 33, 39 49, 54, 65, 75		System Ground

FUNCTIONAL DESCRIPTION

The VL82C203 is part of a five chip set which together perform all of the on-board logic required to construct an IBM PC/AT-compatible system. The PC/AT-Compatible Address Buffer replaces several bus transceivers and address data latches located within the PC/AT-type system. The DRAM refresh circuitry is also located on this device.

The primary function of the Address Buffer is to multiplex the 80286 microprocessor address lines (A1-A16) to the system address bus (SA0-SA16), the peripheral address bus (XA1-XA16), and the memory address bus (MA0-MA7). This is accomplished through positive edge triggered latches and a group of data multiplexers. The two groups of latches can be seen in the block diagram of the device. One set of latches have their output enabled with CPUHLDA and are gated with ALE. This set of latches drive the SA and XA bus outputs. Another parallel set of latches are multiplexed into the MA lines and are gated with RAMALE. RAMALE is an early ALE signal. This allows more setup time for the address to be multiplexed to the DRAMs. If the VL82C203 is not used in conjunction with the other PC/AT-devices, RAMALE and ALE should be wired together to provide maximum PC/AT-compatibility.

The device also provides for address flow between the SA, XA, and MA buses and the –XBHE and –SBHE signals. The –XBHE signal is gated with the RAMALE input while the –SBHE is gated with the ALE input. This control flow is arbitrated with the CPUHLDA, –DMAAEN, and –REFEN inputs and is shown in Table 1.

TABLE 1. INTERNAL BUS CONTROL DECODE

CPU HLDA	–DMA AEN	–REF EN	A	SA	XA	MA	–XBHE	–SBHE
0	X	X	I	O	O	O	O	O
1	0	1	I	O	I	O	I	O
1	1	0	I	O	O	O	O	I
1	1	1	I	I	O	O	O	I

I = Input Mode
O = Output Mode
X = Don't Care

Memory addresses are multiplexed from the SA and A bus sources and are controlled via the CPUHLDA, –REFRESH, and ADDRSEL inputs. The mapping and control is shown in Table 2.

A 9-bit refresh counter is provided on this device. This allows support for DRAMs of up to 1M bit in size. The refresh counter is clocked on the rising edge of the –REFRESH input. A latched register inside the counter latches in the current state of the counter on the falling edge of –REFEN and transfers this value to the internal bus which routes to the SA and MA bus outputs. The SA0 output is provided only for refresh purposes and is driven only during this time. During a refresh the SA and MA bus outputs are driven from the output of the refresh counter latch Q0-Q8. Refer to Table 3 for the mapping of the refresh counter to the bus lines.

Note that all SA bus lines are driven during a refresh cycle. ADDRSEL is not normally toggled during a refresh cycle but is shown in Table 3 for completeness of the logic implementation. The REFBIT9 signal is the Q8 output of the refresh counter. This is required only for the refresh of 1M bit DRAMs.

TABLE 2. MEMORY ADDRESS MAPPING

Mux Control Input			MA Bus	
CPUHLDA	–REFRESH	ADDRSEL	MA7	MA0-MA6
1	0	0	SA8	SA1-SA7
1	0	1	SA16	SA9-SA15
0	X	0	A8	A1-A7
0	X	1	A16	A9-A15

X = Don't Care

TABLE 3. REFRESH ADDRESS MAPPING

Mux Control Input			MA Bus		SA Bus	
CPU HLDA	–REF EN	ADDR SEL	MA7	MA0-MA6	SA9-SA15	SA0-SA8
1	0	0	Q0	Q1-Q7	0	Q0-Q8
1	0	1	0	0	0	Q0-Q8

The –TEST pin has been added to enhance system level testing of the VL82CPCAT-16/-20 chip sets. When this pin is active (0), all outputs and bidirectional pins are placed in three-state.

This allows a board level test system to overdrive outputs of the VL82C203 without damage to the device. When –TEST is active, the internal bus is driven to the state of the system address bus (SA0-SA16).

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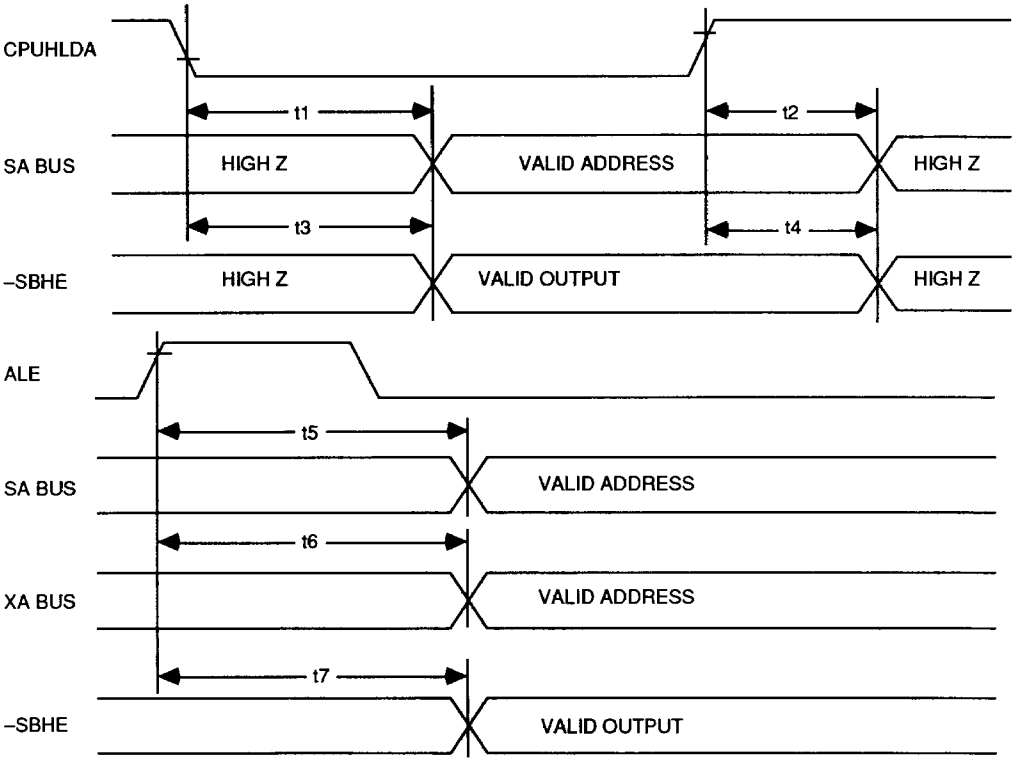
AC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ± 5%, VSS = 0 V

CPU MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t1	CPUHLDA to SA Bus from High Z to Valid Add Out		35		35	ns	
t2	CPUHLDA to SA Bus High Z State		35		35	ns	
t3	CPUHLDA to –SBHE from High Z to Valid Out		35		35	ns	
t4	CPUHLDA to –SBHE High Z State		35		35	ns	
t5	ALE to SA Bus Valid Address		40		40	ns	CL = 200 pF
t6	ALE to XA Bus Valid Address		40		40	ns	CL = 100 pF
t7	ALE to –SBHE Bus Valid Address		40		40	ns	CL = 200 pF

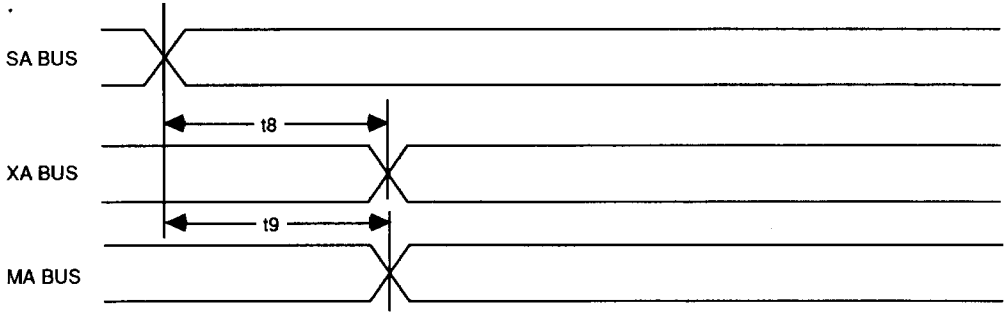
CPU MODE TIMING WAVEFORMS



SYSTEM BUS MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t8	SA Bus In to XA Bus Out		40		40	ns	CL = 100 pF
t9	SA Bus In to MA Bus Out		40		40	ns	CL = 300 pF

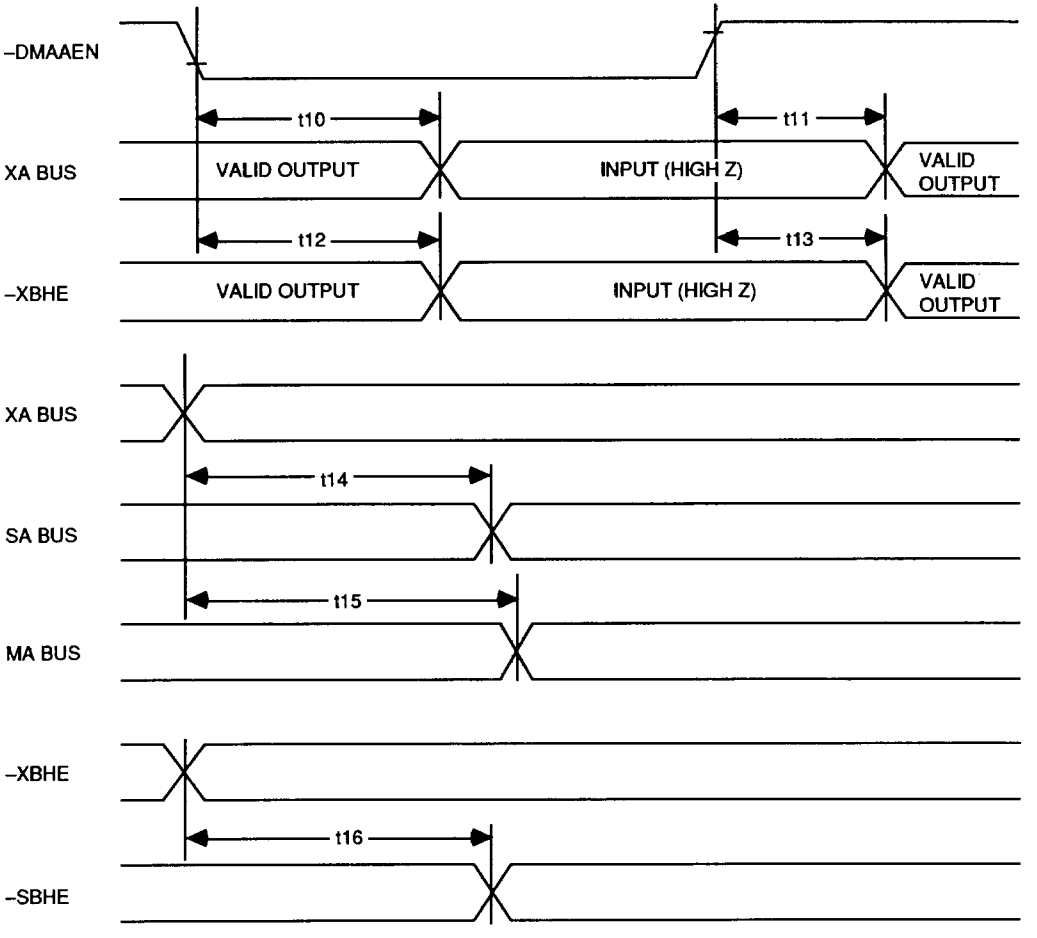
SYSTEM BUS MODE TIMING WAVEFORM



DMA MODE TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t10	–DMAAEN to XA Bus High Z State		35		35	ns	
t11	–DMAAEN to XA Bus from High Z to Valid Add Out		35		35	ns	
t12	–DMAAEN to –XBHE High Z State		35		35	ns	
t13	–DMAAEN to –XBHE from High Z to Valid Output		35		35	ns	
t14	XA Bus to SA Bus Out		40		40	ns	CL = 200 pF
t15	XA Bus In to MA Bus Out		40		40	ns	CL = 300 pF
t16	–XBHE In to –SBHE Out		40		40	ns	CL = 200 pF

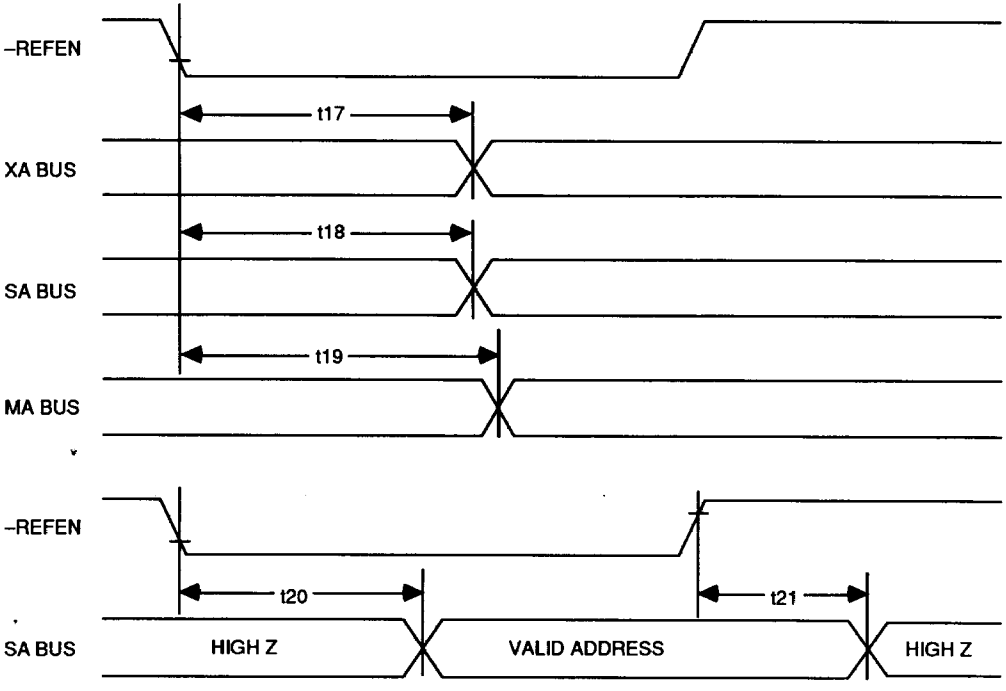
DMA MODE TIMING WAVEFORMS



REFRESH TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t17	–REFEN to XA Bus Valid Add Out		35		35	ns	CL = 100 pF
t18	–REFEN to SA Bus Valid Add Out		35		35	ns	CL = 200 pF
t19	–REFEN to MA Bus Valid Add Out		35		35	ns	CL = 300 pF
t20	–REFEN to SA Bus from High Z to Valid Add Out		35		35	ns	
t21	–REFEN to SA Bus High Z Out		35		35	ns	

REFRESH TIMING WAVEFORMS

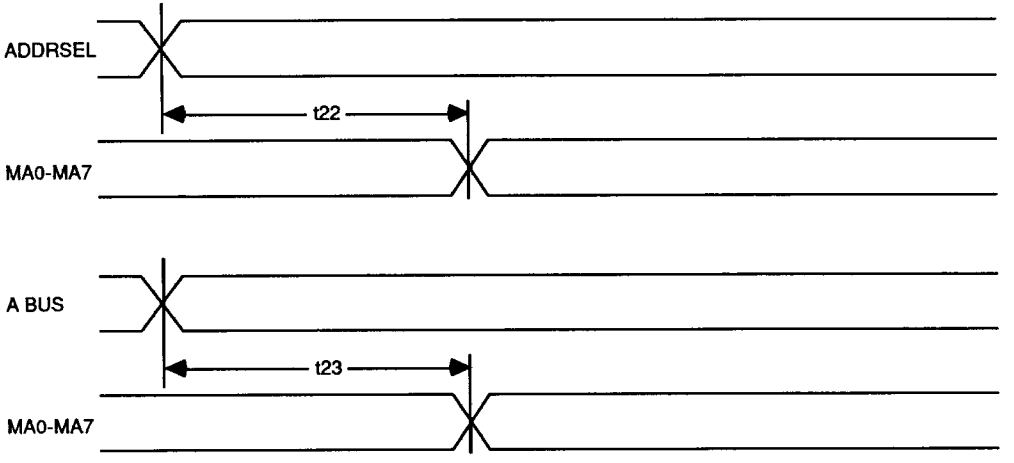


ADDRESS TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t22	ADDRSEL to MA Bus Out	4	19	4	19	ns	CL = 300 pF
t23	A Bus to MA Bus Out		25		25	ns	CL = 300 pF

Note: t22 delay may be derated by a factor of .04 ns/pF for heavier loads.

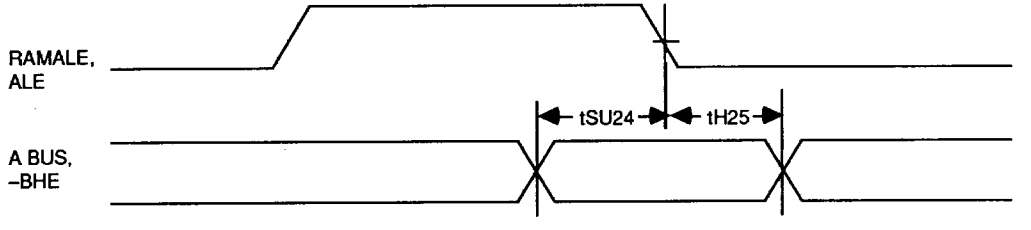
ADDRESS TIMING WAVEFORM



SETUP & HOLD TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
tSU24	A Bus to RAMALE and –BHE to ALE Setup Timing	10		10		ns	
tH25	A Bus to RAMALE and –BHE to ALE Hold Timing	10		10		ns	

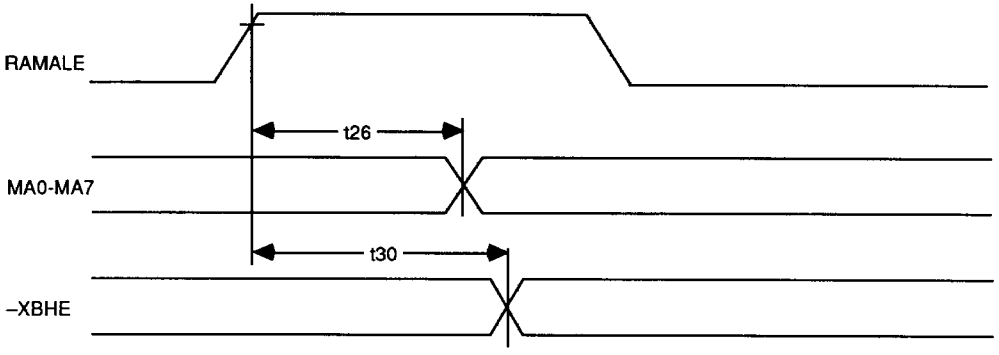
SETUP & HOLD TIMING WAVEFORM



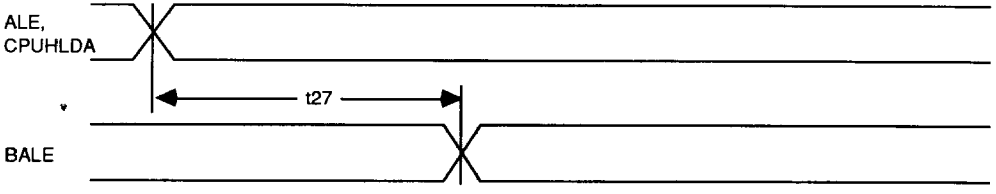
RAMALE, BALE & IRQ13 TIMING

Symbol	Parameter	16 MHz		20 MHz		Unit	Condition
		Min	Max	Min	Max		
t26	RAMALE to MA Bus Out		20		18	ns	CL = 300 pF
t27	ALE, CPUHLDA to BALE Out		25		25	ns	CL = 200 pF
t28	–ERROR to IRQ13 Out		30		30	ns	CL = 50 pF
t29	–BUSY287 to IRQ13 Out		30		30	ns	CL = 50 pF
t30	RAMALE to –XBHE		25		25	ns	CL = 100 pF

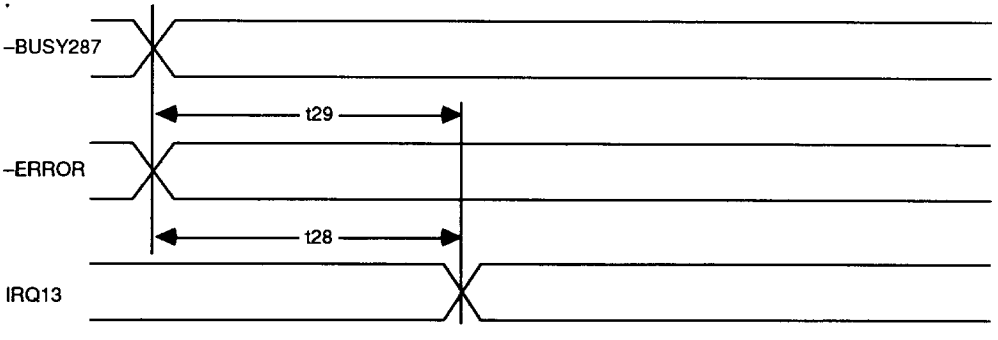
RAMALE TIMING WAVEFORM



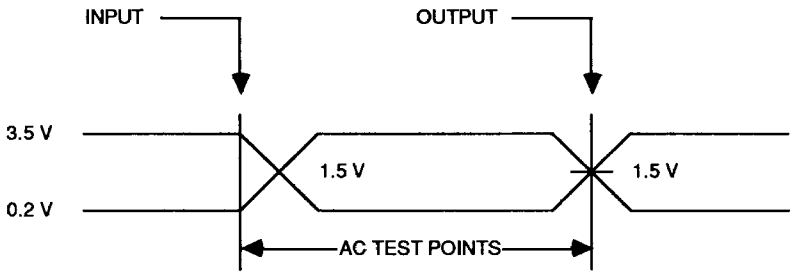
BALE TIMING WAVEFORM



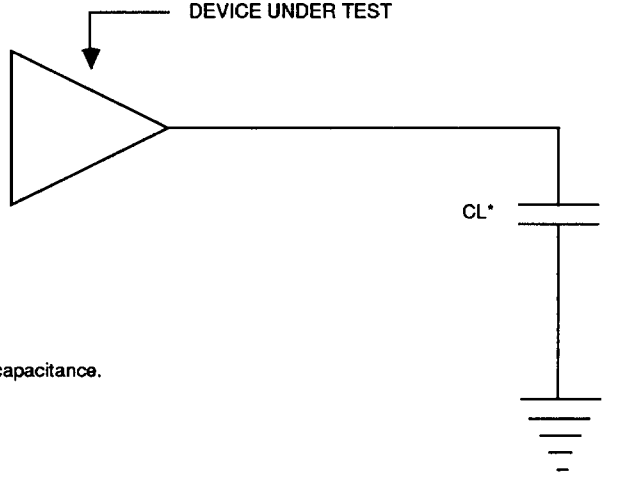
IRQ13 TIMING WAVEFORM



AC TESTING - INPUT, OUTPUT WAVEFORM



AC TESTING - LOAD CIRCUIT



*Includes scope and jig capacitance.

AC TESTING - LOAD VALUES

Test Pin	CL (pF)
32, 34-38, 40-43, 45-48, 50-53, 55	200
57-64	300
66-74, 76-83	100
84, 30	50

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	QC = 0°C to +70°C QI = –40°C to +85°C
Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5 V to +7.0 V
Applied Input Voltage	–0.5 V to +7.0 V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

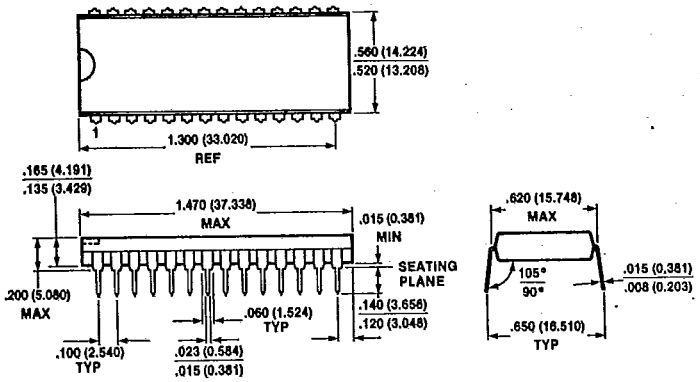
DC CHARACTERISTICS: TA = QC: 0°C to +70°C, QI: –40°C to +85°C, VDD = 5 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
VOH	Output High Voltage	2.4		V	IOH = –3.3 mA
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Notes 1 & 3
VOL2	Output Low Voltage		0.45	V	IOL = 24 mA, Notes 2 & 3
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIL	Input Low Voltage	–0.5	0.8	V	
VIHC	Input High Voltage	3.8	VDD + 0.5	V	ALE, RAMALE
VILC	Input Low Voltage	–0.5	0.6	V	ALE, RAMALE
CO	Output Capacitance		8	pF	
CI	Input Capacitance		8	pF	
CIO	Input/Output Capacitance		16	pF	
ILOL	Three-state Leakage Current	–100	100	µA	
ILI	Input Leakage Current	–10	10	µA	
ICC	Power Supply Current		20	mA	@ 1 MHz Test Rate

Notes: 1. Pins 57-64, 66-74, and 76-83.
2. Pins 32, 34-38, 40-43, 45-48, and 50-53, 55.
3. Output low current on all other outputs not mentioned in Note 1 or 2 have IOL (max) = 2 mA.

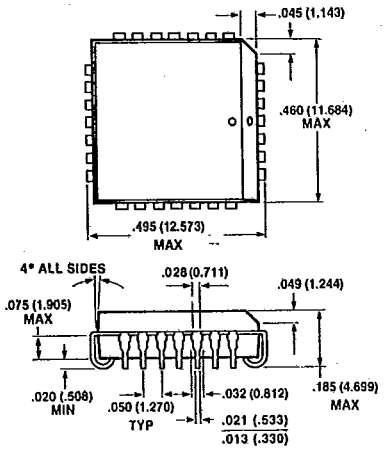
PACKAGE OUTLINES:

28-PIN PLASTIC DUAL IN-LINE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
4. TOLERANCE TO BE ± .005 (0.127) UNLESS OTHERWISE NOTED.
5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

28-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR Sn Pb SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

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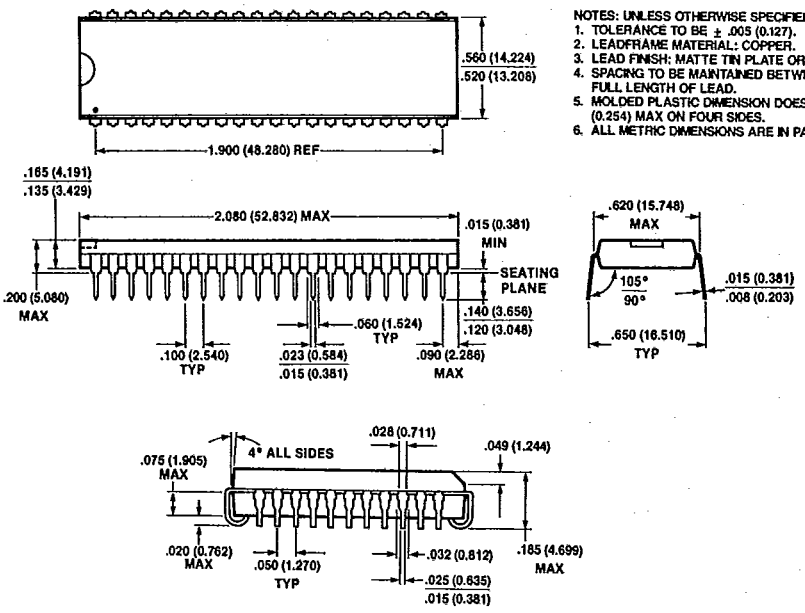
PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

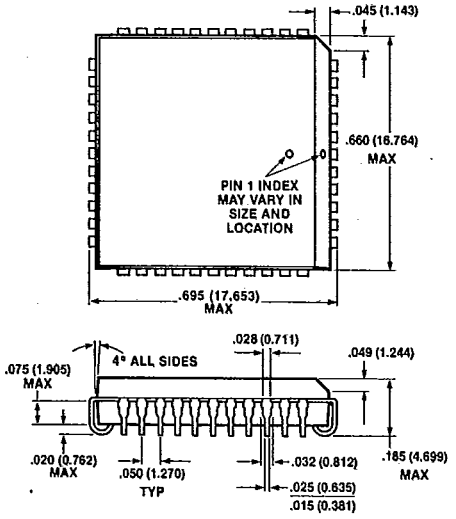
T-90-20

40- PIN PLASTIC DUAL IN-LINE



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

44-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE ± .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

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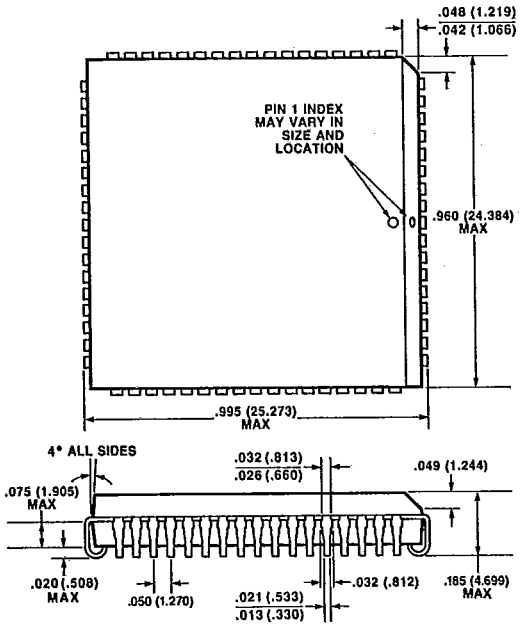
PACKAGE OUTLINES (Cont.):

T-90-20

68-PIN PLASTIC LEADED CHIP CARRIER



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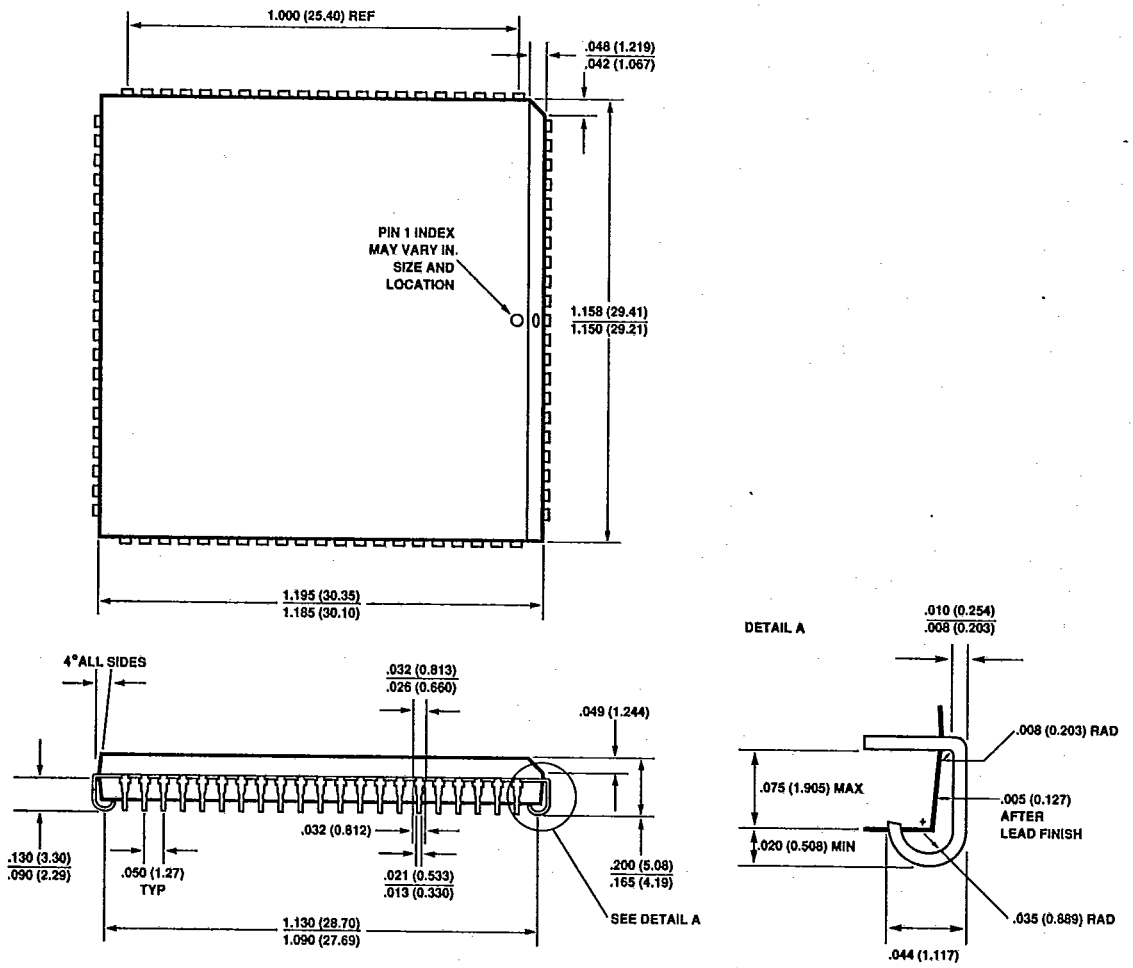
VLSI TECHNOLOGY, INC.

PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

T-90-20

84-PIN PLASTIC LEADED CHIP CARRIER



NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE +/- .005 (0.127).
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
6. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.

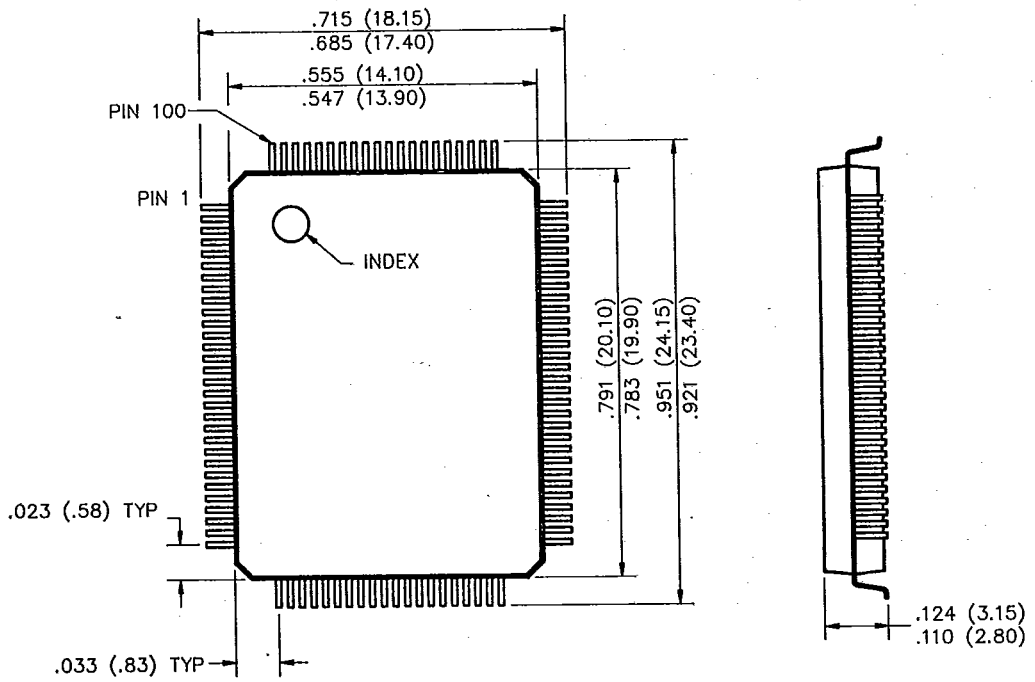
VLSI TECHNOLOGY, INC.

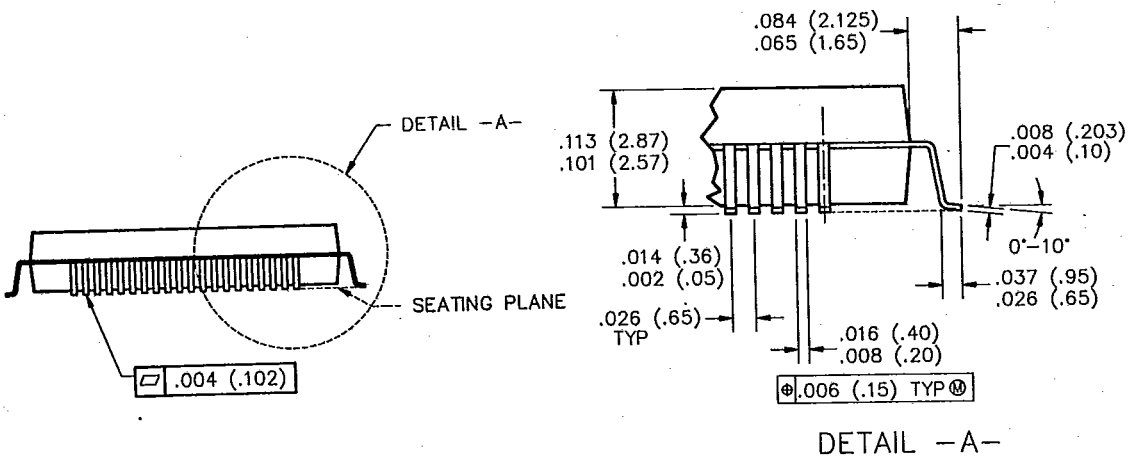
PACKAGE OUTLINES

PACKAGE OUTLINES (Cont.):

T-90-20

100-PIN PLASTIC FLATPACK





DETAIL -A-

NOTES:
1. CONTROLLING DIMENSION IS MM.

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