- High-Speed 1-μm CMOS Technology Supports System Speeds up to 33 MHz
- Fully AT-Compatible 386 Three-Chip SX, Four-Chip DX Solutions
- Only Four Additional Logic Chips Needed
- Major Features Programmable Through Software
- TACT83442 Memory Control Unit (MCU)
  - Cascadable up to Eight Devices
  - Address Range of up to 32M Byte Per Device, 256M Byte Fully Cascaded
  - Supports 256K-, 1M-, and 4M-Bit DRAMs in Normal, Page, Word-Interleave, and Page Block-Interleave Modes
  - Programmable DRAM Timing Parameters
  - Supports up to Two Memory Banks for 32-Bit Systems and Four Banks for 16-Bit Systems
  - Can Directly Drive up to 36 DRAM Devices
  - Shadow RAM Available Between 0C 0000h and 0F FFFFh
  - Contains Global Page Mapping RAM Allowing Remap of
    - 64K-Byte Memory Blocks Above 1M Byte
    - 16K-Byte Memory Blocks Below 1M Byte
- TACT83443 AT Bus Interface Unit (ATU)
  - Internal Clock Switching Between Two Independent Frequencies Controlled by Software
  - Asynchronous AT Bus Interface With Write Buffer Option
  - Full AT Direct-Drive Capability
  - Extended Direct Memory Access Mode for 32-Bit Operation
  - Fast CPU Reset and A20GATE Modification
  - Numeric Processor Interface for 387SX, 387DX, and Weitek 3167
  - Integrates All Essential AT Peripherals
  - Real Time Clock With 128-Byte CMOS RAM
- TACT83441 Data Path Unit (DPU)
  - 8- and 16-Bit Data Bus Sizing
  - Data Path Cascadable to 32 Bits
  - Write Buffer Capability for AT Bus Access
  - Supports Posted Write Operations From Cache Controller
  - Parity Generation and Checking Logic

description

The Texas Instruments TACT83000 AT Chip Set is designed for cached and noncached 386™-based PC-AT™ compatible systems running at speeds up to 33 MHz. Manufactured with high-speed 1-μm CMOS EPIC™ technology, the chip set is functionally partitioned into three devices: the TACT83443 AT Bus Interface Unit (ATU), the TACT83442 Memory Control Unit (MCU), and the TACT83441 Data Path Unit (DPU). The ATU is packaged in a 208-lead plastic quad flatpack (QFP), while the MCU and DPU are packaged in 100-lead plastic QFPs.

These three chips, along with four other logic chips, comprise all the logic necessary for a fully compatible 16-bit 386SX-based system. Since one DPU provides a 16-bit data path, a 32-bit 386DX-based system requires an additional DPU.

With software-controlled configuration registers on board the ATU and MCU, the chip set supports a wide variety of PC system configurations. For complete programming details, see the *TACT83000 AT Chip Set User's Guide*, literature number SRZU001.

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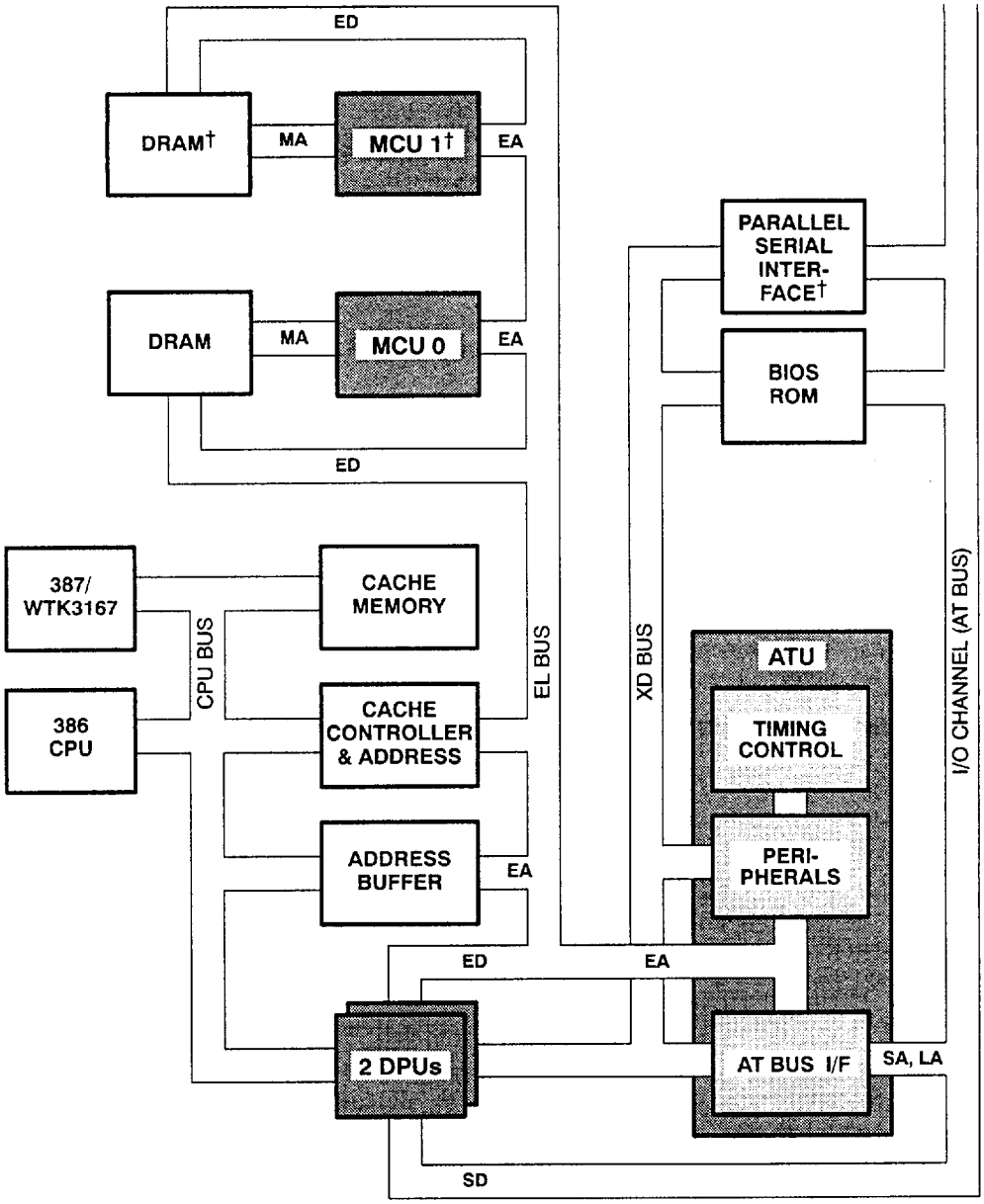
functional block diagram – 386DX cache-based system



† Optional

architecture

In a 386 cache-based system, the TACT83000 chip set architecture uses three tiers of buses. From the system core outward, these buses are the local or CPU bus, the extended local (EL) bus, and the AT bus. The architecture also provides an 8-bit peripheral bus, the XD bus, which operates with AT bus timing. The three-tiered bus structure used by the TACT83000 in a cache-based system can be seen in the functional block diagram.

The EL bus includes both data (ED) and address (EA) lines. CPU addresses sent out on the EA lines are mapped to physical memory addresses (MA) by the MCU. The AT bus includes system address (SA) and latched address (LA) lines, as well as system data (SD). Control lines are also included in the buses, though they are not listed separately in the block diagram. All data traffic between the buses is controlled by the DPU(s), which contain(s) logic for bus sizing and conversion, as well as for parity generation and checking.

The TACT83000 chip set supports the 82385 (or compatible) cache controller, providing control of external address buffers and data transceivers in the DPU between the CPU local bus and EL bus. In a cache-based system, the interface between the CPU local bus and the EL bus is controlled by the cache controller. In a noncached system, the EL bus essentially becomes the CPU bus.

The ATU, situated between the EL bus and the AT system bus, provides the interface, timing, and command control for both buses, as well as direct 24-mA drive capability for the I/O channel. The ATU also contains essential AT system board peripherals.

The MCU, located on the EL bus, controls system memory interface. The MCU is a programmable DRAM controller that has extensive memory mapping capability. It can function in several DRAM modes selectable through its configuration registers.

extended local (EL) bus

The EL bus is a buffered CPU bus with additional parity lines and control signals for EL bus accesses. These control signals, local access with parity ($\overline{\text{LAP}}$) and local access with no parity ($\overline{\text{LANP}}$), are required of all devices on the EL bus and gated to the ATU to indicate that the current cycle is an EL bus access.

In many systems, performance can be greatly improved by placing high-speed I/O peripheral devices on the EL bus instead of on the AT bus. These devices can then operate at CPU speed, rather than at the 8-MHz limit of the AT bus. Typical examples of such peripherals are SCSI disk controllers, LAN adapters, and display subsystems. A peripheral placed on the EL bus must generate $\overline{\text{LAP}}$/$\overline{\text{LANP}}$ when it is accessed in order to let the system controller know that the bus cycle belongs to that device on the EL bus. Otherwise, the cycle will be either passed on to the AT bus or terminated by a ready signal from the system controller.

The EL bus directly supports the data bus width of the attached processor. Bus sizing must be accomplished through the byte enable bits ($\overline{\text{BE3}}$ – $\overline{\text{BE0}}$) and the DPU(s).

In a minimum system without a cache controller, the EL bus is identical to the CPU bus with respect to address and control. For example, the CPU address line A10 will be directly connected to the MCU EA10 address line. Note, however, that the EL data bus (ED0-EDxx) is always the output data from the DPU; it is the CPU data bus buffered via the DPU and is, therefore, the same in either a cached or noncached system.

chip set configuration

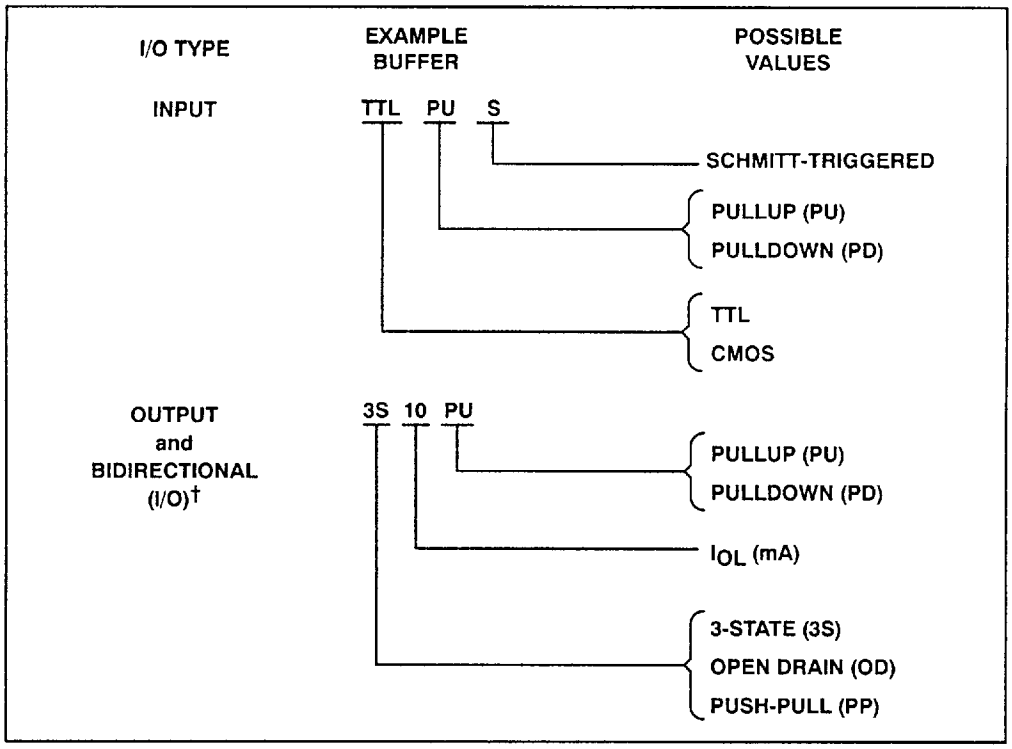
All programmable functions and page map entries for the ATU and MCU are accessed through an index/data register pair, minimizing the size of CPU I/O space necessary for configuration. The index register is a pointer to the actual configuration register/map entry location, and the data register is the port used to access the location pointed to by the index register. Once the desired index value is set by writing to the index register, reading from or writing to the data register will retrieve or update the value in the configuration register/page map entry addressed by the index register. A read or write of either register involves a single 16-bit data access.

By default, the data register is located at I/O address 0024h and the index register at 0026h. However, the register pair may be relocated after power-up to any unused I/O address between 0000h and FFFFh by resetting the configuration register I/O base address for the device (index = 0XFF). In a 32-bit system, the data register address must be at a double-word boundary.

For details regarding programming the configuration registers, see the *TACT83000 AT Chip Set User's Guide.*

internal I/O buffers

To ensure both AT compatibility and flexible system configurations, the TACT83000 chip set uses a variety of input and output buffers internally. These buffers are listed, along with the pin descriptions for each device, in the device Terminal Function Table. Figure 1 details the convention used to describe each type of I/O buffer.



† Bidirectional buffers operate at non-Schmitt-triggered TTL Input levels.

Figure 1. Buffer Naming Convention

TACT83443 AT Bus Interface Unit (ATU)

The ATU supports three types of functions: system bus interfacing, timing between buses, and standard AT peripherals. During a DMA cycle or a master cycle for an AT bus device, the ATU asserts control over the EL bus. At all other times, it is a slave to the EL bus master. This master is normally the cache controller in a cache-based system; however, there may be other EL bus masters as well.

interfacing system address and control buses

The ATU provides the interface, command translation, and timing control among the CPU/EL bus, AT bus, and system support peripherals. It manages two separate command/control buses – the AT bus and the EL bus. The signals from these two buses are inputs to two internal control blocks.

The AT control block monitors inbound CPU/EL signals and encodes those into corresponding AT bus signals. The EL control block monitors inbound AT bus signals and decodes those into CPU/EL signals. There is also a common support peripheral block, address management block, data control block, and configuration register space shared by the AT and EL control blocks.

timing between system buses

System oscillators are fed into the ATU, which in turn divides them to generate the appropriate system clocks for both the EL and AT buses. In addition to providing the clocks as outputs, the ATU uses the clocks for timing control and synchronization. The ATU also manages the generation of system reset and drives AT bus refresh timing.

The AT bus interface works either synchronously or asynchronously in both directions. All timing parameters, including control of the clock dividers, are defined by software.

AT peripherals

The ATU contains the following standard AT system board peripherals:

- Two 8237A-compatible direct memory access (DMA) controllers with SN74LS612-compatible page registers
- Two 8259-compatible interrupt controllers
- 8254-compatible timer/counter
- 146818-compatible real-time clock (RTC) with on-board oscillator
- Port B and nonmaskable interrupt (NMI) logic

All of these peripherals are fully AT-compatible functions. The DMA and NMI functions and the static RAM offer additional features. The DMA controller supports full 32-bit DMAs for EL bus devices, including support of an EL cascade or AT master mode. The NMI extensions provide for generation of NMI due to a $\overline{\text{READY}}$ timeout and improved NMI status reporting. The configuration static RAM provided with the RTC registers is 128 bytes in length and can be backed up by a battery.

Because the EL and AT buses share the standard peripheral block, these peripherals are available to both buses. For I/O addressing, the ATU peripherals and keyboard controller are placed on the XD bus, the only data bus that is routed into the ATU. Any additional devices (system ROMs) placed on the XD bus must drive $\overline{\text{XDSEL}}$.

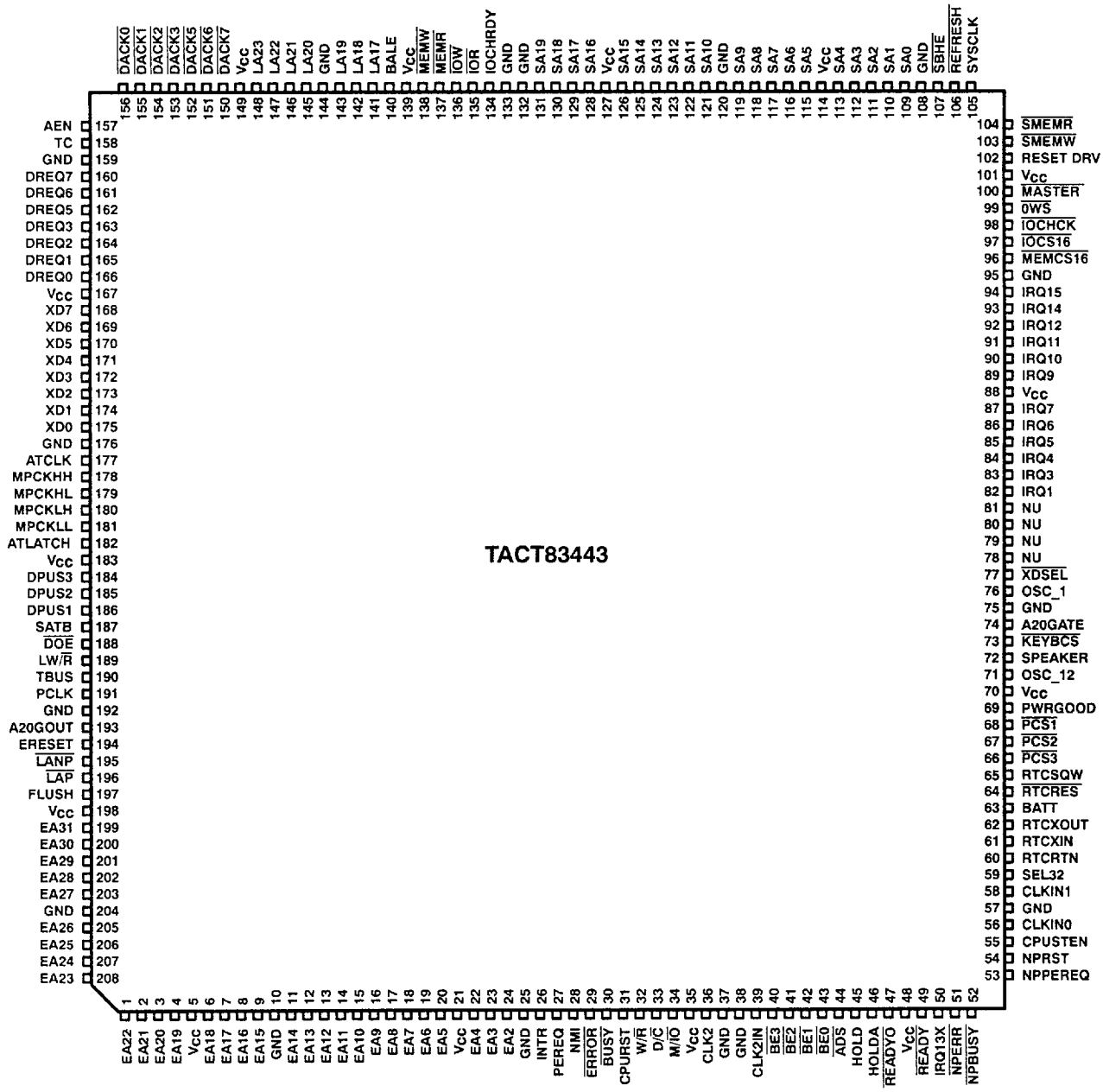
In addition to its extensive control and timing management for the major system buses, the ATU also provides interfaces for or supports several other system devices or functions. For example, an interface is available for a numeric coprocessor. This interface is monitored by the ATU and is used to provide the coprocessor's status to the CPU. A keyboard processor interface, AT bus refresh control logic, programmable chip select options, and AT write buffer control are also available.

ATU terminal assignments

T-52-33-05

The ATU is packaged in a 208-lead QFP. The ATU Terminal Functions Table gives a description of each terminal. See Figure 1 for details of the I/O buffer types.

Top View



NU–Nonusable, make no external connection. These are reserved for future use.

ATU Terminal Descriptions

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TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
CPU Signals				
$\overline{ADS}$	44	I/O	3S10PU	Address status control
$\overline{BUSY}$	30	O	PP6	Numeric coprocessor busy
CLK2	36	O	PP24	CPU Clock. This is the basic CPU clock. On power-up, the default source is CLKIN0.
CLK2IN	39	I	CMOS	CLK2 Input. Feedback of the CLK2 signal. This input is required to verify that the CPU clock and the internal AT unit clock have the same delay. It should be sourced after any clock distribution buffering.
CPURST	31	O	PP16	CPU Reset. Active during power-on reset, shutdown, and keyboard reset. The keyboard reset is generated internally to the ATU by intercepting the keyboard controller reset command.
D/$\overline{C}$	33	I/O	3S10PU	Data/Code control
$\overline{ERROR}$	29	O	PP6	Coprocessor error
HOLD	45	O	PP10	Hold request input to CPU
HOLDA	46	I	TTL-S	Hold acknowledge output from CPU
INTR	26	O	PP6	Interrupt request output to CPU
M/$\overline{IO}$	34	I/O	3S10PU	Memory/IO control
NMI	28	O	PP6	Nonmaskable Interrupt output to CPU
PEREQ	27	O	PP6	Numeric processor request
$\overline{READY}$	49	I	TTL-S	Ready input. Same signal as CPU or $\overline{EREADY}$.
$\overline{READYO}$	47	O	PP10	Ready out control. This ready output is ORed with the other EL bus READY signals.
W/$\overline{R}$	32	I/O	3S10PU	Write/Read control
EL Bus Signals†				
$\overline{BE0}$	43	I/O	3S10PU	Byte enable 0. Used with the 386 to enable data bits 0–7. The 386SX uses the signal $\overline{BLE}$ (Byte Low Enable).
$\overline{BE1}$	42	I/O	3S10PU	Byte enable 1. Used with the 386 to enable data bits 8–15. The 386SX uses the signal $\overline{BHE}$ (Byte High Enable).
$\overline{BE2}$	41	I/O	3S10PU	Byte enable 2. Used with the 386 to enable data bits 16–23. The 386SX uses the CPU address line A1.
$\overline{BE3}$	40	I/O	3S10PU	Byte enable 3. Used with the 386 to enable data bits 24–32. Tied high on 386SX systems.
EA2–EA4 EA5–EA14 EA15–EA18 EA19–EA22 EA23–EA26 EA27–EA31	24–22 20–11 9–6 4–1 208–205 203–199	I/O	3S10PU	EL bus address bits 2–31
ERESET	194	O	PP16	EL bus reset. Active only during power-on reset.
$\overline{LANP}$	195	I	TTL-S	Local access with no parity
$\overline{LAP}$	196	I	TTL-S	Local access with parity
LW/$\overline{R}$	189	O	PP10	Latched W/$\overline{R}$. This is the latched CPU or EL bus W/$\overline{R}$ signal.
PCLK	191	O	PP16	CPU phase clock. High during processor phase 2.

† In a minimum system configuration without cache and address buffers, some EL signals can be connected directly to the CPU. For example, in this case, EA10 is identical to A10 from the CPU.

ATU Terminal Descriptions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
SEL32	59	I	CMOS	Select 32-bit data bus width: L 386SX Operation Mode H 386DX Operation Mode
TBUS	190	O	PP10	CPU or EL bus state signal indicating T2/T2P. Active high.
Numeric Processor Interface Signals				
IRQ13X	50	I	TTLPD-S	Interrupt request 13. This signal is ORed internally with the output from the ATU numeric processor error logic to generate IRQ13 if a processor other than the 387 is used.
$\overline{\text{NPBUSY}}$	52	I	TTLPU-S	Numeric processor busy. This active low numeric processor output signal is used for generating a $\overline{\text{BUSY}}$ signal for the CPU.
$\overline{\text{NPERR}}$	51	I	TTLPU-S	Numeric processor error. If the numeric processor sets this signal low, an unmasked error condition has been detected. In this case, the $\overline{\text{NPBUSY}}$ signal is latched, and a numeric processor interrupt signal will be generated.
NPPEREQ	53	I	TTLPD-S	Numeric processor extension request input.
NPRST	54	O	PP16	Numeric processor reset. A high level on this signal generates a reset for the numeric processor. Either a write to I/O address 00F1h or a system reset will activate this signal.
DPU/Cache Interface Signals				
ATLATCH	182	O	PP6	AT bus buffer latch control
$\overline{\text{DOE}}$	188	O	PP6	Data output enable. This signal controls the CPU bus transceiver on the DPU if no cache controller is present.
DPUS1	186	O	PP6	DPU source select 1
DPUS2	185	O	PP6	DPU source select 2
DPUS3	184	O	PP6	DPU source select 3 (conversion signal)
FLUSH	197	O	PP6	Reset cache controller contents. This signal is set active by writing a 1 to the FPC bit of the ATU miscellaneous control register and cleared by writing 0.
MPCKHH	178	I	CMOS	Memory parity check high word high byte
MPCKHL	179	I	CMOS	Memory parity check high word low byte
MPCKLH	180	I	CMOS	Memory parity check low word high byte
MPCKLL	181	I	CMOS	Memory parity check low word low byte
SATB	187	O	PP6	Source/destination control of the AT bus Buffer
AT Bus Signals				
AEN	157	O	PP24	Address enable. This signal is used to disable other address driver devices from the AT bus. When this line is active, the DMA controller has control of the address data bus and read/write lines.
ATCLK	177	O	PP10	AT bus clock output. Output of the internal clock divider for the AT bus state machine. This clock is used for generating the independent AT bus timing. The power-on default source is CLKIN0/4.
BALE	140	O	PP24	Buffered address latch enable. During a HOLD cycle (HOLDA=1), this signal is driven high.

ATU Terminal Descriptions (continued)

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TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
$\overline{\text{DACK0}}$–$\overline{\text{DACK3}}$ $\overline{\text{DACK5}}$–$\overline{\text{DACK7}}$	156–153 152–150	O	PP6	DMA request acknowledge
DREQ0–DREQ3 DREQ5–DREQ7	166–163 162–160	I	TTL-S	DMA request. These signals are asynchronous channel requests that are prioritized. DREQ0 has the highest priority; DREQ7 has the lowest. DREQ0–DREQ3 will perform 8-bit DMA transfers and DREQ4–DREQ7 will perform 16-bit DMA transfers.
$\overline{\text{IOCHCK}}$	98	I	TTL-S	I/O channel check. This signal is used by devices on the I/O channel to indicate an uncorrectable error, such as a parity error. An NMI will be generated if NMI is enabled in Port B/NMI logic.
IOCHRDY	134	I/O	OD24	I/O channel ready. The ATU does not complete the current cycle as long as IOCHRDY is low. This signal is used by AT bus cards to extend the number of wait states beyond the set default values.
$\overline{\text{IOCS16}}$	97	I	TTL-S	I/O chip select 16. If $\overline{\text{IOCS16}}$ goes active low during an AT bus I/O cycle, the ATU disables the 16-to-8-bit conversion logic and sets the default wait states for 16-bit I/O transfer; otherwise, the ATU generates two 8-bit I/O cycles on the AT bus.
$\overline{\text{IOR}}$	135	I/O	3S24PU	I/O read. During AT master and DMA cascade modes, outputs are in 3-state.
$\overline{\text{IOW}}$	136	I/O	3S24PU	I/O write. During AT master and DMA cascade modes, outputs are in 3-state.
IRQ1 IRQ3–IRQ7 IRQ9–IRQ12 IRQ14–IRQ15	82 83–87 89–92 93–94	I	TTL-S	Interrupt request. Available for AT bus devices
LA17–LA19 LA20–LA23	141–143 145–148	I/O	3S24	Latchable address. These address bits are inputs when $\overline{\text{MASTER}}$ is low and HOLDA is high, indicating an external bus master cycle; they are outputs otherwise.
$\overline{\text{MASTER}}$	100	I	TTL-S	Master request input
$\overline{\text{MEMCS16}}$	96	I	TTL-S	Memory chip select 16. If $\overline{\text{MEMCS16}}$ goes active low during an AT bus memory cycle, the ATU disables the 16-to-8-bit conversion logic and activates the default wait state logic for a 16-bit transfer; otherwise, the ATU generates two 8-bit memory cycles on the AT bus.
$\overline{\text{MEMR}}$	137	I/O	3S24PU	Memory read bus. During AT master and DMA cascade modes, outputs are in 3-state.
$\overline{\text{MEMW}}$	138	I/O	3S24PU	Memory write bus. During AT master and DMA cascade modes, outputs are in 3-state.
$\overline{\text{REFRESH}}$	106	I/O	OD24	AT bus refresh
RESET DRV	102	O	PP24	Reset drive. This line is used to reset or initialize system logic on the AT bus. This signal is active during power-on and if the RPC bit in the ATU miscellaneous control register is set.
SA0–SA4 SA5–SA9 SA10–SA15 SA16	109–113 115–119 121–126 128	I/O	3S24	System address lines 0–16. Latched by BALE. During AT master and DMA cascade modes, outputs are in 3-state.
SA17–SA19	129–131	O	3S24	System address lines 17–19
$\overline{\text{SBHE}}$	107	I/O	3S24	System byte high enable

ATU Terminal Descriptions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
$\overline{\text{SMEMR}}$	104	O	3S24PU	System memory read. This signal is similar to the $\overline{\text{MEMR}}$ signal, but is only active in the first 1M byte address range.
$\overline{\text{SMEMW}}$	103	O	3S24PU	System memory write. This signal is similar to the $\overline{\text{MEMW}}$ signal, but is only active in the first 1M byte address range.
SYSCLK	105	O	PP24	AT bus system clock. This clock is half of the ATCLK frequency and is inactive until the first CPU access after reset.
TC	158	O	PP24	Terminal count. During DMA service, a high level indicates the completion of the requested number of transfers.
$\overline{\text{0WS}}$	99	I	TTL-S	Zero-wait state. AT bus cards can use this input to shorten the current bus cycle. After $\overline{\text{0WS}}$ goes low, the ATU will synchronously finish the cycle.
Peripheral Signals				
A20GATE	74	I	TTL-S	A20 gate input. Sourced by the keyboard and input to A20 gate out control logic.
A20GOUT	193	O	PP6	A20 gate output. Combination of keyboard controller, A20 gate, and gate output control bit of miscellaneous control register. A low level on this input will hold the A20 line low; otherwise, the A20 line is identical to the CPU A20 line.
BATT	63	I		Real-time clock power supply input. This terminal should be connected to battery circuit. This terminal is at V_{CC} level during powered operations and battery voltage is applied to it during a powered-down condition.
$\overline{\text{KEYBCS}}$	73	O	PP6	Keyboard controller chip select. Normally, the ATU generates chip select signals for I/O addresses 60h and 64h. However, when F0, F2, F4, F6, F8, FA, or FCh is written as data to I/O address 64h, both CPURST and $\overline{\text{KEYBCS}}$ are generated. When FEh is written to I/O address 64h, only CPURST is generated.
OSC_1	76	I	TTL	Oscillator clock input. This is the 14.31818-MHz clock, which is not synchronous to the AT-system clock (SYSCLK); an external oscillator is required.
OSC_12	71	O	PP6	Oscillator clock output. Provides 1.193-MHz frequency for a PC-AT-compatible design, which is used internally for the timers and by the MCU for refresh and $\overline{\text{RAS}}$ pulse width timing.
$\overline{\text{PCS1}}$	68	O	OD6	Programmable chip select 1. Programmable through index address = 0809.
$\overline{\text{PCS2}}$	67	O	OD6	Programmable chip select 2. Programmable through index address = 080A.
$\overline{\text{PCS3}}$	66	O	OD6	Programmable chip select 3. Programmable through index address = 080B.
$\overline{\text{RTCRES}}$	64	I	CMOS-S	Real-time clock reset. This signal resets the real time clock after a battery power-up.
RTCRTN	60	I		Real-time clock oscillator ground terminal. This terminal provides ground return for the 32.768-kHz crystal timing capacitor to the onboard oscillator circuit.
RTCSQW	65	O	PP2	Real-time clock square-wave output. This signal is enabled through the RTC configuration registers.

ATU Terminal Descriptions (continued)

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TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
RTCXIN	61	I		Real-time clock oscillator input. This signal connects to a 32.768-kHz crystal or can be used as a frequency input pin. It is powered by battery.
RTCXOUT	62	O		Real-time clock oscillator output. This is the second terminal for the 32.768 kHz crystal. It is powered by battery.
SPEAKER	72	O	PP6	Speaker output. This is an ANDed output of data bit 1 of port B (I/O address 0061h) and the OUT2 output of the timer. For driving the speaker, an open collector TTL buffer or a transistor with a base resistor is necessary.
XD0-XD7	175–168	I/O	3S6	I/O Data lines 0–7 for the peripheral bus
$\overline{\text{XDSEL}}$	77	I	TTL-S	XD bus select. Driven by XD bus devices to indicate XD bus transfers.
Miscellaneous Signals				
CLKIN0	56	I	CMOS	Clock Input 0. One of the two oscillator inputs.
CLKIN1	58	I	CMOS	Clock Input 1. One of the two oscillator inputs.
CPUSTEN	55	I	TTL	CPU self-test enable. When active high (pulled up), the ATU will drive $\overline{\text{BUSY}}$ low during power-on reset and hold it low for 10 $\overline{\text{CLK2}}$ states following the negation of reset, indicating an 80386 self-test.
PWRGOOD	69	I	CMOS	Power good. Power supply generates this signal, which is used as a general reset input.
NU	78 - 81			Nonusable, make no external connection. Reserved for future use.
Power Terminals				
GND	10, 25, 37, 38, 57, 75, 95, 108, 120, 132, 133, 144, 159, 176, 192, 204	I		Ground
V_{CC}	5, 21, 35, 48, 70, 88, 101, 114, 127, 139, 149,167, 183, 198	I		Supply voltage

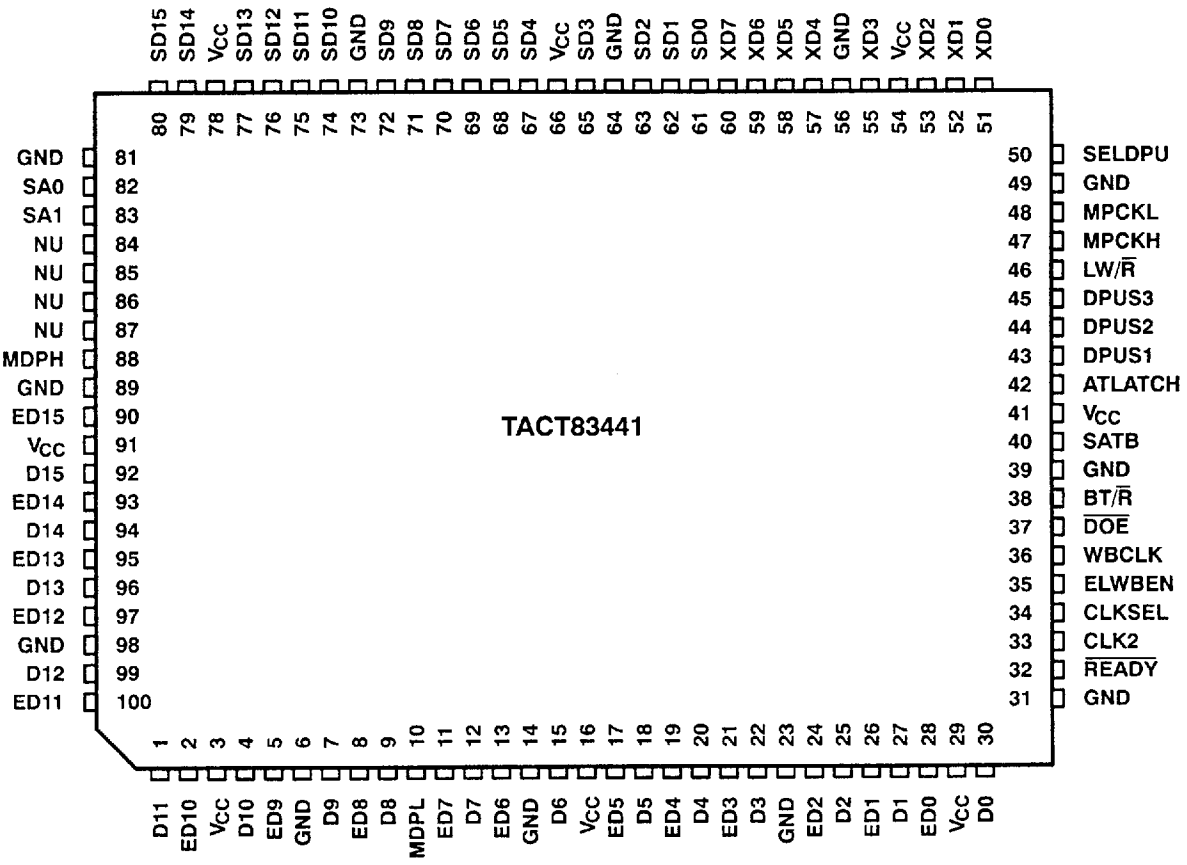
TACT83441 Data Path Unit (DPU)

The DPU provides data routing for all system data traffic. The data routing is provided by two sections of the DPU: the CPU and EL data buses (the D/ED data lines) and the AT data bus (the SD/XD data lines). For both read and write operations, data between these two sections is transferred through an AT bus buffer latch. An AT write buffer controlled by the ATU is also provided on the DPU. In addition, the DPU contains bus sizing and conversion logic for 8-bit and 16-bit AT bus accesses, and parity generation and checking logic.

DPU terminal assignments

The DPU is packaged in a 100-terminal QFP. The DPU Terminal Function Table gives a description of each terminal. See Figure 1 for details of the I/O buffer types.

Top View



NU – Nonusable, make no external connection. These are reserved for future use.

DPU Terminal Functions

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TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
DPU Control Signals				
ATLATCH	42	I	CMOS	AT read/write buffer latch control. Data is latched in the AT read/write buffer on the rising edge of this input.
BT/$\overline{R}$	38	I	TTL	Bus transmit/receive. CPU D bus transceiver direction control. This signal is sourced by the cache controller or connects to the ATU LW/$\overline{R}$ signal in a non-cache system.
CLKSEL	34	I	CMOS	Clock select input. Used for inverting the CLK2 input. L 386DX or 386SX H Reserved
$\overline{DOE}$	37	I	TTL	Data output enable control. CPU D bus transceiver output control. This signal is sourced either by the cache controller or, in a non–cached system, by the ATU.
DPUS1	43	I	CMOS	AT bus source select bit 1
DPUS2	44	I	CMOS	AT bus source select bit 2
DPUS3	45	I	CMOS	AT bus conversion control
ELWBEN	35	I	CMOS	EL bus write buffer enable L Disable write buffer H Enable write buffer
LW/$\overline{R}$	46	I	CMOS	Latched write/read signal from ATU
MPCKH	47	O	PP6	Latched parity high byte status
MPCKL	48	O	PP6	Latched parity low byte status
SATB	40	I	CMOS	CPU/EL bus source/destination control for the AT bus buffer
SELDPU	50	I	CMOS	DPU word select L Low word (D15–0) in a 16-bit or 32-bit system H High word (D31–16) in a 32-bit system **Note:** SA1 must also be tied low in a 16-bit system.
WBCLK	36	I	TTL	Write buffer clock. Latch signal for cache controller posted write operations. Write data is latched on the rising edge of WBCLK.
Data Signals				
D0–D2 D3–D5 D6–D8 D9–D12 D13–D15	30, 27, 25, 22, 20, 18, 15, 12, 9, 7, 4, 1, 99, 96, 94, 92	I/O	3S16PU	CPU data lines 0–15
ED0–ED2 ED3–ED5 ED6–ED8 ED9–ED11 ED12–ED14 ED15	28, 26, 24, 21, 19, 17, 13, 11, 8, 5, 2, 100, 97, 95, 93, 90	I/O	3S16PU	EL bus data lines 0–15
MDPL	10	I/O	3S16PU	EL bus parity bit for the low byte
MDPH	88	I/O	3S16PU	EL bus parity bit for the high byte

DPU Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
SD0–SD3 SD4–SD9 SD10–SD13 SD14–SD15	61–63, 65 67–72 74–77 79–80	I/O	3S24PU	AT bus system data bits 0–15
XD0–XD3 XD4–XD7	51–53, 55 57–60	I/O	3S10PU	XD bus peripheral data bits 0–7
Miscellaneous Signals				
CLK2	33	I	CMOS	CPU system clock
$\overline{\text{READY}}$	32	I	TTL	CPU or EL bus ready input
SA0	82	I	TTL	AT bus system address line 0
SA1	83	I	TTL	AT bus system address line 1. Must be tied low in a 16-bit system.
NU	84–87			Nonusable, make no external connection. Reserved for future use.
Power Terminals				
GND	6, 14, 23, 31, 39, 49, 56, 64, 73, 81, 89, 98	I		Ground
V_{CC}	3, 16, 29, 41, 54, 66, 78, 91	I		Supply voltage

TACT83442 Memory Control Unit (MCU)

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The MCU is a high-performance, programmable DRAM controller with an address range of 32M bytes. The MCU provides several access modes, including normal, page, word-interleave, and page block-interleave modes, as well as programmable DRAM timing parameters. Its physical memory address is generated by the on-chip page mapping RAM (PMRAM). Each page may be enabled or disabled, allowing flexible memory configuration for shadow RAM and EMS 4.0 features.

The MCU can directly drive up to 36 DRAM devices. If the memory array contains more than 36 DRAM devices, then buffers are required for the memory address and write enable signals. DRAM configuration and timing parameters are programmed through the configuration registers and PMRAM in the MCU.

Up to eight MCUs can be cascaded to expand the system memory. The MCU base address register and page mapping RAM combine to provide memory configuration control in a multiple MCU environment. When multiple MCUs are used, they are initialized automatically at power up as MCU0, MCU1, . . . MCU7 for configuration. Since each MCU can manage up to 32M bytes, a fully cascaded system will provide control for up to 256M bytes.

memory array organization

The MCU configures system memory according to the processor being used. In a 386DX system, the MCU can support two 32-bit banks of DRAM, while in a 386SX system it can support four 16-bit banks. The MCU defines DRAM type based on bank pairs, allowing for a mixture of DRAM types in system memory. However, when memory interleaving is used, each bank pair must use identical DRAM types.

DRAM access modes and timing

The MCU supports normal and page DRAM access modes, as well as interleaving on page block, odd/even word, or double-word boundaries (depending on the memory data width of 16 or 32 bits). Interleaved banks must use identical DRAMs. Four interleaved 16-bit banks may be used as two pairs of banks, in which case the *pairs* may use different-sized DRAMs, but the banks *within* pairs must use identical DRAMs. If four banks are organized in two pairs, the banks within each pair must be interleaved.

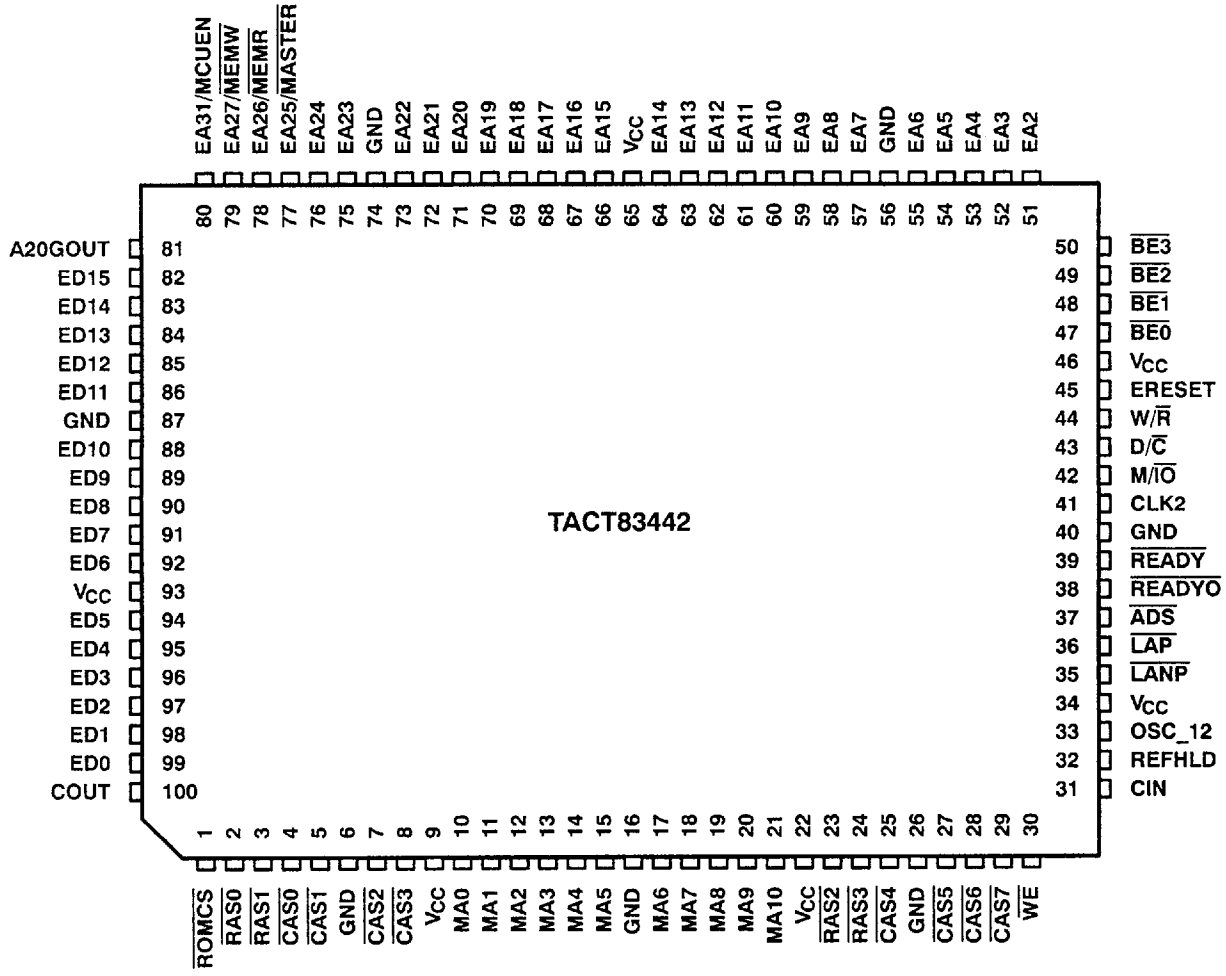
DRAM timing information is programmable for each pair of banks through separate configuration registers. Programmable parameters include $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse durations, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ precharge times, $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ delay, $\overline{\text{CAS}}$ active write delay, $\overline{\text{RAS}}$ to memory address delay, and memory address to $\overline{\text{CAS}}$ read delay.

The MCU supports a programmable DRAM refresh scheme with staggered $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$.

MCU terminal assignments

The MCU is packaged in a 100-terminal QFP. The MCU Terminal Functions Table gives a description of each terminal. See Figure 1 for details of the I/O buffer types.

Top View



MCU Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
EL Bus Signals				
$\overline{ADS}$	37	I	TTL	Address status control signal
$\overline{BE0}$	47	I	TTL	Byte enable 0. Used with the 386DX to enable data bits 0–7. The 386SX uses the signal $\overline{BLE}$ (Byte Low Enable).
$\overline{BE1}$	48	I	TTL	Byte enable 1. Used with the 386DX to enable data bits 8–15. The 386SX uses the signal $\overline{BHE}$ (Byte High Enable).
$\overline{BE2}$	49	I	TTL	Byte enable 2. Used with the 386DX to enable data bits 16–23. The 386SX uses the CPU address line A1.

MCU Terminal Functions (continued)

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TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
$\overline{BE3}$	50	I	TTL	Byte enable 3. Used with the 386DX to enable data bits 24–32. Tied high on 386SX systems.
CLK2	41	I	TTL	CPU system clock
D/$\overline{C}$	43	I	TTL	Data/code control signal
EA2–EA6 EA7–EA14 EA15–EA22 EA23–EA24	51–55 57–64 66–73 75–76	I	TTL	EL bus address bits 2–24 **Note:** In 386SX designs, EA24 must be tied low.
EA25/$\overline{MASTER}$ EA26/$\overline{MEMR}$ EA27/$\overline{MEMW}$ EA31/MCUEN	77 78 79 80	I I I I	TTL	Multiplexed EL address/AT control signal for support of AT master mode. The terminal definition is selected by mode select bits 2 and 3 of the configuration register.
ED0–ED5 ED6–ED10 ED11–ED15	99–94 92–88 86–82	I/O	3S10	EL bus data bits 0–15
ERESET	45	I	TTL	EL bus reset
M/$\overline{IO}$	42	I	TTL	Memory/IO control signal
$\overline{READY}$	39	I	TTL	Ready input signal. This $\overline{READY}$ is the output of the ANDed EL bus ready signals.
$\overline{READYO}$	38	O	PP10	Ready out control signal. Output to system ready generation logic. Must be ANDed with the other EL bus ready signals.
W/$\overline{R}$	44	I	TTL	Write/read control signal
Memory Control Signals				
$\overline{CAS0}$–$\overline{CAS3}$	4, 5, 7, 8	O	PP16	Column address strobe signals 0–3
CAS4–CAS7	25, 27–29	O	PP16	Column address strobe signals 4–7
$\overline{MA0}$–$\overline{MA5}$ $\overline{MA6}$–$\overline{MA10}$	10–15 17–21	O	PP16	Memory address multiplexer outputs 0–10
RAS0–RAS3	2, 3, 23, 24	O	PP16	Row address strobe signals for banks 0–3
WE	30	O	PP16	Write enable for DRAMs
MCU Control Signals				
A20GOUT	81	I	TTL	A20 gate output from the ATU in non-cached systems. It is tied high in cache-based systems (assuming AND gate is used between processor and cache for A20 control.)
CIN	31	I	TTL	MCU cascade input. Must be grounded for first MCU.
COUT	100	O	PP10	MCU cascade output. Connects to the CIN pin of the next MCU in the chain.
$\overline{LANP}$	35	O	PP10	EL bus local access with no parity
LAP	36	O	PP10	EL bus local access with parity
OSC_12	33	I	TTL	Oscillator frequency of 1.19 MHz, used for $\overline{RAS}$ duration time limit and refresh timing.
REFHLD	32	I	TTL	DRAM refresh inhibit
$\overline{ROMCS}$	1	O	PP10	ROM chip select. This signal is inactive if shadow RAM is enabled.

MCU Terminal Functions (continued)

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TERMINAL NAME	TERMINAL NO.	I/O	BUFFER TYPE	DESCRIPTION
Power Terminals				
GND	6, 16, 26, 40, 56, 74, 87	I		Ground
V_{CC}	9, 22, 34, 46, 65, 93	I		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous total power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: All voltage values are with respect to all GND terminals connected together.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range	20 MHz	4.5		5.5	V
V_{CC}	Supply voltage range	25 and 33 MHz	4.75		5.25	V
V_{batt}	Battery voltage (ATU only)	Backup	3		5.5	V
		Normal	V_{CC}−0.3		V_{CC}+0.3	
V_I	Input voltage range		0		V_{CC}	V
V_{IH}	High-level input voltage	TTL levels	2			V
V_{IL}	Low-level input voltage				0.8	
V_{IH}	High-level input voltage	CMOS level	0.7V_{CC}			
V_{IL}	Low-level input voltage				0.2V_{CC}	
t_t	Input transition time	(Except Schmitt-trigger inputs)	0		25	ns
T_A	Operating free-air temperature range		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going threshold level	Schmitt-trigger inputs				2	V
V_{T-}	Negative-going threshold level			0.8			V
V_{hys}	Hysteresis (see Note 2)			0.2		0.6	V
V_{OH}	High-level output voltage	PP2, 3S	I_{OH} = 2 mA	3.7			V
		PP6	I_{OH} = 6 mA	3.7			
		PP10, 3S	I_{OH} = 10 mA	3.7			
		PP16	I_{OH} = 16 mA	3.7			
		PP24, 3S	I_{OH} = 16 mA	3.7			
V_{OL}	Low-level output voltage	PP2, 3S, OD	I_{OL} = 2 mA			0.5	V
		PP6	I_{OL} = 6 mA			0.5	
		PP10, 3S	I_{OL} = 10 mA			0.5	
		PP16	I_{OH} = 16 mA			0.5	
		PP24, 3S, OD	I_{OL} = 24 mA			0.5	
I_I	Input current	CMOS	V_I = 0 to V_{CC}			±10	µA
		TTL Pullup input	V_I = 2.2 V	70		450	
			V_I = 0.4 V	80		500	
		TTL Pulldown input	V_I = 2.2 V	20		170	µA
			V_I = 4.5 V	35		200	
I_{OZ}	Off-state output current		V_O = 0 or V_{CC}			±10	µA
I_{CC}	Quiescent power supply current		V_{CC} = 5.25 V			100	µA
P_D	Power dissipation	ATU	See Note 3		75		mW
		MCU			460		
		DPU			40		
I_{batt}	Battery current	Backup	V_{batt} = 3.6 V		4	10	µA
		Backup	V_{batt} = 5.5 V			35	
		Normal	V_{batt} = V_{CC+} 0.3 V			100	µA
f_{RTC}	Real-time clock output frequency				32.768		kHz

NOTES: 2. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

3. System environment: 25-MHz CPU without cache operating in pipeline mode. 8-MHz AT bus. Relevant load capacitances equivalent to stated test conditions.

TEXAS INSTR (UC/UP) 53E D 8961722 0088643 2T6 TII2

TIMING AND SWITCHING DATA

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timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{c1}	Cycle time, CLKIN1, CLKIN0	25		20		15		ns
t_{w1}	Pulse duration, high or low	9		7		6		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d2}	Delay time, CLKIN1, CLKIN0 to CLK2 or ATCLK	Undivided	3	12	3	10	3	10	ns
t_{d3}	Delay time to CLK2OUT or ATCLK	Divided	4	18	4	16	4	16	ns

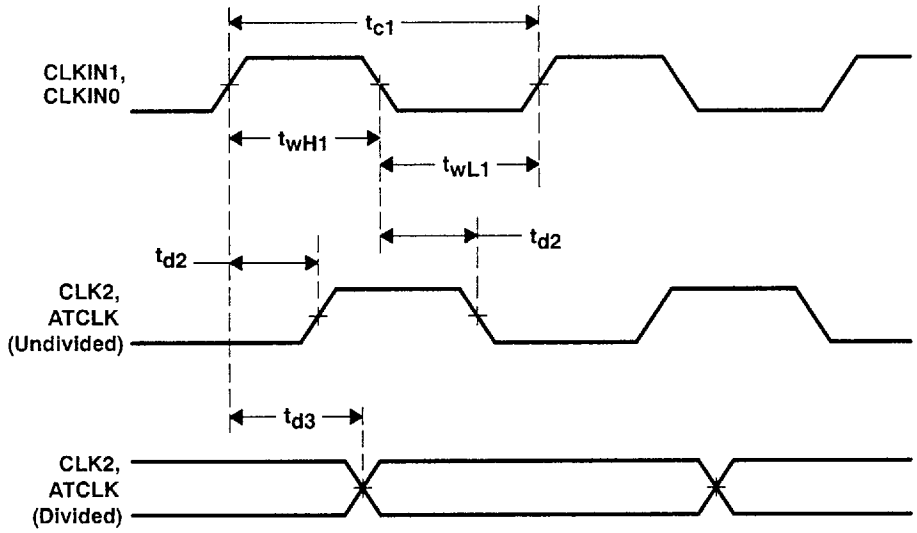


Figure 2. Clock Generator/Divider Waveforms

RESET/PCLK

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{c4}	Cycle time, CLK2IN high or low	25		20		15		ns
t_{w4}	Pulse duration, CLK2IN high or low	8		7		6		ns
t_{su6}	Setup time, PWRGOOD before CLK2IN↑	12		10		10		ns
t_{h6}	Hold time, PWRGOOD after CLK2IN↑	3		2		2		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d5}	Delay time, CLK2IN to PCLK		4	17	4	15	3	13	ns
t_{d7}	Delay time, CLK2IN to CPURST	C_L = 30 pF	4	13	4	12	3	11	ns
t_{d8}	Delay time, CLK2IN to ERESET and NPRST		4	13	4	12	3	11	ns

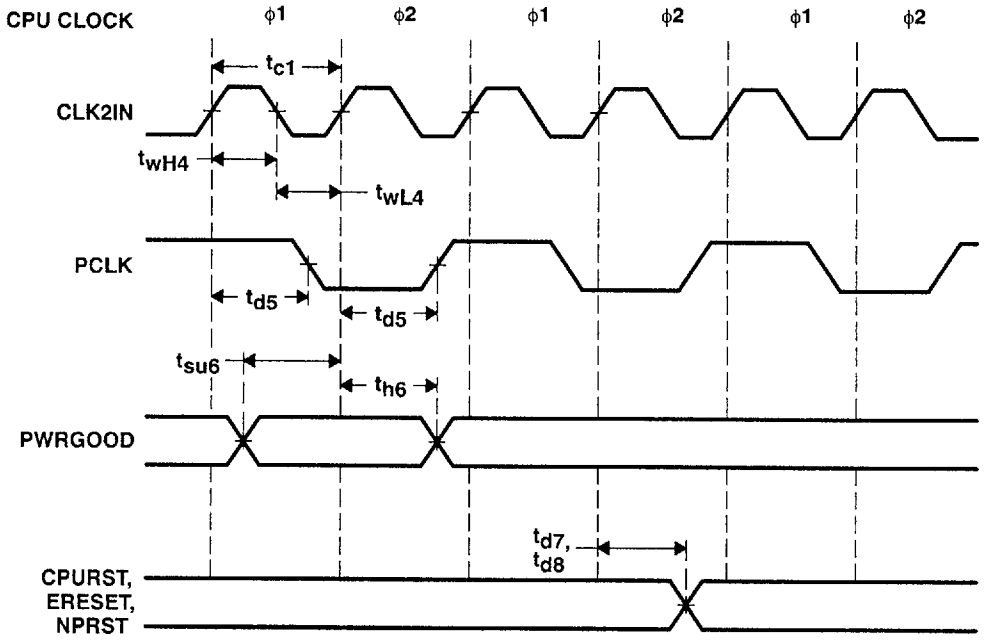


Figure 3. Reset/PCLK Waveforms

ATU SLAVE CYCLE: EL BUS SIGNALS

timing requirements, T_A = 0°C to 70°C

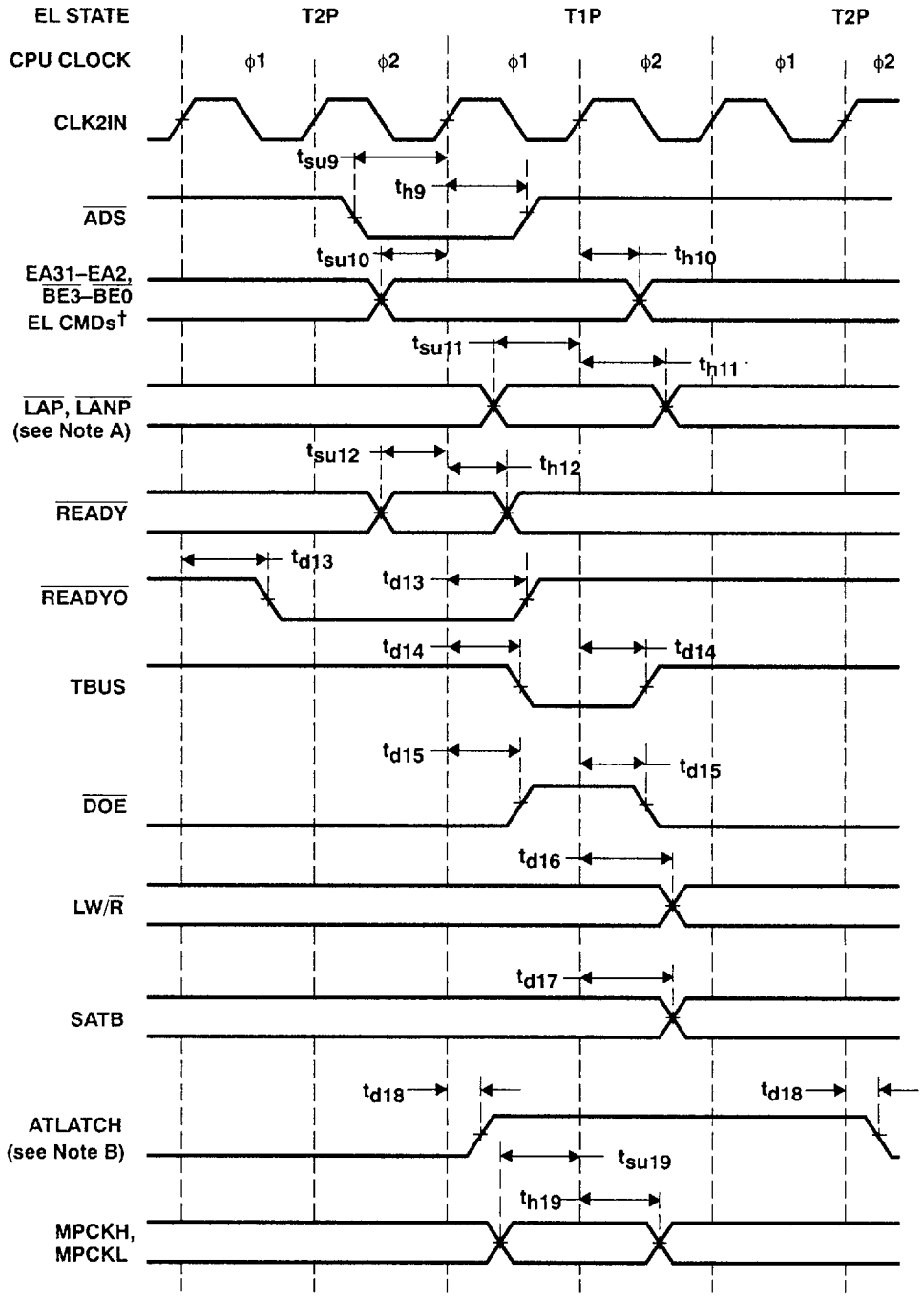
		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su9}	Setup time, $\overline{ADS}$ before CLK2IN↑	12		10		8		ns
t_{h9}	Hold time, $\overline{ADS}$ after CLK2IN↑	4		4		3		ns
t_{su10}	Setup time, EA31–EA2, $\overline{BE3}$–$\overline{BE0}$, and EL CMDs† before CLK2IN↑	9		7		5		ns
t_{h10}	Hold time, EA31–EA2, $\overline{BE3}$–$\overline{BE0}$, and EL CMDs† after CLK2IN↑	9		7		7		ns
t_{su11}	Setup time, $\overline{LAP}$ and $\overline{LANP}$ before CLK2IN↑	10		9		8		ns
t_{h11}	Hold time, $\overline{LAP}$ and $\overline{LANP}$ after CLK2IN↑	9		7		7		ns
t_{su12}	Setup time, $\overline{READY}$ before CLK2IN↑	12		10		7		ns
t_{h12}	Hold time, $\overline{READY}$ after CLK2IN↑	5		4		3		ns
t_{su19}	Setup time, MPCKH, MPCKL before CLK2IN↑	7		5		3		ns
t_{h19}	Hold time, MPCKH, MPCKL after CLK2IN↑	4		4		4		ns

† The EL CMDs consist of M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d13}	Delay time, CLK2IN to $\overline{READYO}$	C_L = 15 pF	3	14	3	13	3	12	ns
t_{d14}	Delay time, CLK2IN to TBUS		4	20	4	18	4	15	ns
t_{d15}	Delay time, CLK2IN to $\overline{DOE}$	See Note	5	22	5	20	5	17	ns
t_{d16}	Delay time, CLK2IN to LW/$\overline{R}$		4	20	4	18	4	15	ns
t_{d17}	Delay time, CLK2IN to SATB		5	22	5	20	5	17	ns
t_{d18}	Delay time, CLK2IN to ATLATCH		4	20	4	18	4	15	ns

NOTE: For 33-MHz operation, the MCU DRAM control register CWD bit = 1.



† The EL CMDs consist of M/IO, W/R, and D/C.

NOTES: A. LAP/LANP sampled at center of T1P. Can also be sampled at end of T1P. Sampling is controlled by BCTT bit of ATU timing control register.

B. The ATU timing control register AT write bit is enabled.

C. The EL bus cycle states are as follows: T1 = idle, T1 = first state of cycle, T2 = second state of cycle, T1P = first state of cycle in pipelined mode, T2P = subsequent state of cycle in pipelined mode, Tx = any state.

Figure 4. EL Bus Waveforms

ATU SLAVE CYCLE: AT BUS NORMAL 8-BIT AND 16-BIT CYCLES

timing requirements, T_A = 0°C to 70°C

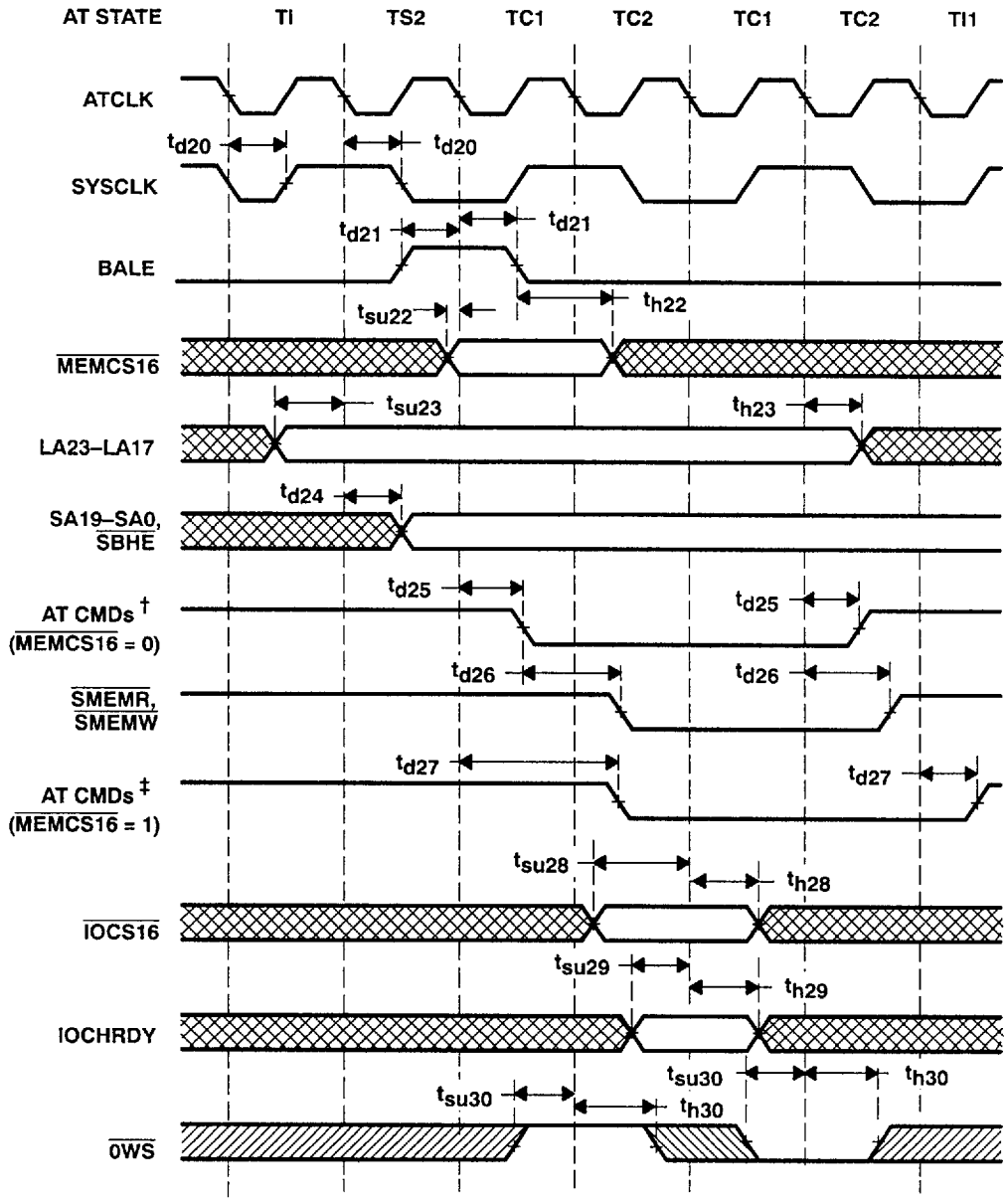
		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su22}	Setup time, $\overline{\text{MEMCS16}}$ before ATCLK↓	10		8		8		ns
t_{h22}	Hold time, $\overline{\text{MEMCS16}}$ after BALE↓	12		10		10		ns
t_{su23}	Setup time, LA23–LA17 before ATCLK↓	(See Note 3)		(See Note 3)		(See Note 3)		ns
t_{h23}	Hold time, LA23–LA17 after ATCLK↓	3 × CLK2		3 × CLK2		3 × CLK2		ns
t_{su28}	Setup time, $\overline{\text{IOCS16}}$ before ATCLK↓	7		5		5		ns
t_{h28}	Hold time, $\overline{\text{IOCS16}}$ after ATCLK↓	12		10		10		ns
t_{su29}	Setup time, IOCHRDY before ATCLK↓	7		5		5		ns
t_{h29}	Hold time, IOCHRDY after ATCLK↓	12		10		10		ns
t_{su30}	Setup time, $\overline{\text{0WS}}$ before ATCLK↓	7		5		5		ns
t_{h30}	Hold time, $\overline{\text{0WS}}$ after ATCLK↓	12		10		10		ns

NOTE 4: Default MIN = 2 × CLK2. When early AT bus control trigger is selected, MIN = 1 × CLK2. MAX = MIN + 2 × ATCLK.

switching characteristics, T_A = 0°C to 70°C, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d20}	Delay time, ATCLK to SYSCLK	C_L = 50 pF	6	22	6	22	6	22	ns
t_{d21}	Delay time, ATCLK to BALE	C_L = 50 pF	8	25	8	25	8	25	ns
t_{d24}	Delay time, ATCLK to SA19–SA0 and $\overline{\text{SBHE}}$		10	32	10	32	10	32	ns
t_{d25}	Delay time, ATCLK to AT CMDs†	$\overline{\text{MEMCS16}}$ = 0	8	30	8	30	8	30	ns
t_{d26}	Delay time, AT CMDs† to $\overline{\text{SMEMW}}$ and $\overline{\text{SMEMR}}$	$\overline{\text{MEMCS16}}$ = 0	6	22	6	22	6	22	ns
t_{d27}	Delay time, ATCLK to AT CMDs‡	$\overline{\text{MEMCS16}}$ = 1	8	30	8	30	8	30	ns

† The AT CMDs are $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$.
‡ The AT CMDs are $\overline{\text{SMEMW}}$, $\overline{\text{SMEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$.



† The AT CMDs are $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$.
‡ The AT CMDs are $\overline{\text{SMEMW}}$ and $\overline{\text{SMEMR}}$.
NOTE: The AT bus cycle states are as follows: Ti = idle, TS = status state, TC = command state, and Tx = any state.

Figure 5. AT Bus Waveforms (Normal 8-Bit and 16-Bit Cycles)

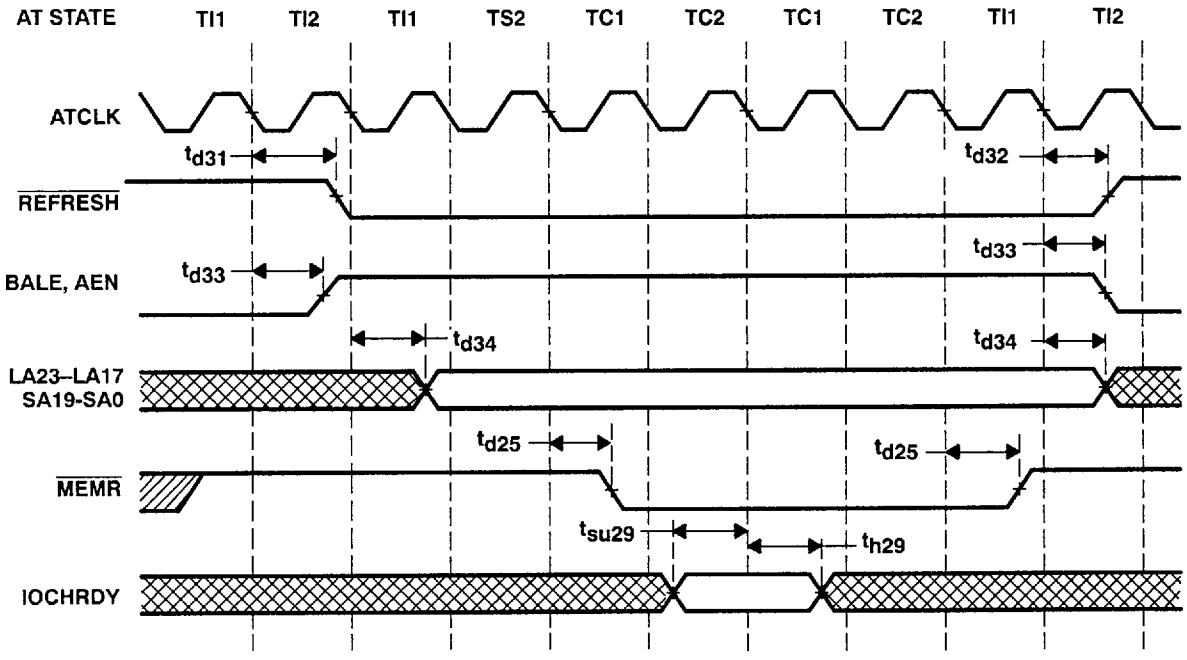
ATU SLAVE CYCLE: REFRESH

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su29}	Setup time, IOCHRDY before ATCLK↓	7		5		5		ns
t_{h29}	Hold time, IOCHRDY after ATCLK↓	12		10		10		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d31}	Delay time, ATCLK to $\overline{\text{REFRESH}}$↓		8	30	8	30	8	30	ns
t_{d32}	Delay time , ATCLK to $\overline{\text{REFRESH}}$↑	C_L = 0	8	30	8	30	8	30	ns
t_{d33}	Delay time, ATCLK to AEN and BALE		8	25	8	25	8	25	ns
t_{d34}	Delay time, ATCLK to LA23–LA17 and SA19–SA0		10	35	10	35	10	35	ns
t_{d25}	Delay time, ATCLK to $\overline{\text{MEMR}}$		8	30	8	30	8	30	ns



NOTE: The AT bus cycle states are as follows: Ti = idle, TS = status state, TC = command state, and Tx = any state.

Figure 6. AT Bus Refresh Waveforms

ATU MASTER CYCLE: EL BUS DMA CYCLE – HOLD REQUEST

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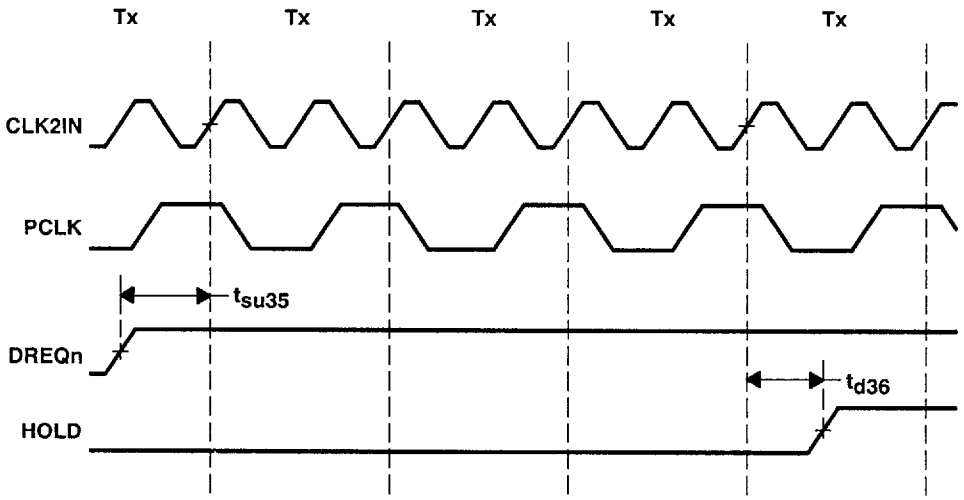
timing requirements, T_A = 0°C to 70°C

	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
	V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{su35} Setup time, DREQn before CLK2IN↑	15		13		11		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER	TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{d36} Delay time, CLK2IN to HOLD		4	20	4	18	4	15	ns



NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 7. EL Bus DMA Cycle Waveforms – HOLD Request

ATU MASTER CYCLE: EL BUS DMA CYCLE – SINGLE TRANSFER MODE (1 WAIT STATE)

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{h35}	Hold time, DREQn after CLK2IN↑	5		5		5		ns
t_{su37}	Setup time, HOLDA before CLK2IN↑	14		12		10		ns
t_{su12}	Setup time, $\overline{READY}$ before CLK2IN↑	12		10		7		ns
t_{h12}	Hold time, $\overline{READY}$ after CLK2IN↑	5		4		3		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d38}	Delay time, CLK2IN to $\overline{DACKn}$		6	30	6	27	6	22	ns
t_{d39}	Delay time, CLKIN to $\overline{ADS}$		5	28	5	23	5	18	ns
t_{en39}	Enable time, CLK2IN to $\overline{ADS}$		5	28	5	23	5	18	ns
t_{dis40}	Disable time, CLK2IN to $\overline{ADS}$	C_L = 0	5	28	5	25	5	21	ns
t_{en41}	Enable time, CLK2IN to EL CMDs†		5	28	5	23	5	18	ns
t_{dis42}	Disable time, CLK2IN to EL CMDs†	C_L = 0	5	28	5	25	5	21	ns
t_{en43}	Enable time, CLK2IN to EA31–EA2 and $\overline{BE3}$–$\overline{BE0}$		5	28	5	23	5	19	ns
t_{dis44}	Disable time, CLK2IN to EA31–EA2 and $\overline{BE3}$–$\overline{BE0}$	C_L = 0	5	28	5	25	5	21	ns
t_{d45}	Delay time, CLK2IN to TC		5	35	5	31	5	25	ns

† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.

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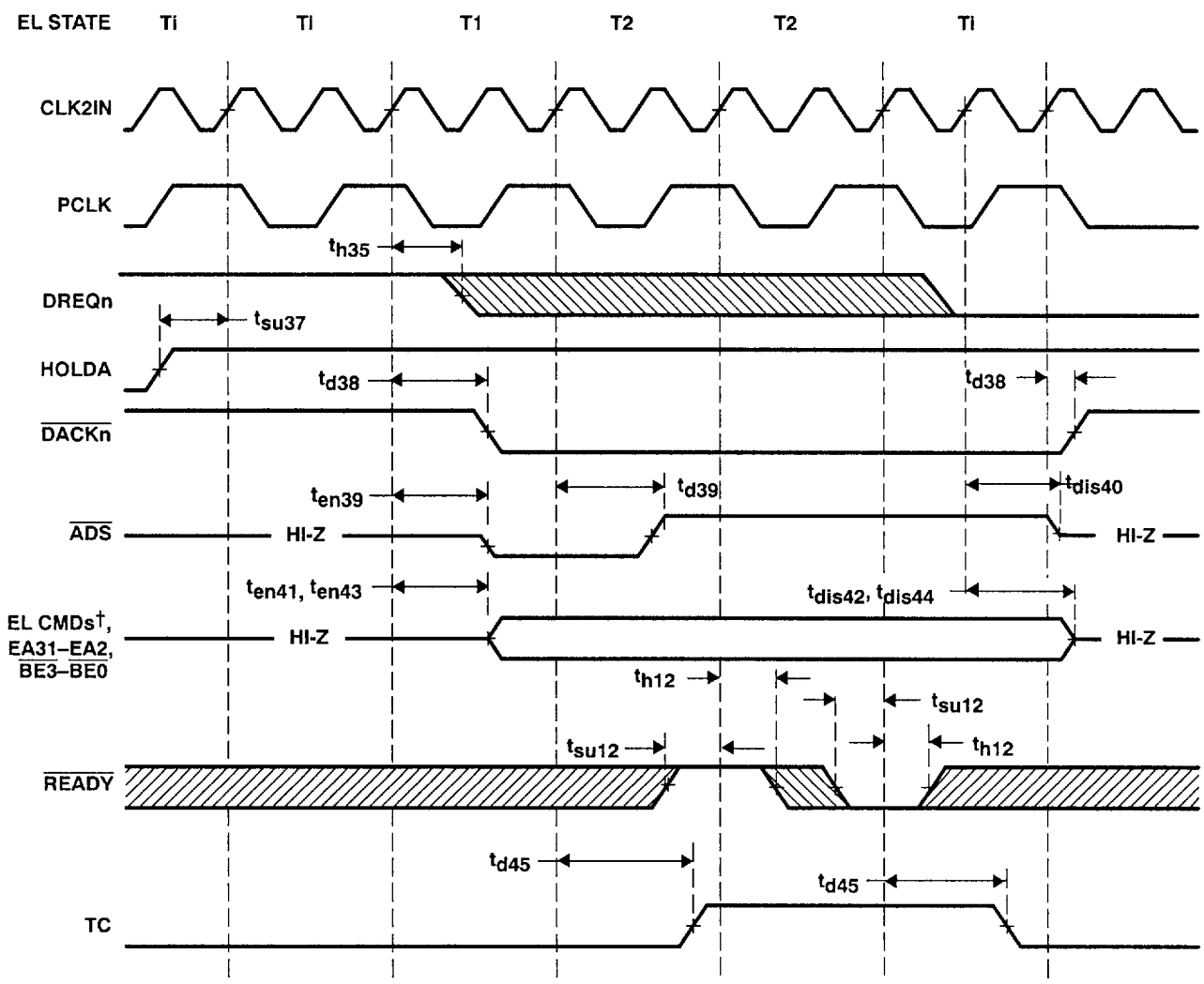

† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.

NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 8. EL Bus DMA Cycle Waveforms – Single Transfer Mode (1 Wait State)

ATU MASTER CYCLE: EL BUS DMA CYCLE – BLOCK DEMAND TRANSFER MODE (0 WAIT STATE)

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su35}	Setup time, DREQn before CLK2IN↑	15		15		15		ns
t_{h35}	Hold time, DREQn after CLK2IN↑	5		5		5		ns
t_{su37}	Setup time, HOLDA before CLK2IN↑	14		12		10		ns
t_{su12}	Setup time, $\overline{\text{READY}}$ before CLK2IN↑	12		10		7		ns
t_{h12}	Hold time, $\overline{\text{READY}}$ after CLK2IN↑	5		4		3		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d38}	Delay time, CLK2IN to $\overline{\text{DACKn}}$		6	30	6	27	6	22	ns
t_{d39}	Delay time, CLK2IN to $\overline{\text{ADS}}$		5	28	5	23	5	18	ns
t_{en39}	Enable time, CLK2IN to $\overline{\text{ADS}}$		5	28	5	23	5	18	ns
t_{en41}	Enable time, CLK2IN to EL CMDs†		5	28	5	23	5	18	ns
t_{d43}	Delay time, CLK2IN to EA31–EA2 and $\overline{\text{BE3}}$–$\overline{\text{BE0}}$		5	28	5	23	5	19	ns
t_{en45}	Enable time, CLK2IN to EA31–EA2 and $\overline{\text{BE3}}$–$\overline{\text{BE0}}$		5	28	5	23	5	19	ns
t_{d45}	Delay time, CLK2IN to TC		5	35	5	31	5	25	ns

† The EL CMDs are M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$, and D/$\overline{\text{C}}$.

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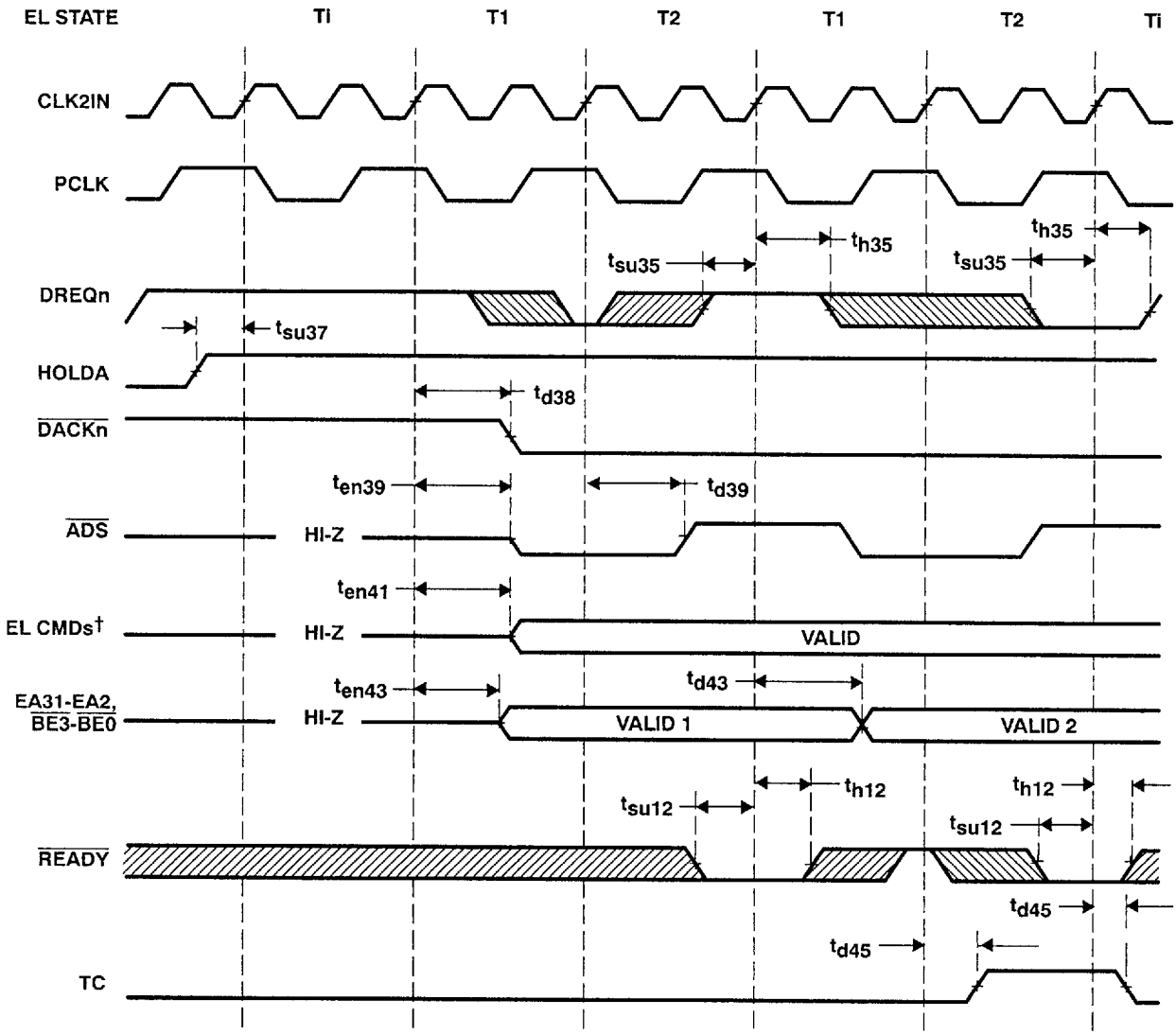


† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.

NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

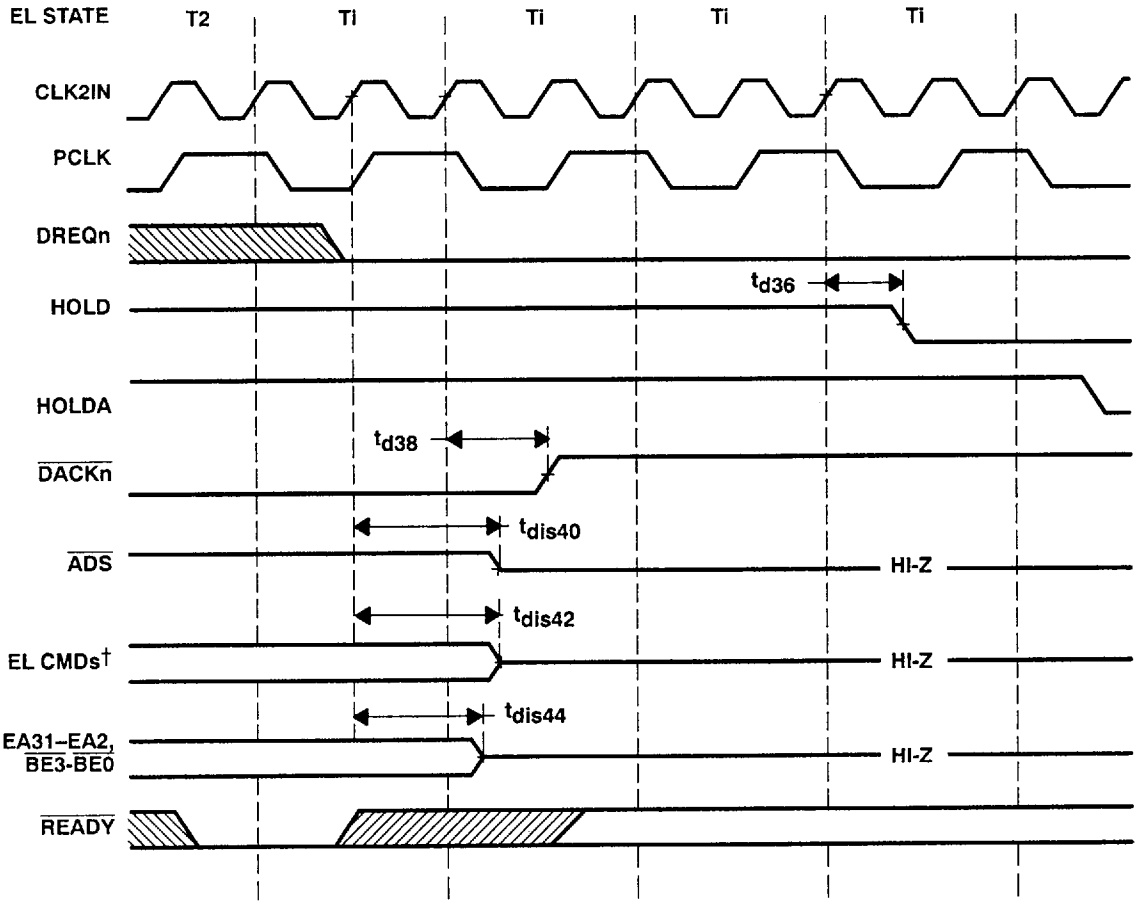
Figure 9. EL Bus DMA Cycle Waveforms – Block Demand Transfer Mode (0 Wait States)

ATU MASTER CYCLE: EL BUS DMA CYCLE – EXITING

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d36}	Delay time, CLK2IN to HOLD		4	20	4	18	4	15	ns
t_{d38}	Delay time, CLK2IN to $\overline{DACKn}$		6	30	6	27	6	22	ns
t_{dis40}	Disable time, CLK2IN to $\overline{ADS}$	C_L = 0	5	28	5	25	5	21	ns
t_{dis42}	Disable time, CLK2IN to EL CMDs†	C_L = 0	5	28	5	25	5	21	ns
t_{dis44}	Disable time, CLK2IN to EA31–EA2 and $\overline{BE3}$–$\overline{BE0}$	C_L = 0	5	28	5	25	5	21	ns

† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.



† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.

NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 10. EL Bus DMA Cycle Waveforms – Exiting

ATU MASTER CYCLE: EL BUS DMA CYCLE – CASCADE

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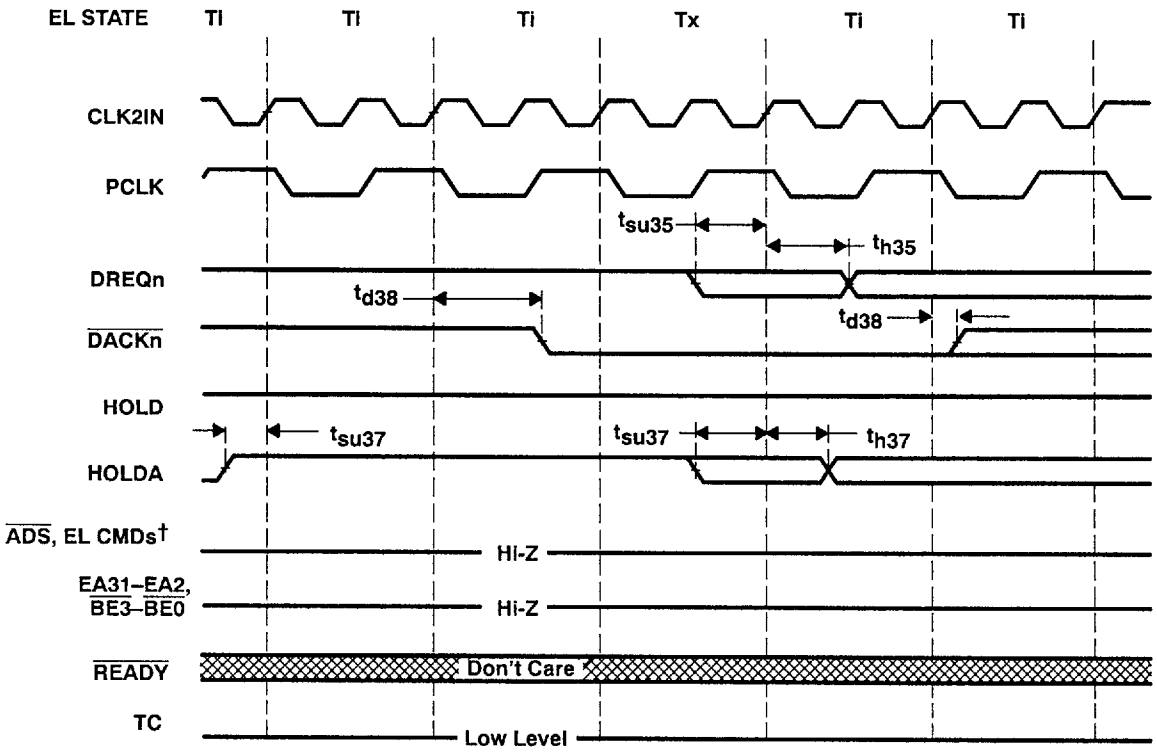
timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su35}	Setup time, DREQn before CLK2IN↑	15		13		11		ns
t_{h35}	Hold time, DREQn after CLK2IN↑	5		5		5		ns
t_{su37}	Setup time, HOLDA before CLK2IN↑	14		12		10		ns
t_{h37}	Hold time, HOLDA after CLK2IN↑	4		4		3		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d38}	Delay time, CLK2IN to $\overline{DACKn}$		6	30	6	27	6	22	ns



† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.
NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 11. EL Bus DMA Cycle Waveforms – Cascade

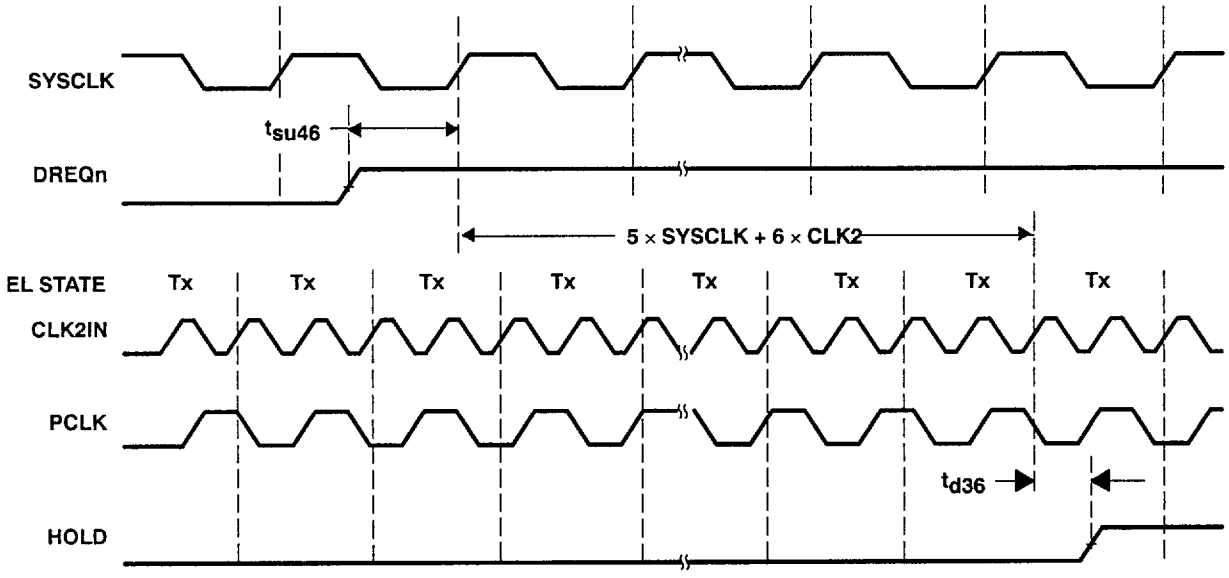
ATU MASTER CYCLE: AT BUS DMA CYCLE – HOLD REQUEST

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su46}	Setup time, DREQn before SYSCLK↑	15		15		15		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d36}	Delay time, CLK2IN to HOLD		4	20	4	18	4	15	ns



NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 12. AT Bus DMA Cycle Waveforms – HOLD Request

ATU MASTER CYCLE: AT BUS DMA CYCLE – EL BUS SIGNALS

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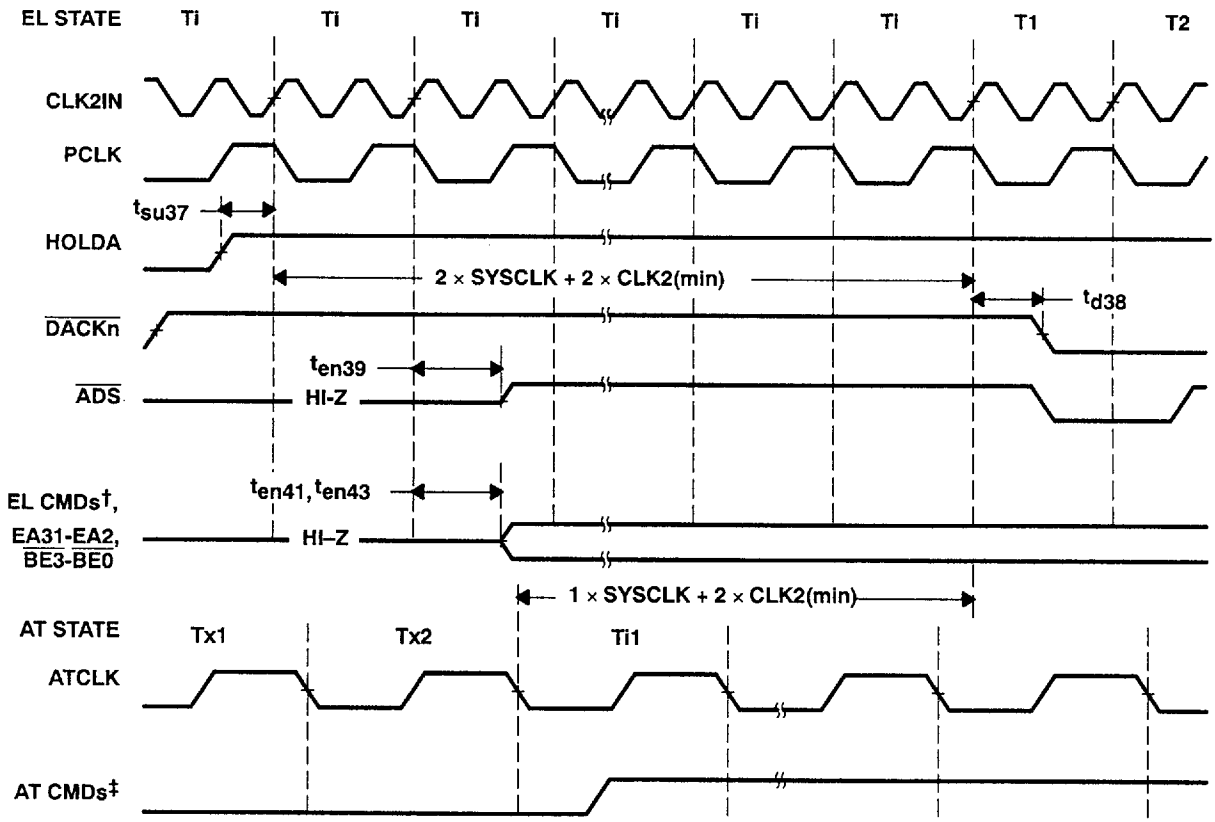
timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su37}	Setup time, HOLDA before CLK2IN↑	14		12		10		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d38}	Delay time, CLK2IN to $\overline{DACKn}$		6	30	6	27	6	22	ns
t_{en39}	Enable time, CLK2IN to $\overline{ADS}$		5	28	5	23	5	18	ns
t_{en41}	Enable time, CLK2IN to EL CMDs†		5	28	5	23	5	18	ns
t_{en43}	Enable time, CLK2IN to EA31–EA2 and $\overline{BE3}$–$\overline{BE0}$		5	28	5	28	5	28	ns

† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.



† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.
‡ The AT CMDs are $\overline{SMEMW}$, $\overline{SMEMR}$, $\overline{MEMW}$, $\overline{MEMR}$, $\overline{IOW}$, and $\overline{IOR}$.
NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 13. AT Bus DMA Cycle Waveforms – EL Bus Signals

ATU MASTER CYCLE: AT BUS DMA CYCLE – AT BUS SIGNALS

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su29}	Setup time, IOCHRDY before ATCLK↓	7		5		5		ns
t_{h29}	Hold time, IOCHRDY after ATCLK↓	12		10		10		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d21}	Delay time, ATCLK to BALE and AEN	C_L = 50 pF	8	25	8	25	8	25	ns
t_{d24}	Delay time, ATCLK to LA23–LA17, SA19–SA0, and $\overline{SBHE}$		10	32	10	32	10	32	ns
t_{d26}	Delay time, ATCLK to $\overline{IOR}$		8	30	8	30	8	30	ns
t_{d26}	Delay time, ATCLK to $\overline{IOW}$, $\overline{MEMW}$, and $\overline{MEMR}$		8	30	8	30	8	30	ns

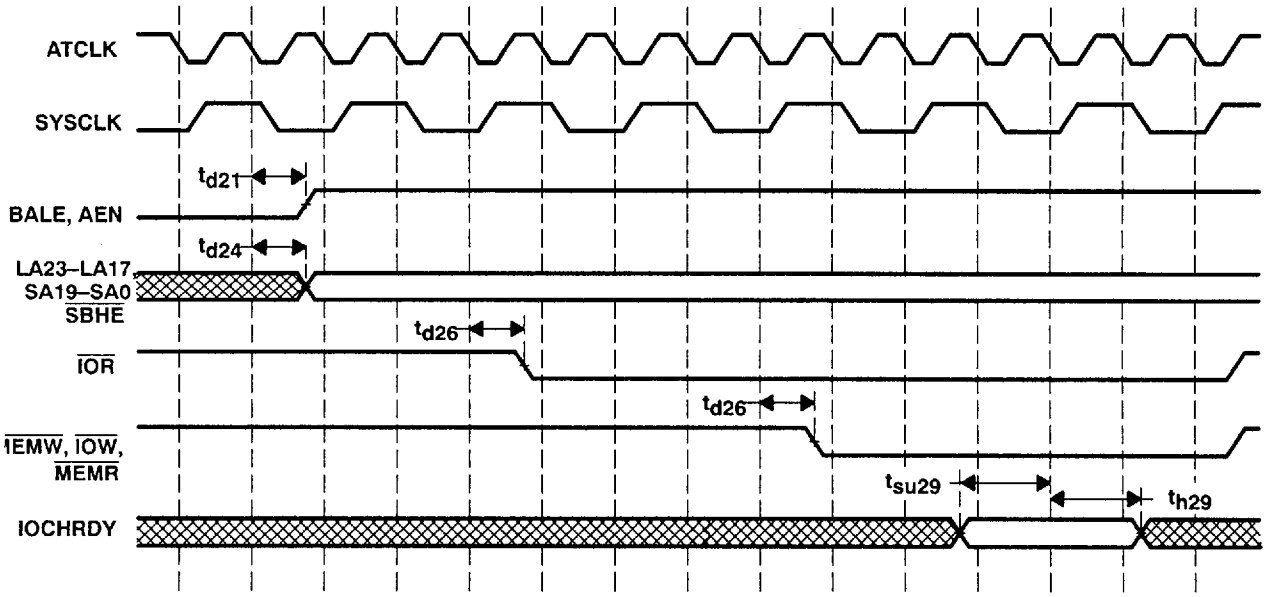


Figure 14. AT Bus DMA Cycle Waveforms – AT Bus Signals

ATU MASTER CYCLE: AT BUS DMA CASCADE – RELEASE/CAPTURE

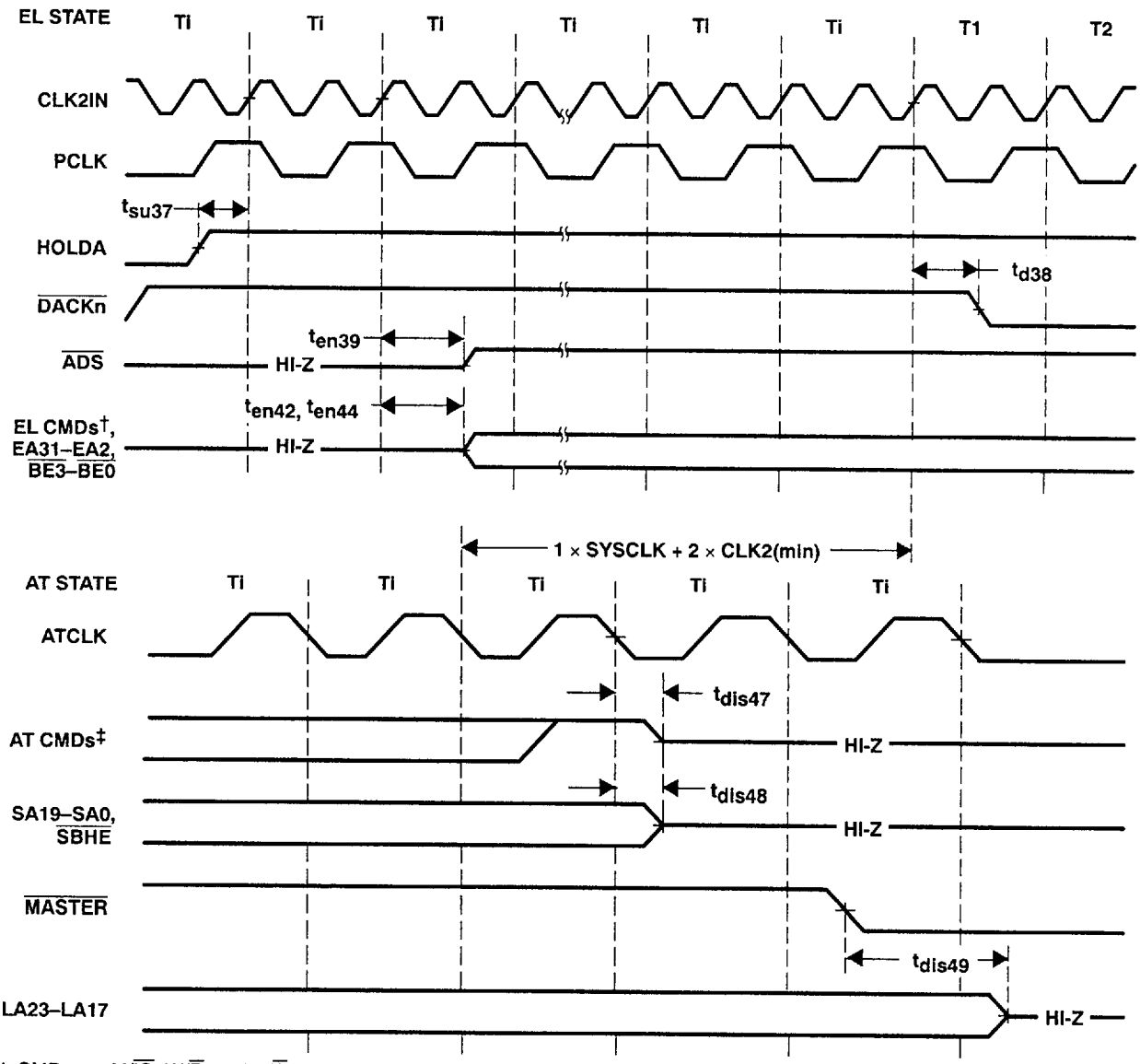
timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su37}	Setup time, HOLDA before CLK2IN↑	14		12		10		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF(unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d38}	Delay time, CLK2IN to $\overline{DACKn}$		6	30	6	27	6	22	ns
t_{en39}	Enable time, CLK2IN to $\overline{ADS}$		5	28	5	23	5	18	ns
t_{en42}	Enable time, CLK2IN to EL CMDs†		5	28	5	25	5	21	ns
t_{en44}	Enable time, CLK2IN to EA31–EA2 and $\overline{BE3}$–$\overline{BE0}$		5	28	5	25	5	21	ns
t_{dis47}	Disable time, ATCLK to AT CMDs‡	C_L = 0	8	35	8	35	8	35	ns
t_{dis48}	Disable time, ATCLK to SA19–SA0 and $\overline{SBHE}$	C_L = 0	8	35	8	35	8	35	ns
t_{dis49}	Disable time, $\overline{MASTER}$ to LA23–LA17	C_L = 0	5	22	5	22	5	22	ns

† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.
‡ The AT CMDs are $\overline{SMEMW}$, $\overline{SMEMR}$, $\overline{MEMW}$, $\overline{MEMR}$, $\overline{IOW}$, and $\overline{IOR}$.



† The EL CMDs are M/$\overline{IO}$, W/$\overline{R}$, and D/$\overline{C}$.
‡ The AT CMDs are $\overline{SMEMW}$, $\overline{SMEMR}$, $\overline{MEMW}$, $\overline{MEMR}$, $\overline{IOW}$, and $\overline{IOR}$.
NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.

Figure 15. AT Bus DMA Cascade Waveforms – Capture/Release

ATU MASTER CYCLE: AT BUS DMA CASCADE – AT-TO-EL BUS CYCLE CONVERSION

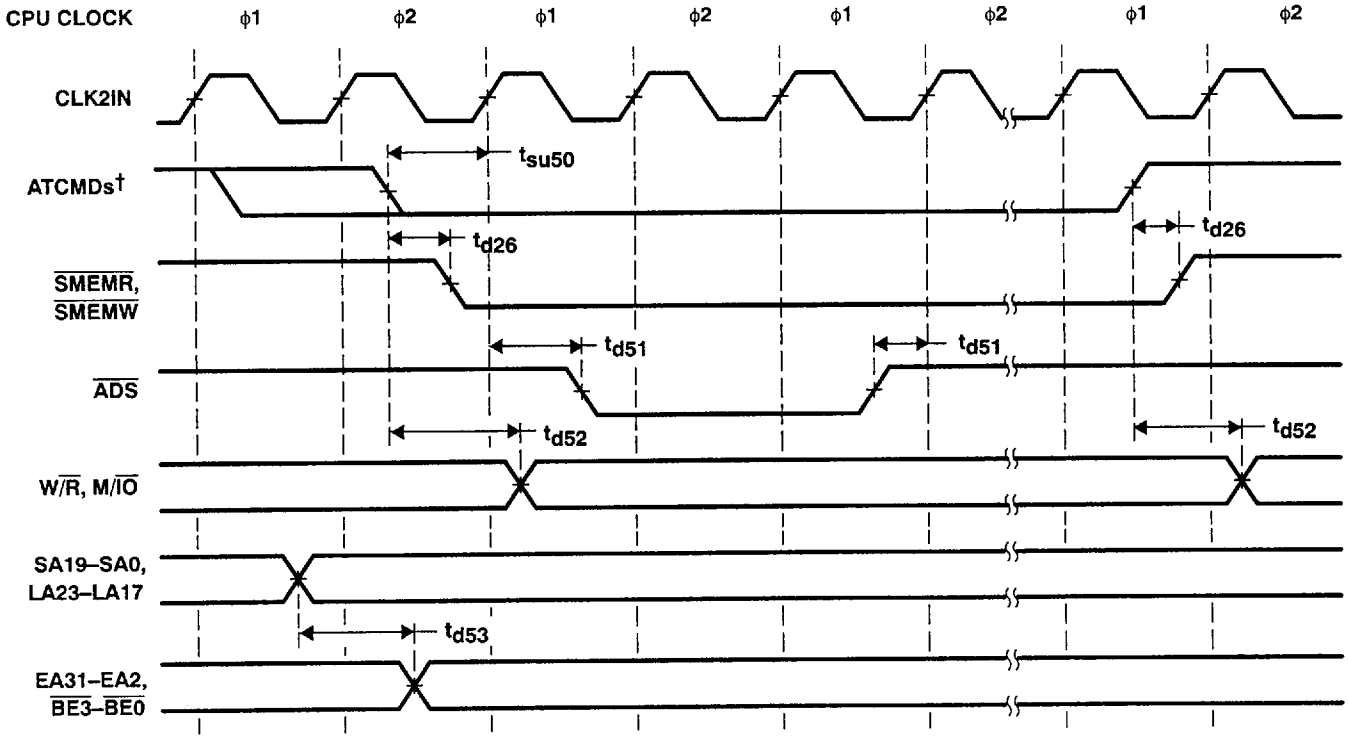
timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su50}	Setup time, AT CMDs† before CLK2IN↑	12		10		10		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d51}	Delay time, CLK2IN to $\overline{ADS}$		5	28	5	23	5	18	ns
t_{d26}	Delay time, AT CMDs† to $\overline{SMEMR}$/$\overline{SMEMW}$	C_L = 100 pF	6	22	6	22	6	22	ns
t_{d52}	Delay time, AT CMDS† to M/$\overline{IO}$ and W/$\overline{R}$		5	28	5	25	5	25	ns
t_{d53}	Delay time, SA19–SA0 and LA23–LA17 to EA31–EA0 and $\overline{BE3}$–$\overline{BE0}$		5	28	5	25	5	25	ns

† The AT CMDs are $\overline{MEMW}$, $\overline{MEMR}$, $\overline{IOW}$, and $\overline{IOR}$.



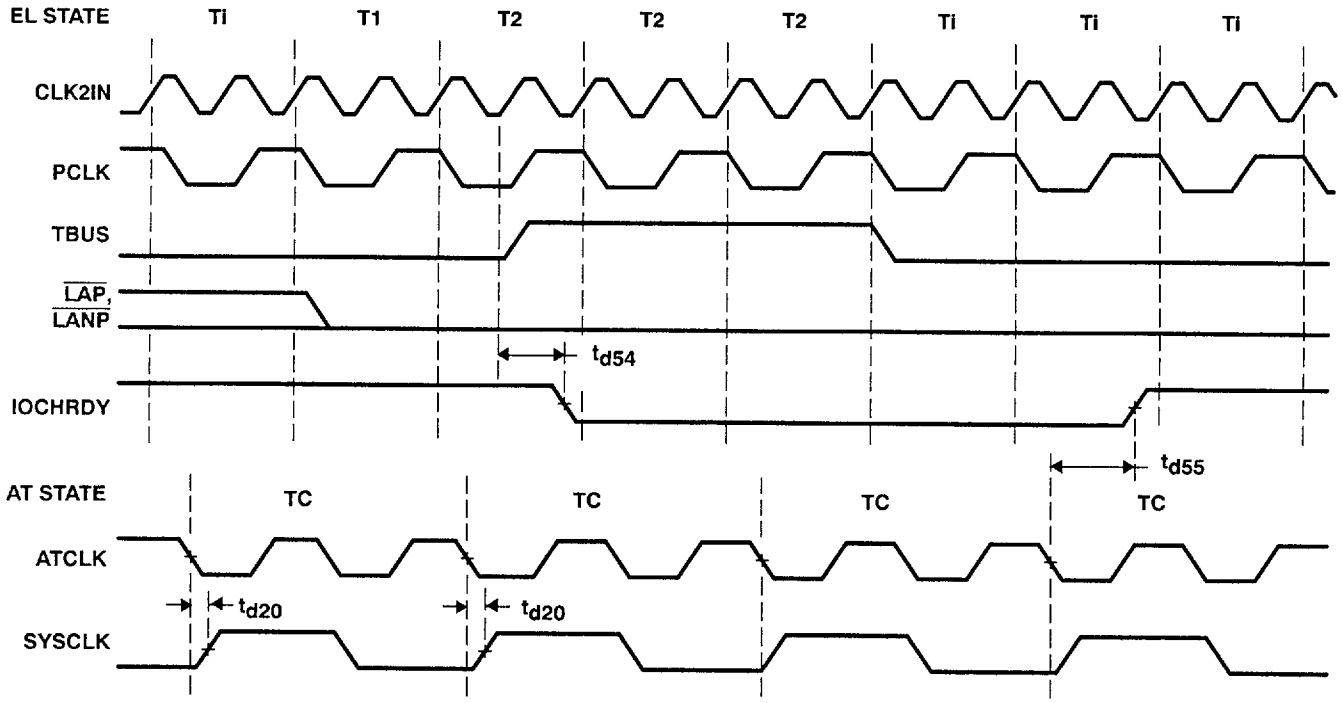
† The AT CMDs are $\overline{SMEMW}$, $\overline{SMEMR}$, $\overline{MEMW}$, $\overline{MEMR}$, $\overline{IOW}$, and $\overline{IOR}$.

Figure 16. AT Bus DMA Cascade Waveforms – AT-to-EL Bus Cycle Conversion

ATU MASTER CYCLE: IOCHRDY DRIVE

switching characteristics, T_A = 0°C to 70°C, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz, V_{CC} = 5 V ± 10%		f = 25 MHz, V_{CC} = 5 V ± 5%		f = 33 MHz, V_{CC} = 5 V ± 5%		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d54}	Delay time, CLK2IN to IOCHRDY		5	28	5	25	5	23	ns
t_{d55}	Delay time, ATCLK to IOCHRDY	C_L = 0	5	30	5	30	5	30	ns
t_{d20}	Delay time, ATCLK to SYSCLK		6	22	6	22	6	22	ns



NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = subsequent state of cycle, and Tx = any state.
The AT bus cycle states are as follows: Ti = idle, TS = status cycle, TC = command state, and Tx = any state.

Figure 17. IOCHRDY Drive Waveforms

DPU INTERFACE: SELECT CODE

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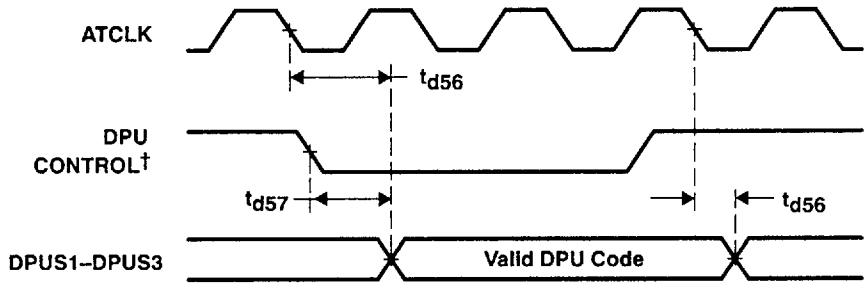
switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d56}	Delay time, ATCLK to DPUS3–DPUS1		5	22	5	20	5	20	ns
t_{d57}	Delay time, DPU Control† to DPUS3-DPUS1		5	27	5	25	5	25	ns



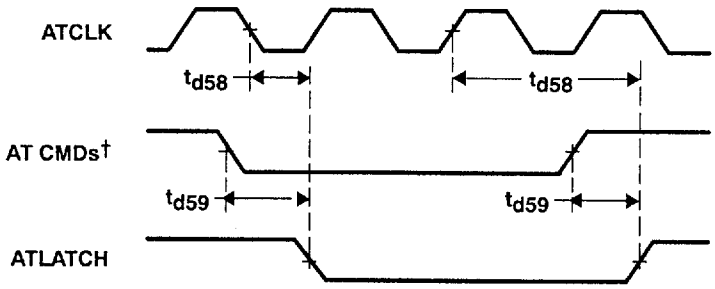
† The DPU control signals consist of SA0, $\overline{\text{IOCS16}}$, $\overline{\text{MEMCS16}}$, $\overline{\text{XDSEL}}$, and the AT CMDS ($\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$).

Figure 18. Select Code Waveforms

DPU INTERFACE: ATLATCH – AT-TO-EL DATA TRANSFER CYCLE (CPU READ FROM AT BUS, AT-DMA/AT-MASTER WRITE TO EL BUS)

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d58}	Delay time, ATCLK to ATLATCH		6	22	6	20	6	20	ns
t_{d59}	Delay time, AT CMDs† to ATLATCH		6	22	6	20	6	20	ns



† The AT CMDs are $\overline{\text{SMEMR}}$, $\overline{\text{SMEMW}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{IOW}}$, and $\overline{\text{IOR}}$.

Figure 19. ATLATCH Waveform – AT-to-EL Data Transfer Cycle (CPU Read from AT Bus, AT-DMA/AT-Master Write to EL Bus)

DPU INTERFACE: ATLATCH – EL-TO-AT DATA TRANSFER CYCLE (CPU WRITE TO AT BUS, AT-DMA/AT-MASTER READ FROM EL BUS)

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{d18}	Delay time, CLK2IN to ATLATCH	4	20	4	18	4	15	ns

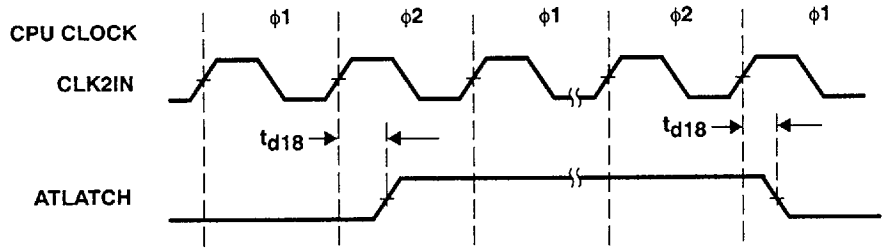


Figure 20. ATLATCH – EL-to-AT Data Transfer Cycle Waveforms (CPU Write to AT Bus, AT-DMA/AT-Master Read from EL Bus)

NUMERIC COPROCESSOR: 387 IDENTIFICATION

T-52-33-05

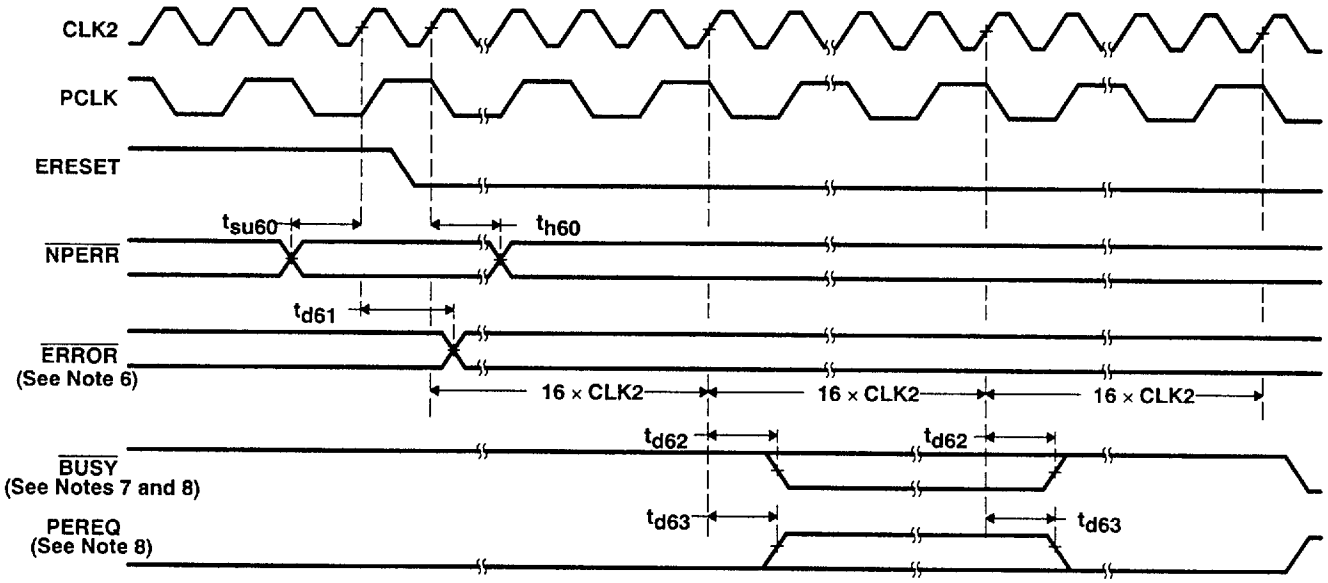
timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su60}	Setup time, $\overline{\text{NPERR}}$ before CLK2↑	7		5		5		ns
t_{h60}	Hold time, $\overline{\text{NPERR}}$ after CLK2↑	5		5		5		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d61}	Delay time, CLK2 to $\overline{\text{ERROR}}$		5	22	5	20	5	18	ns
t_{d62}	Delay time, CLK2 to $\overline{\text{BUSY}}$	See Note 5	5	22	5	20	5	18	ns
t_{d63}	Delay time, CLK2 to PEREQ	See Note 5	5	22	5	20	5	18	ns

NOTE 5: System has no 387. $\overline{\text{BUSY}}$ is driven by the ATU.



NOTES: 6. If there is a 387 installed, $\overline{\text{NPERR}}$ is sampled low at the falling edge of ERESET. In this case, $\overline{\text{ERROR}}$ is held low until $\overline{\text{ADS}}$ is driven low.

7. When CPUSTEN is high, $\overline{\text{BUSY}}$ is held low for 10 CLK2 cycles after ERESET is driven low.

8. If there is no 387 installed, $\overline{\text{NPERR}}$ is sampled high at the falling edge of ERESET. In this case, $\overline{\text{BUSY}}$ and PEREQ toggle every 16 CLK2 cycles.

Figure 21. 387 Identification Waveforms

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su64}	Setup time, $\overline{\text{NPBUSY}}$ before $\overline{\text{NPERR}}$↓	7		5		5		ns
t_{h64}	Hold time, $\overline{\text{NPBUSY}}$ after $\overline{\text{NPERR}}$↓	5		5		5		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d65}	Delay time, $\overline{\text{NPBUSY}}$ to $\overline{\text{BUSY}}$		4	20	4	18	4	15	ns
t_{d66}	Delay time, $\overline{\text{IOW}}$ to $\overline{\text{BUSY}}$	See note	5	25	5	25	5	25	ns
t_{d67}	Delay time, NPPEREQ to PEREQ		4	20	4	18	4	15	ns
t_{d68}	Delay time, $\overline{\text{NPBUSY}}$ to PEREQ		4	20	4	18	3	15	ns
t_{d69}	Delay time, $\overline{\text{IOW}}$ to PEREQ	See note	5	22	5	20	5	18	ns

NOTE: Address on SA19–SA0 = 00F0h or 00F1h.

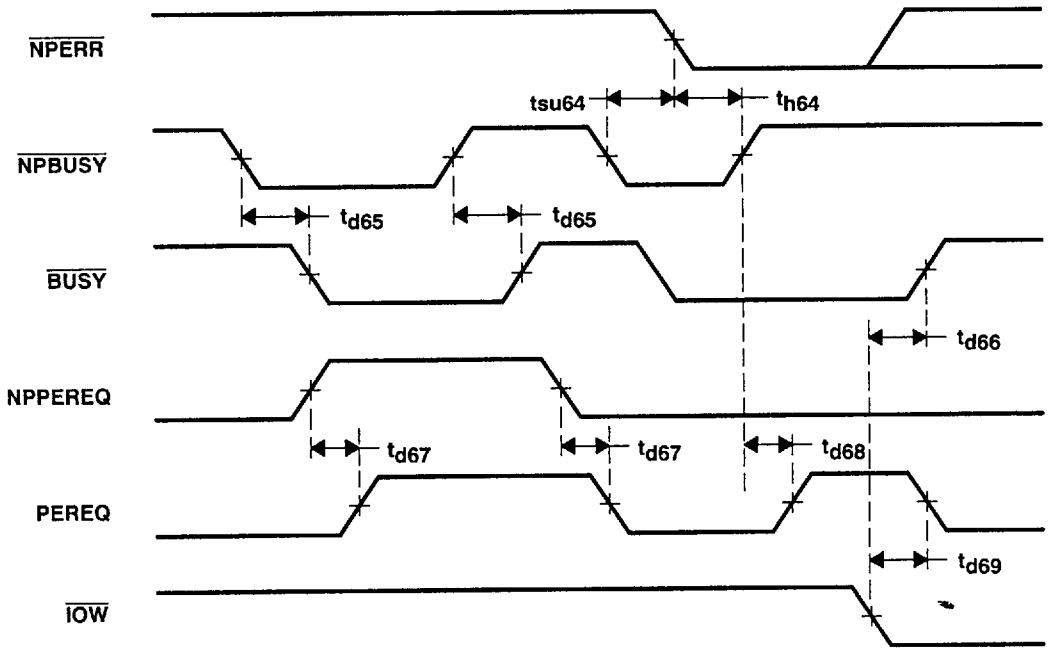


Figure 22. 387 $\overline{\text{BUSY}}$/$\overline{\text{ERROR}}$ Waveforms

NONMASKABLE INTERRUPT (NMI)

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{w70}	Pulse duration, $\overline{IOCHCK}$	10		8		8		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d71}	Delay time, CLK2IN to NMI		5	22	5	20	5	18	ns
t_{d72}	Delay time, $\overline{IOCHCK}$ to NMI		8	40	8	40	8	40	ns
t_{d73}	Delay time, $\overline{IOW}$ to NMI	See note	8	40	8	40	8	40	ns

NOTE: Address on SA19–SA0 = 0061h or 0070h.

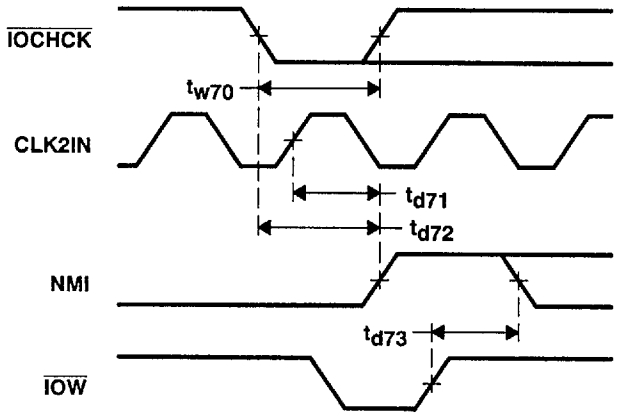


Figure 23. Nonmaskable Interrupt (NMI) Waveforms

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su74}	Setup time, A20GATE before CLK2IN↑	10		8		8		ns
t_{h74}	Hold time, A20GATE after CLK2IN↑	7		5		5		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d75}	Delay time, CLK2IN to A20OUT		4	20	4	18	4	16	ns

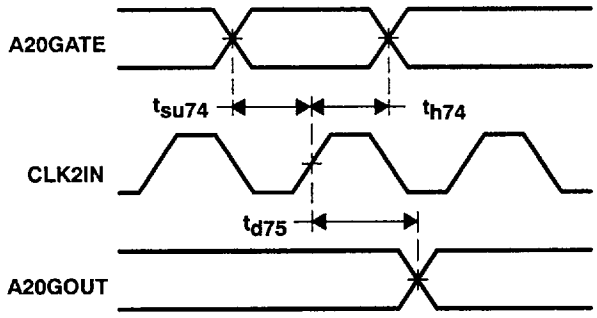


Figure 24. A20GATE/A20GOUT Waveforms

FLUSH

T-52-33-05

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{d76}	Delay time, CLK2IN to FLUSH	4	20	4	18	4	16	ns

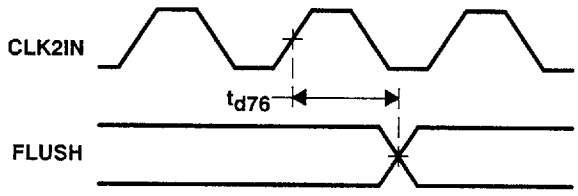


Figure 25. FLUSH Waveforms

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{wL77}	Pulse duration, IRQn and IRQ13X low	30		30		30		ns
t_{wH77}	Pulse duration, IRQn and IRQ13X high	60		60		60		ns
t_{wL78}	Pulse duration, $\overline{\text{NPERR}}$ low	60		60		60		ns
t_{wH78}	Pulse duration, $\overline{\text{NPERR}}$ high	30		30		30		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d79}	Delay time, IRQn to INTR		8	50	8	50	8	50	ns

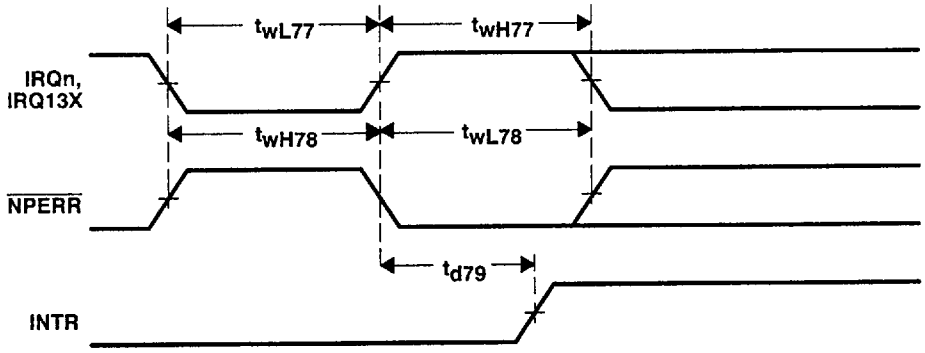


Figure 26. Interrupt Waveforms

OSC_12/SPEAKER

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d80}	Delay time, OSC_1 to OSC_12		5	25	5	25	5	25	ns
t_{d81}	Delay time, OSC_12 to SPEAKER		10	55	10	55	10	55	ns

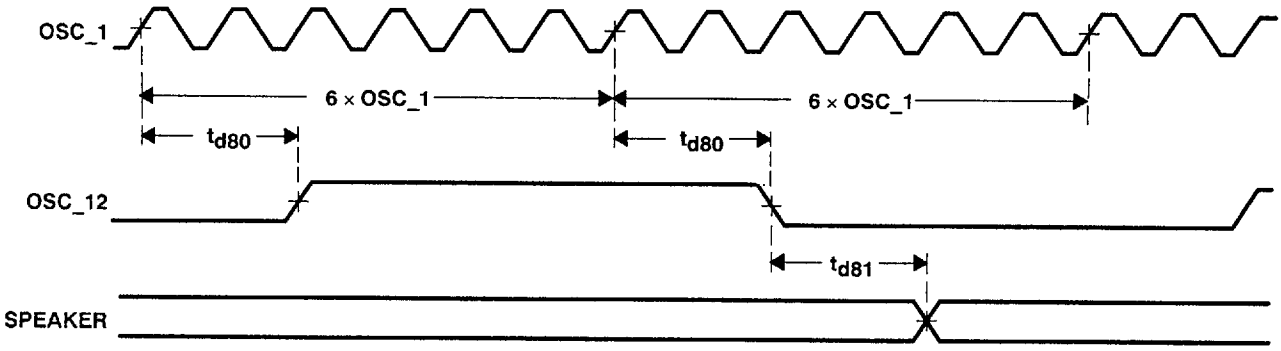


Figure 27. OSC_12/SPEAKER Waveforms

PERIPHERALS: READ/WRITE CYCLE

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su82}	Setup time, SA19–SA0 and AEN before $\overline{IOR}$/$\overline{IOW}$↓	30		30		30		ns
t_{h82}	Hold time, SA19–SA0 and AEN after $\overline{IOR}$/$\overline{IOW}$↓	20		20		20		ns
t_{w83}	Pulse duration, $\overline{IOR}$/$\overline{IOW}$ high or low	120		120		120		ns
t_{su86}	Setup time, XD7–XD0 before $\overline{IOW}$	10		10		10		ns
t_{h86}	Hold time, XD7–XD0 after $\overline{IOW}$	10		10		10		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{a84}	Access time, $\overline{IOR}$ and $\overline{IOW}$ to XD7–XD0		8	100	8	100	8	100	ns
t_{dis85}	Disable time, $\overline{IOR}$ and $\overline{IOW}$ to XD7–XD0		7	35	7	35	7	35	ns
t_{d87}	Delay time, XD7–XD0 to $\overline{KEYBCS}$		4	20	4	20	8	40	ns
t_{d88}	Delay time, SA19–SA0 and AEN to $\overline{KEYBCS}$		8	40	8	40	8	40	ns
t_{d89}	Delay time, SA19–SA0 and AEN to $\overline{PCS1}$–$\overline{PCS3}$		8	40	8	40	8	40	ns

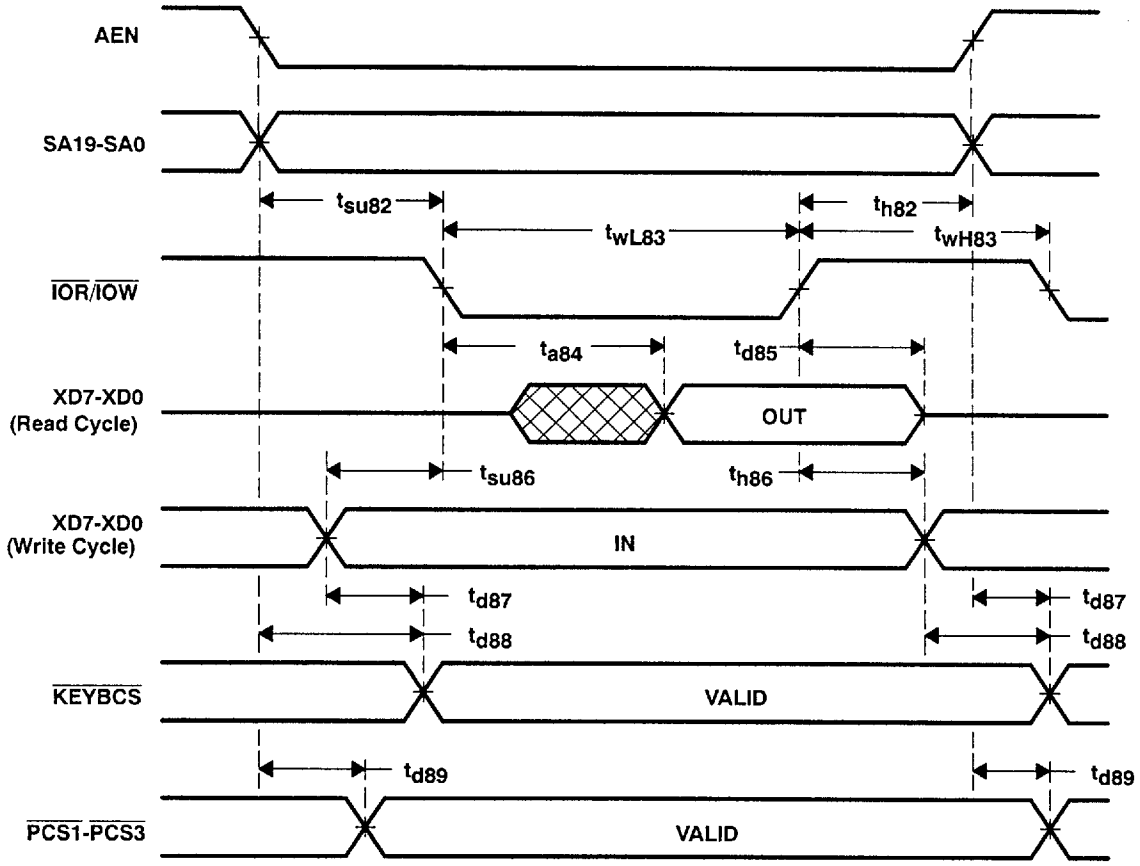


Figure 28. Peripheral Read/Write Cycle Waveforms

WRITE CYCLE: CPU/CACHE CONTROLLER HOST

timing requirements, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C

		MIN	MAX	UNIT
t_{su1}	Setup time, D15-D0 before WBCLK↑	5		ns
t_{h1}	Hold time, D15-D0 after WBCLK↑	2		ns
t_{w2}	Pulse duration, WBCLK high or low	10		ns
t_{w7L}	Pulse duration, ATLATCH low	10		ns
t_{su8}	Setup time, D15-D0 before ATLATCH↑	5		ns
t_{h8}	Hold time, D15-D0 after ATLATCH↑	2		ns
t_{su9}	Delay time, WBCLK to ATLATCH	9		ns

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 100 pF (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{en3}	Enable time, ED15-ED0 from $\overline{DOE}$		4	18	ns
t_{dis3}	Disable time, ED15-ED0 from $\overline{DOE}$	C_L = 50 pF	4	18	ns
t_{en4}	Enable time, ED15-ED0 from BT/$\overline{R}$		4	18	ns
t_{dis4}	Disable time, ED15-ED0 from BT/$\overline{R}$	C_L = 50 pF	4	18	ns
t_{d5}	Delay time, WBCLK to ED15-ED0		3	16	ns
t_{d6}	Delay time, D15–D0 to ED15-ED0		3	16	ns
t_{d10}	Delay time, ATLATCH to SD15-SD0		4	15	ns
t_{d11}	Delay time, DPUS3-DPUS1 to SD15-SD0		4	18	ns
t_{d12}	Delay time, WBCLK to SD15-SD0		5	20	ns
t_{d13}	Delay time, D15–D0 to SD15-SD0		5	20	ns
t_{d14}	Delay time, ATLATCH to XD7-XD0		4	15	ns
t_{d15}	Delay time, DPUS3-DPUS1 to XD7-XD0		4	18	ns
t_{d16}	Delay time, WBCLK to XD7-XD0		5	20	ns
t_{d17}	Delay time, D15–D0 to XD7-XD0		5	20	ns

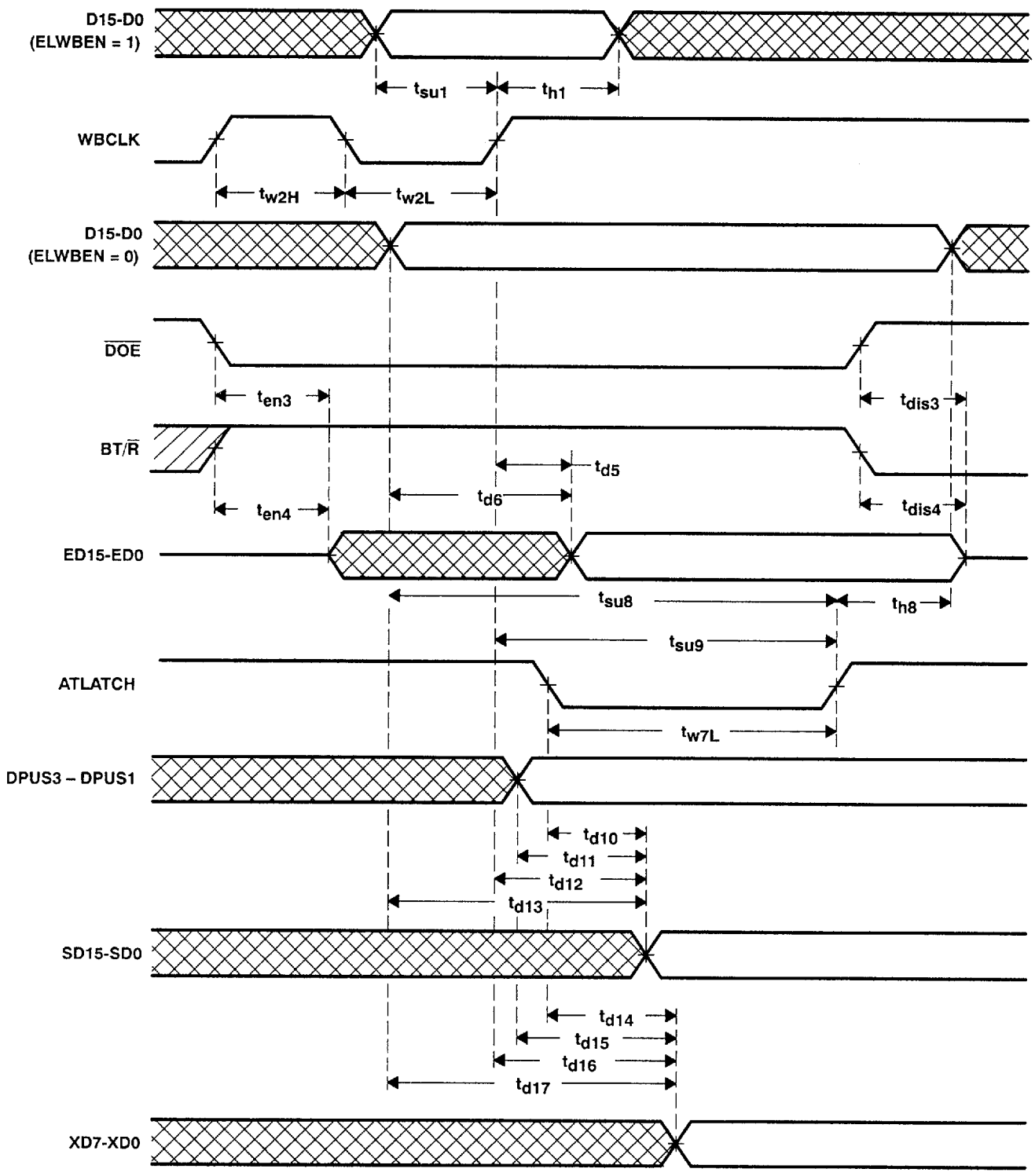


Figure 29. Write Cycle Waveforms – CPU/Cache Controller Host

READ CYCLE: CPU/CACHE CONTROLLER HOST

timing requirements, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C

		MIN	MAX	UNIT
t_{su24}	Setup time, DPUS3–DPUS1 before ATLATCH↑	10		ns
t_{h24}	Hold time, DPUS3-DPUS1 after ATLATCH↑	5		ns
t_{su26}	Setup time, SD15-SD0 before ATLATCH↑	7		ns
t_{h26}	Hold time, SD15-SD0 after ATLATCH↑	2		ns
t_{su28}	Setup time, XD7-XD0 before ATLATCH↑	6		ns
t_{h28}	Hold time, XD7-XD0 after ATLATCH↑	2		ns

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 50 pF

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{en18}	Enable time, D15-D0 from $\overline{DOE}$		4	16	ns
t_{dis18}	Disable time, D15-D0 from $\overline{DOE}$		4	16	ns
t_{en19}	Enable time, D15-D0 from BT/$\overline{R}$		4	16	ns
t_{dis19}	Disable time, D15-D0 from BT/$\overline{R}$		4	16	ns
t_{d20}	Delay time, ED15-ED0 to D15–D0		4	13	ns
t_{d21}	Delay time, SATB to D15-D0		4	13	ns
t_{d22}	Delay time, ATLATCH to D15-D0		4	13	ns
t_{d23}	Delay time, DPUS3–DPUS1 to D15-D0		8	25	ns
t_{d25}	Delay time, SD15–SD0 to D15-D0		6	20	ns
t_{d27}	Delay time, XD7–XD0 to D15-D0		6	20	ns

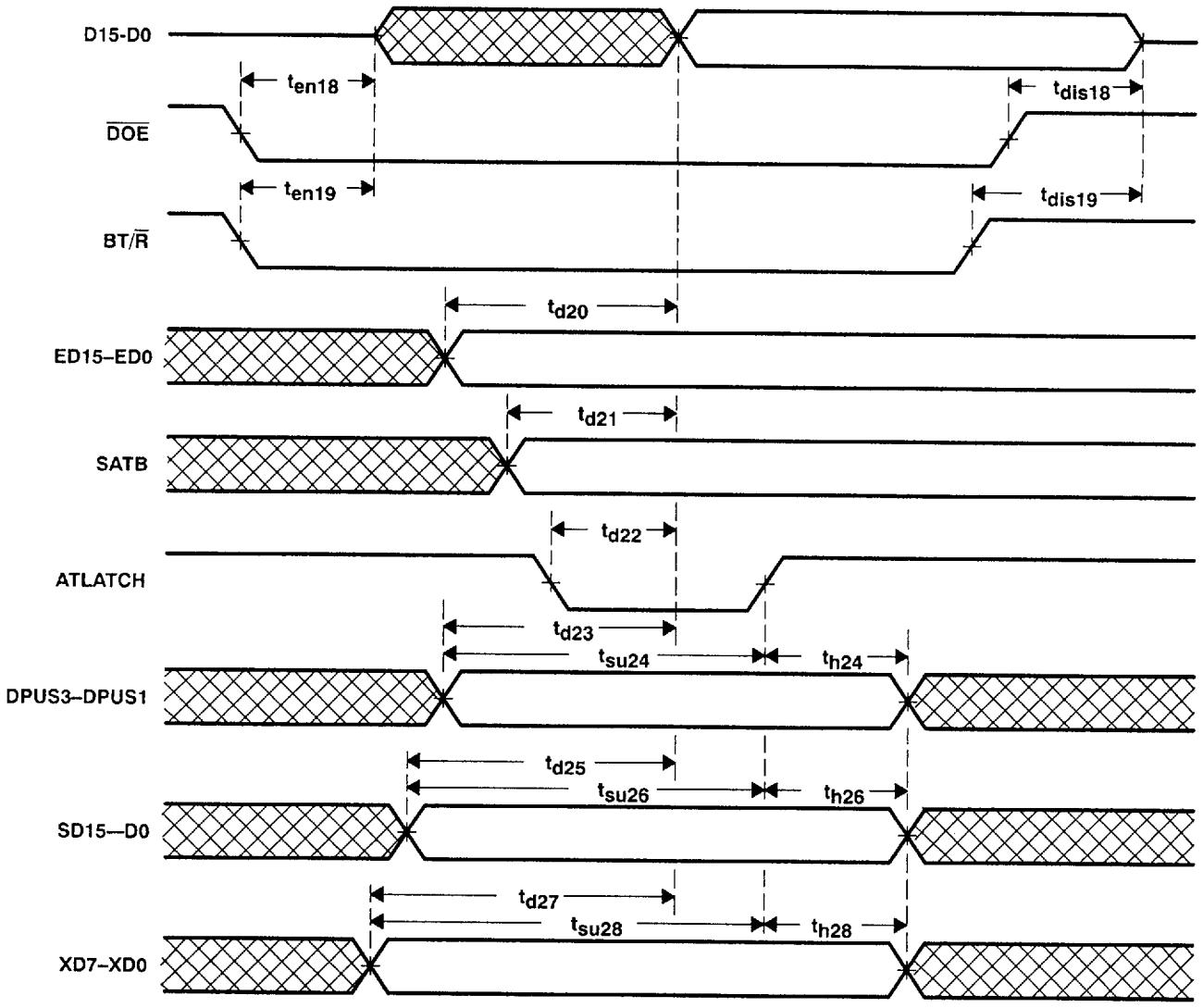


Figure 30. Read Cycle Waveforms – CPU/Cache Controller Host

EL-TO-EL OR EL-TO-AT DATA TRANSFER: DMA CONTROLLER/EL MASTER HOST ($\overline{DOE}$ HIGH, BT/$\overline{R}$ IRRELEVANT, SATB LOW)

timing requirements, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C

		MIN	MAX	UNIT
t_{su29}	Setup time, ED15-ED0 before ATLATCH↑	6		ns
t_{h29}	Hold time, ED15-ED0 after ATLATCH↑	2		ns

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 100 pF

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d30}	Delay time, ED15-ED0 to SD15–SD0		6	22	ns
t_{d10}	Delay time, ATLATCH to SD15-SD0		4	15	ns
t_{d11}	Delay time, DPUS3–DPUS1 to SD15-SD0		4	18	ns
t_{d31}	Delay time, ED15–ED0 to XD7-XD0		6	22	ns
t_{d14}	Delay time, ATLATCH to XD7-XD0		4	15	ns
t_{d15}	Delay time, DPUS1–DPUS3 to XD7-XD0		4	18	ns

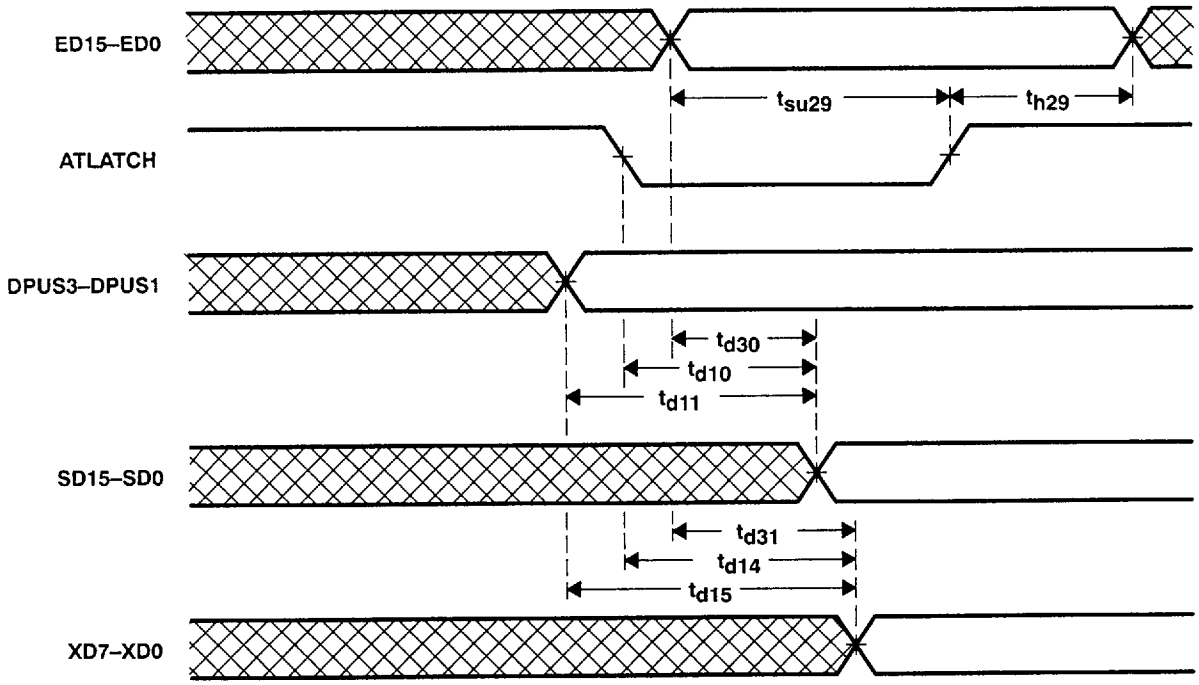


Figure 31. EL-to-EL or EL-to-AT Data Transfer Waveforms: DMA Controller/EL Master Host ($\overline{DOE}$ High, BT/$\overline{R}$ Irrelevant, SATB Low)

AT-TO-EL DATA TRANSFER: DMA CONTROLLER/AT MASTER HOST ($\overline{DOE}$ HIGH, BT/$\overline{R}$ IRRELEVANT)

timing requirements, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C

		MIN	MAX	UNIT
t_{su24}	Setup time, DPUS3-DPUS1 before ATLATCH↑	10		ns
t_{h24}	Hold time, DPUS3-DPUS1 after ATLATCH↑	5		ns
t_{su26}	Setup time, SD15-SD0 before ATLATCH↑	7		ns
t_{h26}	Hold time, SD15-SD0 after ATLATCH↑	2		ns
t_{su28}	Setup time, XD7-XD0 before ATLATCH↑	6		ns
t_{h28}	Hold time, XD7-XD0 after ATLATCH↑	2		ns

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 100 pF

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{en32}	Enable time, ED15-ED0 from SATB		4	15	ns
t_{dis32}	Disable time, ED15-ED0 from SATB		4	15	ns
t_{d33}	Delay time, ATLATCH to ED15-ED0		4	15	ns
t_{d34}	Delay time, DPUS3–DPUS1 to ED15-ED0		8	25	ns
t_{d35}	Delay time, SD15–SD0 to ED15-ED0		6	20	ns
t_{d36}	Delay time, XD7–XD0 to ED7-ED0		6	20	ns

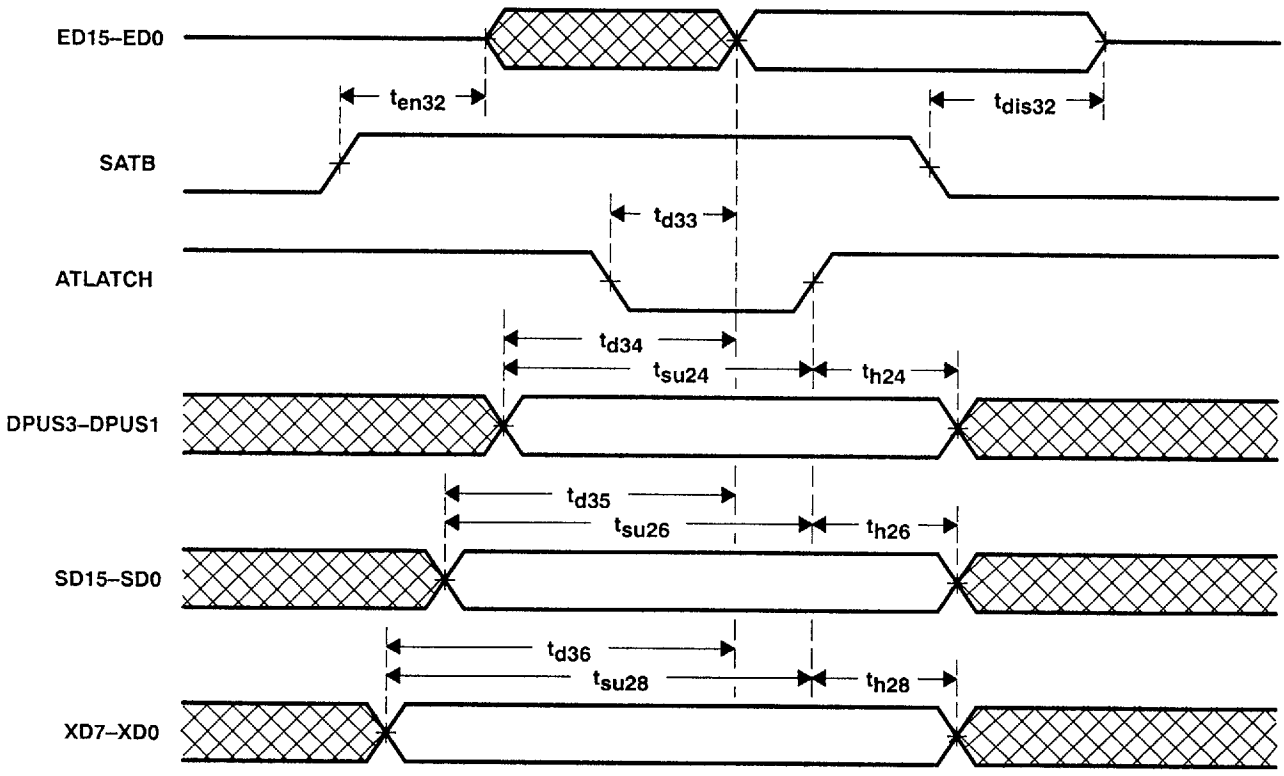


Figure 32. AT-to-EL Data Transfer: DMA Controller/EL Master Host ($\overline{DOE}$ High, BT/$\overline{R}$ Irrelevant)

PARITY GENERATION

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{en37}	Enable time, MDPH, MDPL from LW/$\overline{R}$		5	18	ns
t_{dis37}	Disable time, MDPH, MDPL from LW/$\overline{R}$	C_L = 50 pF	5	18	ns
t_{d38}	Delay time, WBCLK to MDPH, MDPL		4	15	ns
t_{d39}	Delay time, D15-D0 to MDPH, MDPL		4	18	ns
t_{d40}	Delay time, ED15-ED0 to MDPH, MDPL		4	18	ns
t_{d41}	Delay time, ATLATCH to MDPH, MDPL		4	15	ns
t_{d42}	Delay time, DPUS3-DPUS1 to MDPH, MDPL		8	25	ns
t_{d43}	Delay time, SD15–SD0 to MDPH, MDPL		6	22	ns
t_{d44}	Delay time, XD7–XD0 to MDPH, MDPL		6	22	ns

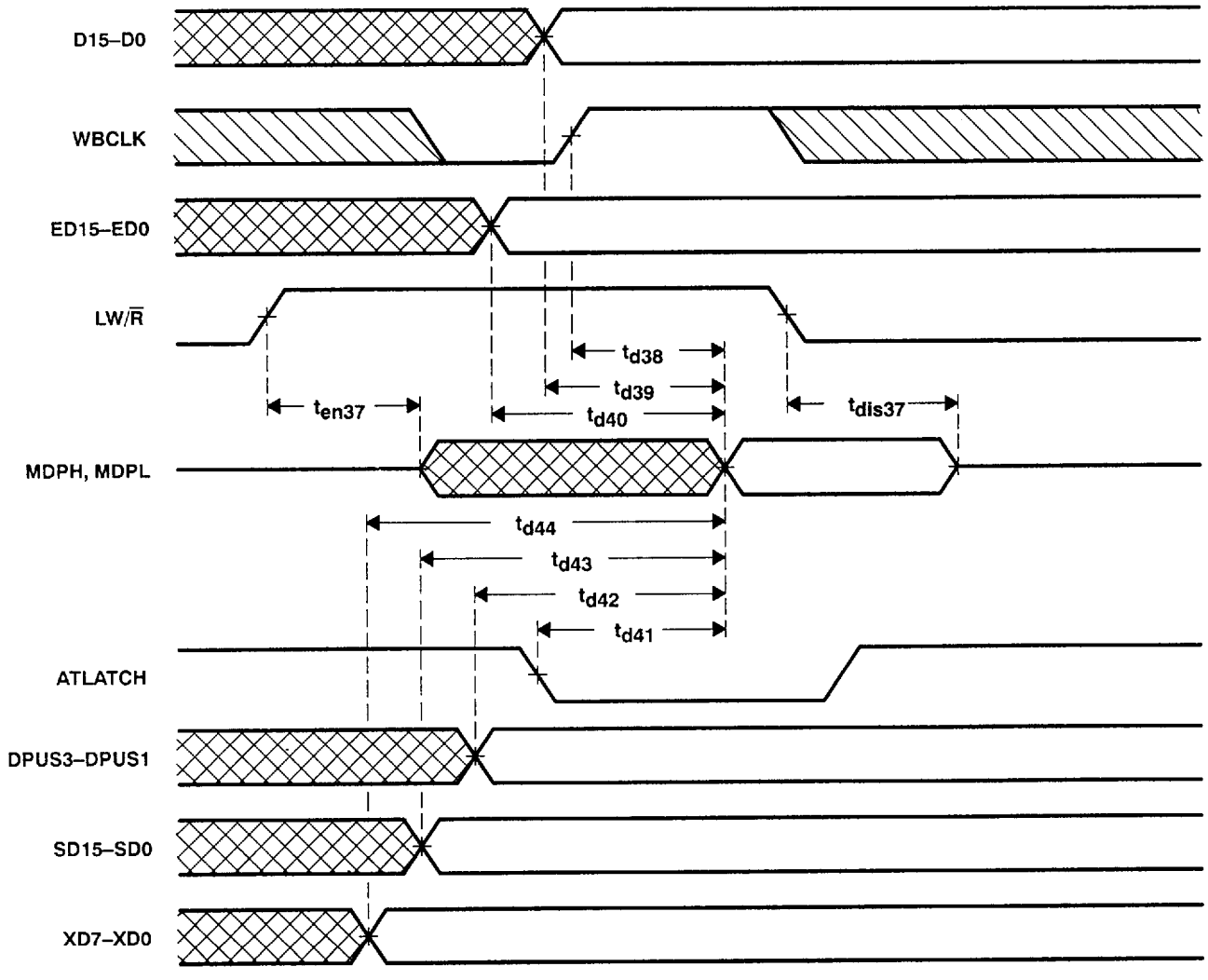


Figure 33. Parity Generation Waveforms

PARITY CHECK

timing requirements, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETERS					MIN	MAX	UNIT
t_{w45}	Pulse duration, CLK2 high or low	V_{CC} = 5 V ±10%,	f = 20 MHz,	$V_{ref} = V_{CC/2}$†	8		ns
		V_{CC} = 5 V ±5%,	f = 25 MHz,	$V_{ref} = V_{CC/2}$†	6		
		V_{CC} = 5 V ±5%,	f = 33 MHz,	$V_{ref} = V_{CC/2}$†	6		
t_{c45}	Cycle time, CLK2	V_{CC} = 5 V ±10%,	f = 20 MHz		25		ns
		V_{CC} = 5 V ±5%,	f = 25 MHz		15		
		V_{CC} = 5 V ±5%,	f = 33 MHz		15		
t_{su46}	Setup time, ED15–ED0 before CLK2↑				4		ns
t_{h46}	Hold time, ED15–ED0 after CLK2↑				2		ns
t_{su47}	Setup time, MDPH, MDPL before CLK2↑				4		ns
t_{h47}	Hold time, MDPH, MDPL after CLK2↑				2		ns
t_{su48}	Setup time, $\overline{READY}$ before CLK2↑				5		ns
t_{h48}	Hold time, $\overline{READY}$ after CLK2↑				2		ns
t_{su49}	Setup time, LW/$\overline{R}$ before CLK2↑				3		ns
t_{h49}	Hold time, LW/$\overline{R}$ after CLK2↑				2		ns

† V_{ref} is the reference voltage with respect to which the time intervals are defined.

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 50 pF

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d50}	Delay time, CLK2 to MPCKH, MPCKL		3	12	ns

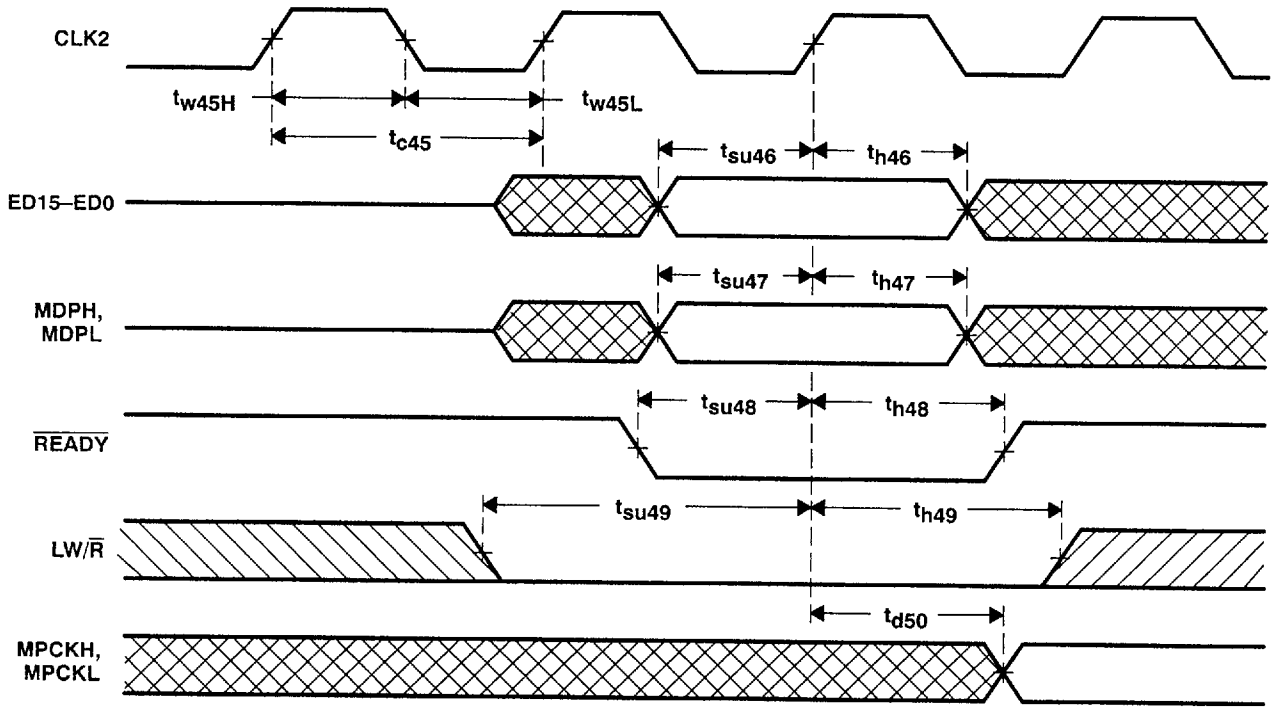
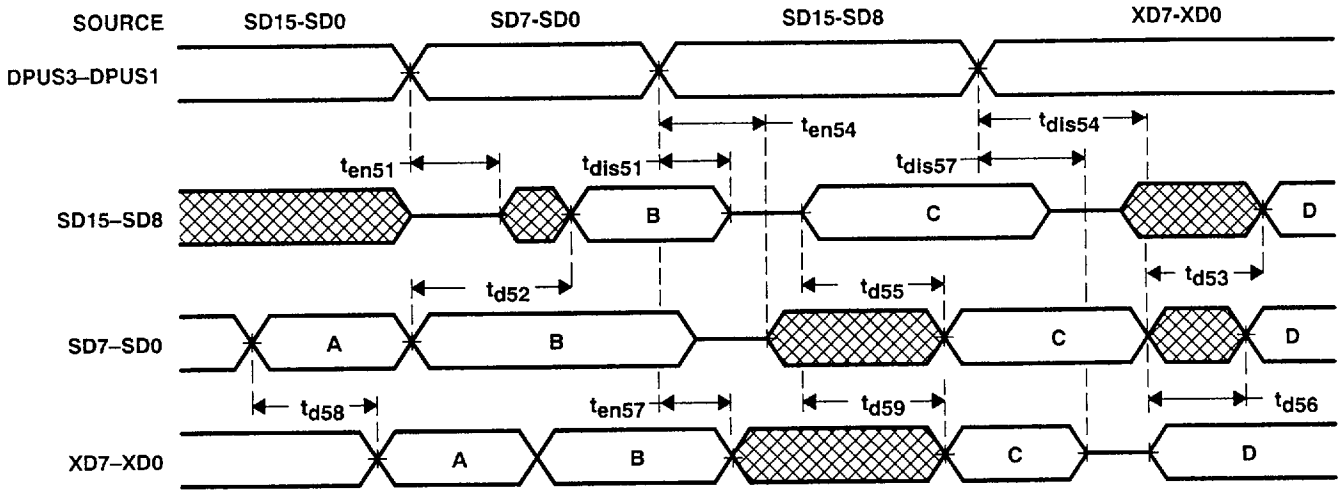


Figure 34. Parity Check Waveforms

SD OR XD DATA TRANSFERS

switching characteristics, V_{CC} = 5 V ±10%, T_A = 0°C to 70°C, and C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{en51}	Enable time, SD15-SD8 from DPUS3-DPUS1		4	18	ns
t_{dis51}	Disable time, SD15-SD8 from DPUS3-DPUS1	C_L = 50 pF	4	18	ns
t_{d52}	Delay time, SD7-SD0 to SD15-SD8		4	18	ns
t_{d53}	Delay time, XD7-XD0 to SD15-SD8		4	18	ns
t_{en54}	Enable time, SD7-SD0 from DPUS3-DPUS1		4	18	ns
t_{dis54}	Disable time, SD7-SD0 from DPUS3-DPUS1	C_L = 50 pF	4	18	ns
t_{d55}	Delay time, SD15-SD8 to SD7-SD0		4	18	ns
t_{d56}	Delay time, XD7-XD0 to SD7-SD0		4	18	ns
t_{en57}	Enable time, XD7-XD0 from DPUS3-DPUS1		4	18	ns
t_{dis57}	Disable time, XD7-XD0 from DPUS3-DPUS1	C_L = 50 pF	4	18	ns
t_{d58}	Delay time, SD7-SD0 to XD7-XD0		4	18	ns
t_{d59}	Delay time, SD15-SD8 to XD7-XD0		4	18	ns



NOTE: A, B, C, and D represent specific bytes being transferred

Figure 35. SD or XD Data Transfer Waveforms

CLK2/ERESET

timing requirements, T_A = 0°C to 70°C

		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{c1}	Cycle time, CLK2		25		20		15		ns
t_{w1}	Pulse duration, CLK2 high or low	$V_{ref} = V_{CC}/2$	9		7		6		ns
t_{su2}	Setup time, ERESET before CLK2↑		9		7		6		ns
t_{h2}	Hold time, ERESET after CLK2↑		4		3		3		ns

† V_{ref} is the reference voltage with respect to which the time intervals are defined.

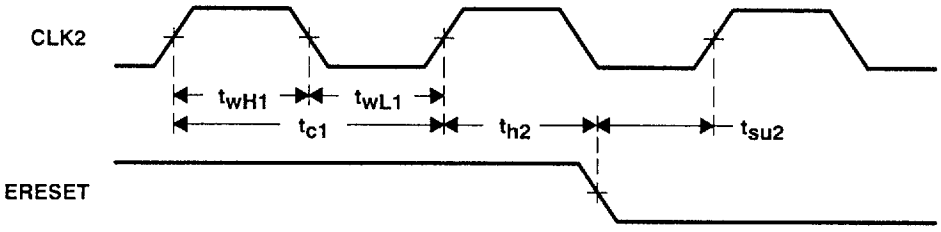


Figure 36. CLK2/ERESET Waveforms

EL BUS INTERFACE

timing requirements, T_A = 0°C to 70°C

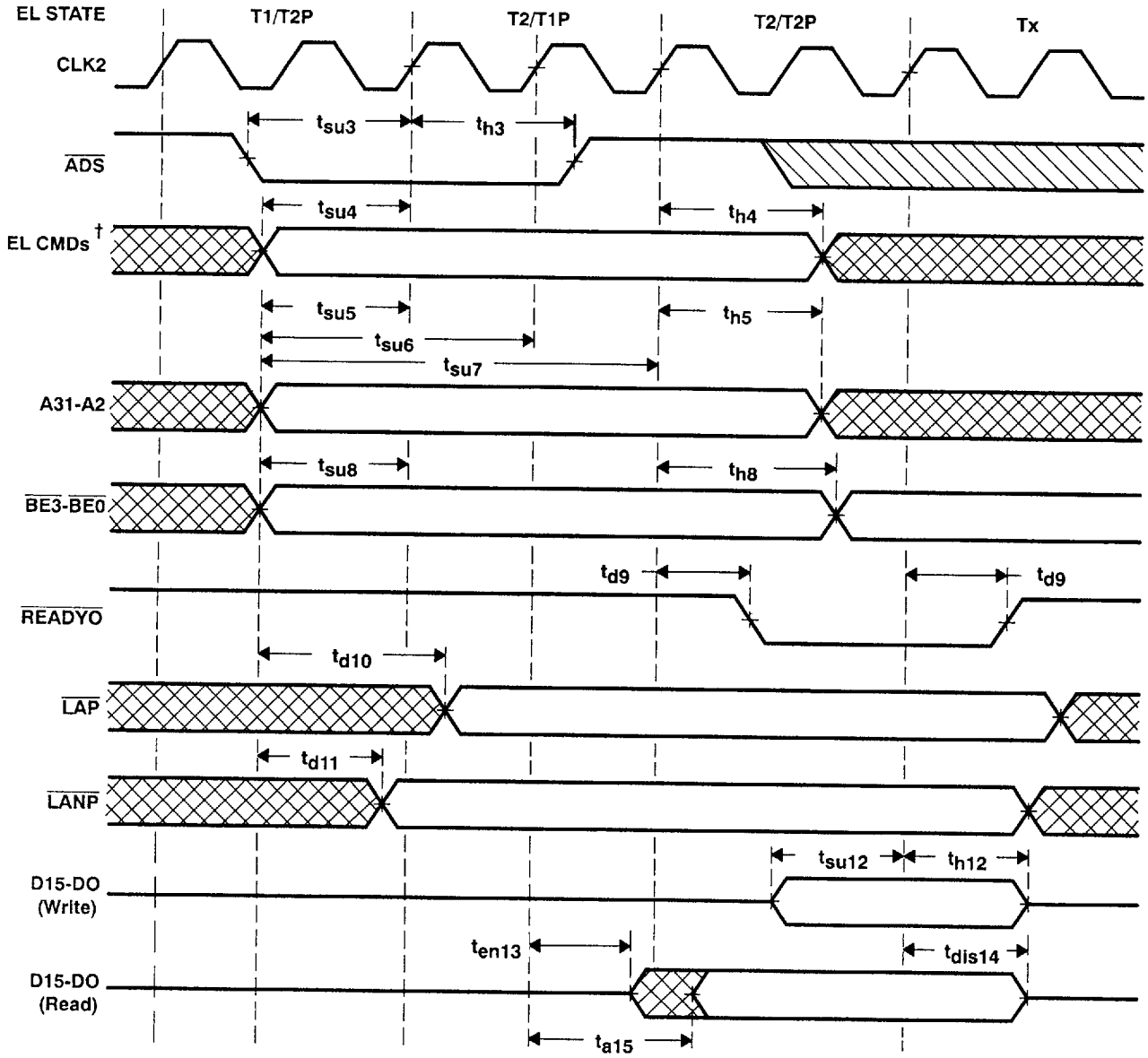
		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su3}	Setup time, $\overline{ADS}$ before CLK2↑	14		11		8		ns
t_{h3}	Hold time, $\overline{ADS}$ after CLK2↑	4		3		3		ns
t_{su4}	Setup time, EL CMDs† before CLK2↑	14		11		8		ns
t_{h4}	Hold time, EL CMDs† after CLK2↑	3		3		3		ns
t_{su5}	Setup time, A2–A31 (including gated A20) before CLK2↑	16		12		8		ns
t_{h5}	Hold time, A2–A31 (including gated A20) after CLK2↑	3		3		3		ns
t_{su6}	Setup time, A2–A31 (including gated A20) before CLK2↑ (See Note 9)	35		32		30		ns
t_{su7}	Setup time, A2–A31 (including gated A20) before CLK2↑ (See Note 10)	35		32		30		ns
t_{su8}	Setup time, $\overline{BE3}$–$\overline{BE0}$ before CLK2↑	16		14		11		ns
t_{h8}	Hold time, $\overline{BE3}$–$\overline{BE0}$ after CLK2↑	4		3		3		ns
t_{su12}	Setup time, D15–D0 before CLK2↑	5		5		5		ns
t_{h12}	Hold time, D15–D0 after CLK2↑	6		6		6		ns

† The EL CMDs consist of W/$\overline{R}$, M/$\overline{IO}$, and D/$\overline{C}$.

NOTES: 9. $\overline{RAS}$/$\overline{CAS}$ active point is at the center of T2/T1P (RCAP bit of DRAM control register = 0).
10. $\overline{RAS}$/$\overline{CAS}$ active point is at the end of T2/T1P (RCAP bit of DRAM control register = 1).

switching characteristics, T_A = 0°C to 70°C, C_L = 15 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d9}	Delay time, CLK2 to $\overline{READYO}$		5	16	5	13	5	12	ns
t_{d10}	Delay time, A2–A31, M/$\overline{IO}$, and D/$\overline{C}$ to $\overline{LAP}$		5	35	5	32	5	29	ns
t_{d11}	Delay time, A2–A31, M/$\overline{IO}$, and D/$\overline{C}$ to $\overline{LANP}$		5	24	5	21	5	19	ns
t_{en13}	Enable time, CLK2 to D15–D0	C_L = 100 pF	4	25	4	20	4	20	ns
t_{dis14}	Disable time, CLK2 to D15–D0	C_L = 0	4	25	4	20	4	20	ns
t_{a15}	Access time, CLK2 to D15–D0	C_L = 100 pF		60		50		50	ns



NOTE: The EL bus cycle states are as follows: Ti = idle, T1 = first state of cycle, T2 = second state of cycle, T1P = first state of cycle in pipelined mode, T2P = subsequent state of cycle in pipelined mode, Tx = any state.
† The EL CMDs consist of W/$\overline{R}$, M/$\overline{IO}$, and D/$\overline{C}$.

Figure 37. EL Bus Interface Waveforms

EL BUS INTERFACE – $\overline{\text{READY}}$

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su16}	Setup time, $\overline{\text{READY}}$ before CLK2↑	16		13		10		ns
t_{h16}	Hold time, $\overline{\text{READY}}$ after CLK2↑	4		3		3		ns

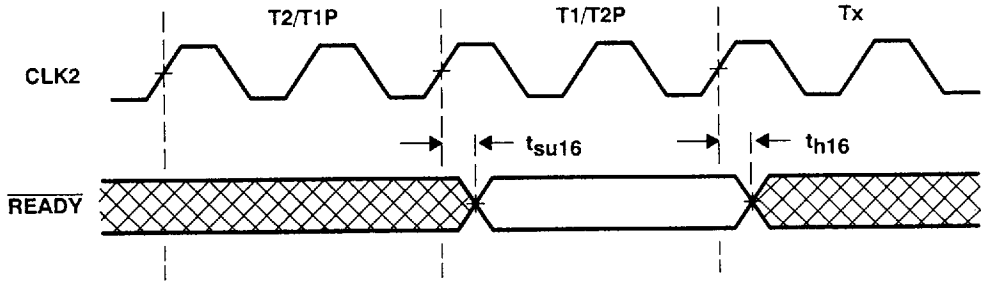
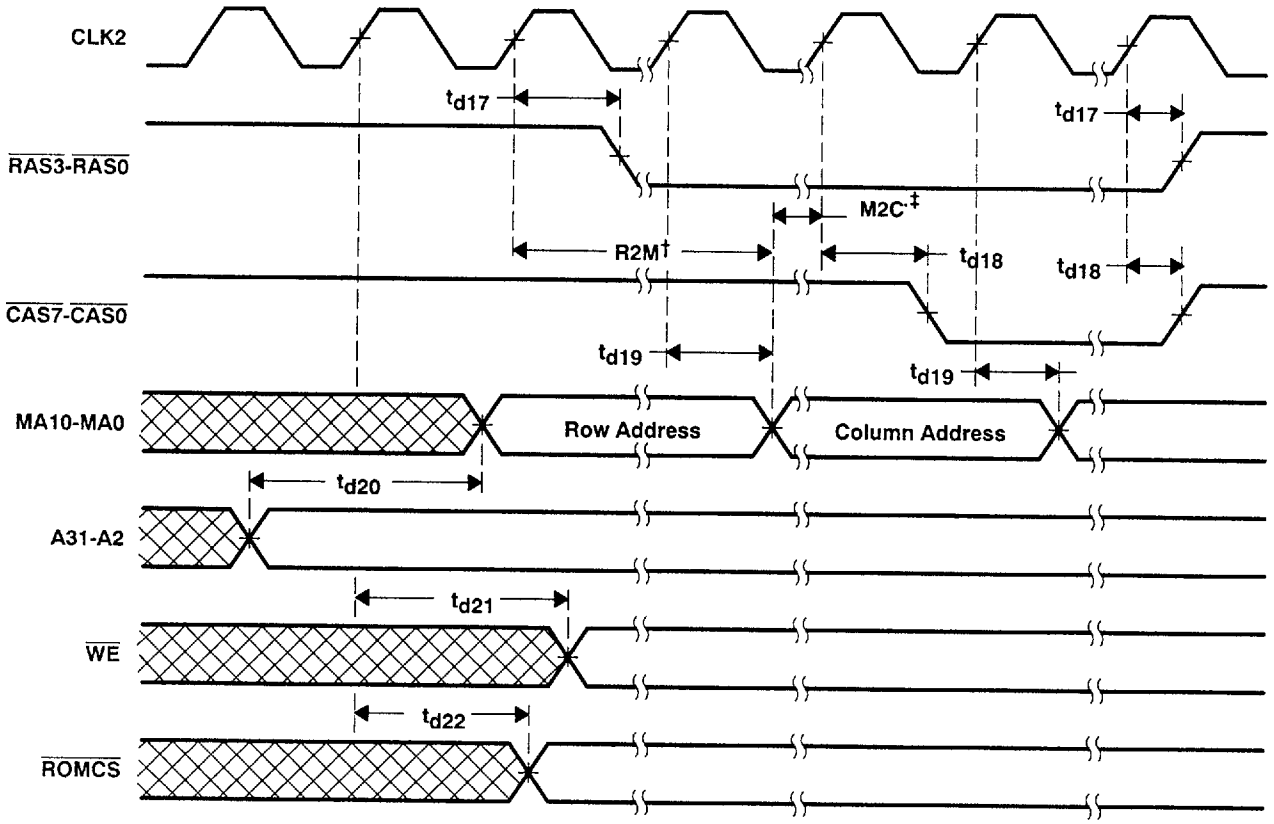


Figure 38. EL Bus Interface Waveforms – $\overline{\text{READY}}$

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d17}	Delay time, CLK2 to $\overline{RAS3}$–$\overline{RAS0}$	C_L = 150 pF	4	25	4	22	4	22	ns
t_{d18}	Delay time, CLK2 to $\overline{CAS7}$–$\overline{CAS0}$	C_L = 75 pF	4	20	4	18	4	18	ns
t_{d19}	Delay time, CLK2 to MA10–MA0	C_L = 250 pF	5	30	5	26	5	24	ns
t_{d20}	Delay time, A31–A2 to MA10–MA0	C_L = 250 pF	5	39	5	35	5	32	ns
t_{d21}	Delay time, CLK2 to $\overline{WE}$	C_L = 250 pF	5	30	5	26	5	24	ns
t_{d22}	Delay time, CLK2 to $\overline{ROMCS}$		4	22	4	20	4	20	ns



† R2M = MA10–MA0 hold time from $\overline{RASn}$. One to two CLK2 cycles as defined by MCU DRAM timing registers.
‡ M2C = $\overline{CASn}$ hold time from MA10–MA0. One to two CLK2 cycles as defined by MCU DRAM timing registers.

Figure 39. Memory Interface Waveforms

CASCADE

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su23}	Setup time, CIN before CLK2↑	2		2		2		ns
t_{h23}	Hold time, CIN after CLK2↑	3		3		3		ns

switching characteristics, T_A = 0°C to 70°C, C_L = 50 pF

PARAMETER		TEST CONDITIONS	f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
			V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{d24}	Delay time, CLK2 to COUT		4	24	4	21	4	19	ns

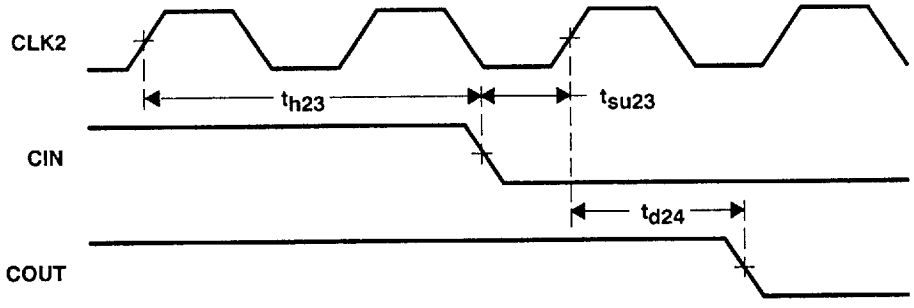


Figure 40. Cascade Waveforms

REFRESH HOLD

timing requirements, T_A = 0°C to 70°C

		f = 20 MHz		f = 25 MHz		f = 33 MHz		UNIT
		V_{CC} = 5 V ± 10%		V_{CC} = 5 V ± 5%		V_{CC} = 5 V ± 5%		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su25}	Setup time, REFHLD before CLK2↑	10		10		10		ns
t_{h25}	Hold time, REFHLD after CLK2↑	3		3		3		ns

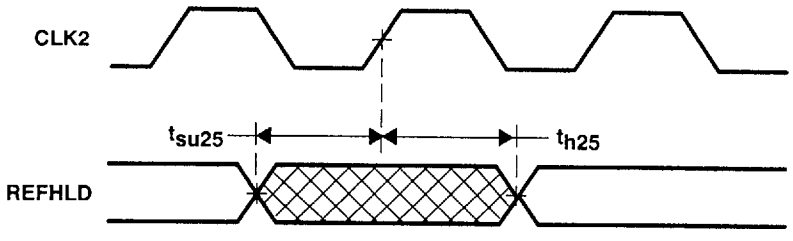
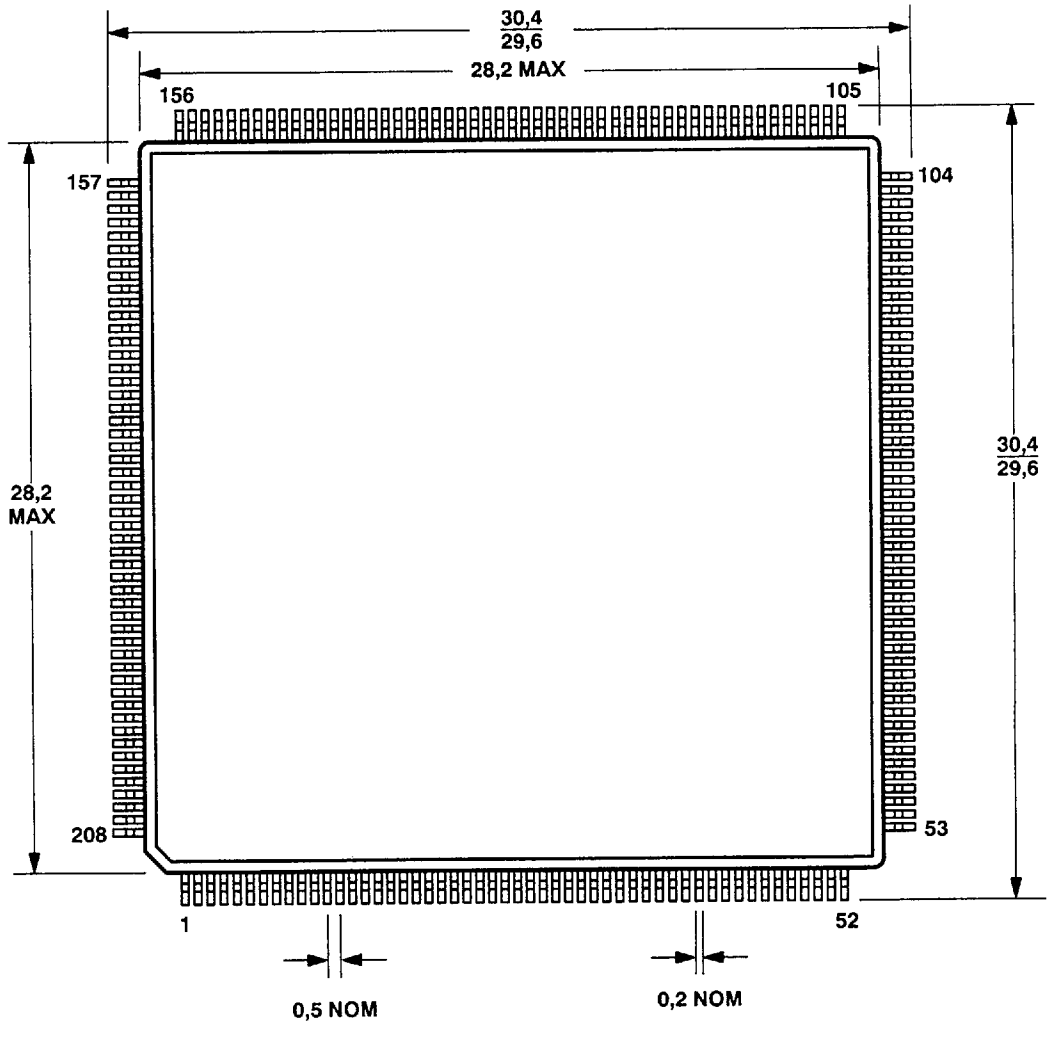
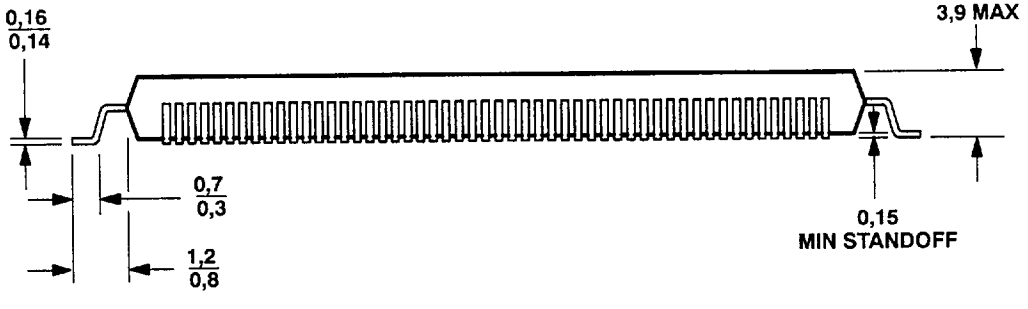


Figure 41. Refresh Hold Waveforms

MECHANICAL DATA

208-Lead Quad Flatpack (ATU)



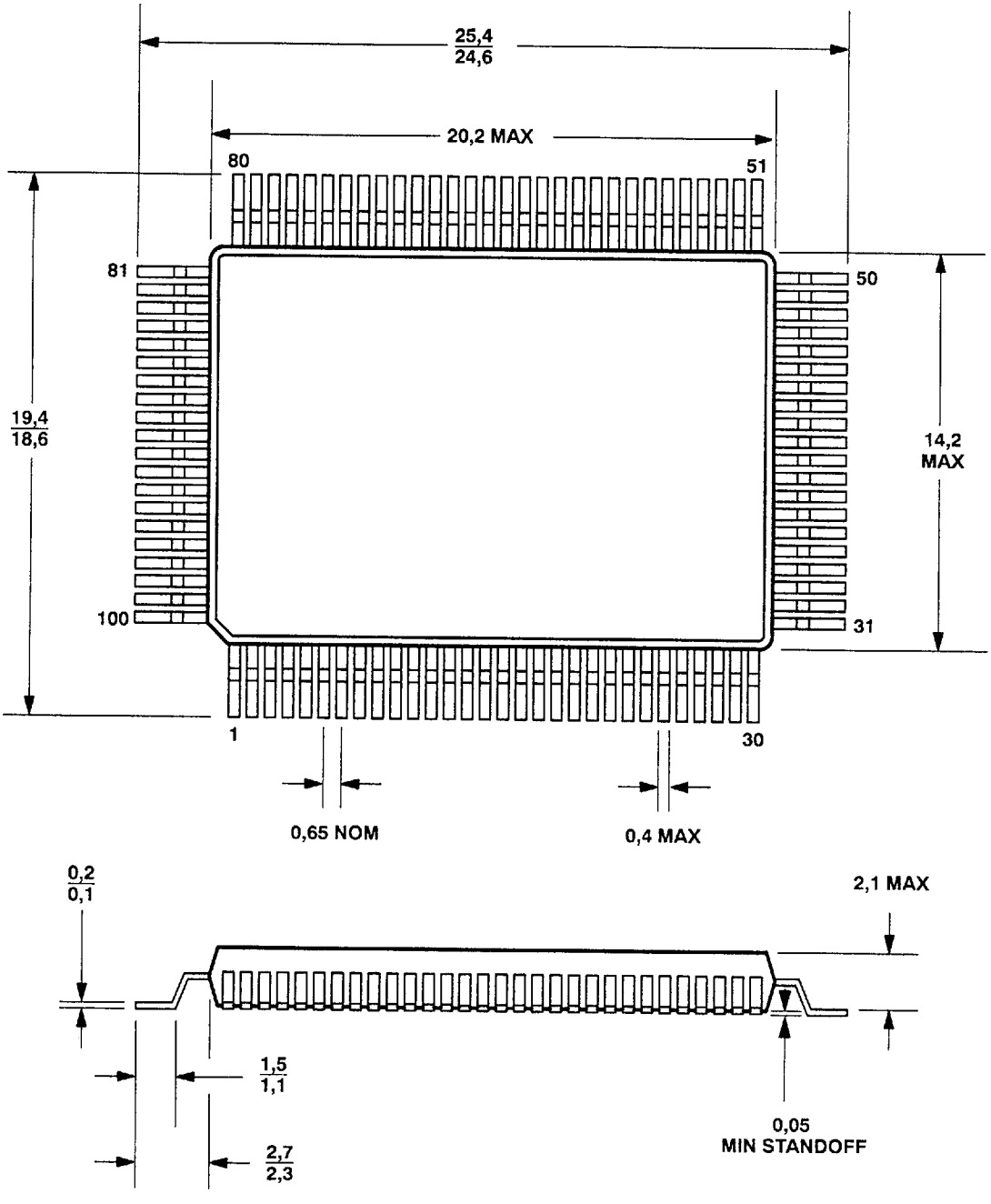


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

MECHANICAL DATA

T-52-33-05

100-Lead Quad Flatpack (DPU and MCU)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS