Texas Instruments TACT82411 AT Chip Preview Bulletin

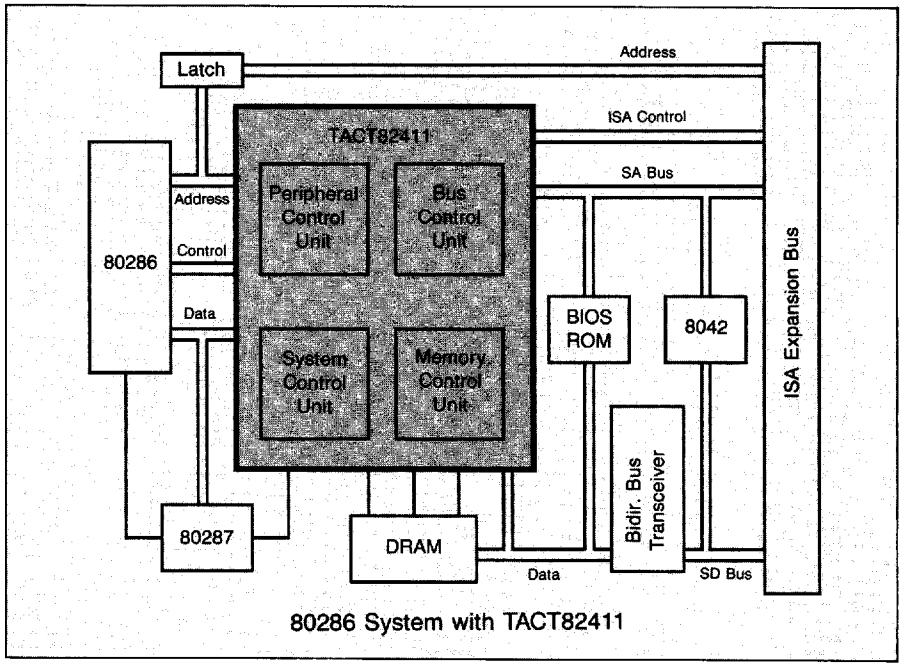
T-52-33-05

OVERVIEW

The new Texas Instruments single-chip TACT82411 contains the system logic and most of the peripheral functions needed to build a 12-20 MHz 80286-based computer that is 100% compatible with the IBM® PC-AT™. Only seven logic components plus memory, CPU, and coprocessor are required to complete an 80286 system board. The chip also supports system boards which use the 80386SX. The TACT82411 is packaged in a 208-pin quad flat pack (QFP).

Because the TACT82411 is manufactured with TI's 1-micron EPIC™ CMOS technology, it provides a high level of integration and high-speed state-of-the-art performance at relatively low power consumption. This combination permits systems that are smaller, lighter, and more sophisticated, but with lower power consumption—an ideal combination for portable, battery-powered systems such as laptop computers. Another benefit of high-integration is increased reliability due to fewer board connections. In addition, product cost is reduced because new system design and testing are simplified.

Redesign of existing multi-chip or discrete 80286 system boards is easy and cost-effective because of the straightforward and flexible structure of the TACT82411 chip. System boards which were originally designed to operate at 12/16 MHz can be easily upgraded to operate at 20 MHz. Non-PC applications using the 80286, such as instrument control, automobiles, and medical equipment, can also benefit by using the TACT82411 chip. Architectural variations can be easily implemented for special- purpose systems such as LAN-based diskless workstations and PC-based portable test equipment.



80286 System with TACT82411

FEATURES	BENEFITS
□ Separate CPU and AT bus clocks for asynchronous AT bus operation	□ Provides AT compatibility
□ Software configuration for wait states, command delays, and memory organization	□ Ensures add-on card compatibility
□ Real-time clock and 128-byte CMOS configuration RAM	□ Reduces chip count
□ Single-bank page mode	□ Activating page mode allows use of slower, less expensive DRAMs
□ 2-way and 4-way page interleave mode with 64K, 256K and 1M DRAMs	□ Enhances flexibility
□ 4M×1 DRAM support	□ Permits up to 32M on-board memory
□ Lotus-Intel-Microsoft Expanded-Memory Specification (LIM-EMS): EMM (Extended Memory Manager) support with four physical pages mapped to 512 logical pages.	□ Complies with industry standards
□ Shadow RAM for BIOS ROM and video ROM	□ Improves system performance
□ Optimized CPU RESET and GATEA20	□ Speeds up operating system

IMPORTANT NOTICE:
This document contains advance information on products in the sampling or pre-production stage.

The primary functional areas of the TACT82411 are:

- Peripheral Control Unit
- Bus Control Unit
- System Control Unit
- Memory Control Unit

PERIPHERAL CONTROL UNIT

DMA Control

The DMA control logic is equivalent to two 8237A DMA controllers in cascade. The first is dedicated to 8-bit transfers and the second is dedicated to 16-bit transfers. The DMA page registers allow DMA operation throughout the 80286's 16-megabyte address range to ensure AT compatibility. The user can program the DMA clock rate, wait states and command delays via one of the peripheral configuration registers.

Interrupt Control

The interrupt control logic is functionally equivalent to two 8259As cascaded through IRQ2 of the master controller. The control and data registers are decoded in system I/O space at addresses that maintain AT compatibility. Four interrupts are dedicated.

Timer

The time base for the 8254-compatible timer is an integral oscillator with an external crystal. Three timer channels have dedicated outputs in the AT system: one each for IRQ0, the refresh clock, and the speaker output.

Real-Time Clock and Configuration RAM

An external oscillator drives the MC146818-compatible real-time clock (RTC). When the main power is turned off, a battery powers the oscillator, the RTC's control and data registers, and the user-controlled configuration RAM.

BUS CONTROL UNIT

System Data Bus Arbitration

Bidirectional control signals allow another bus master to access the main memory. When the DMA controller or another bus master requests control, the arbitration control logic signals the CPU to release the bus, acknowledges the request, and then directs the AT state machine to generate any required control signals.

Data Swapping

The internal data latches and the byte-swapping logic handle transfers between 8-bit and 16-bit buses. Appropriate wait states allow multi-cycle transfers between the different width buses.

Parity Generator and Checker

A parity bit is generated for every byte stored in memory. The parity bit is stored with the byte and is checked when the byte is read.

SYSTEM CONTROL UNIT

Synchronous and Asynchronous Clocks

The user can select either synchronous or asynchronous CPU and AT bus clocks by programming the configuration register. Synchronous operation reduces the number of wait states needed for transactions between the CPU and ISA buses.

CPU System State-Control

The system state-control logic is composed of two closely coupled state machines—one to detect CPU state and generate local-bus cycles when needed, and the other to generate ISA-bus cycles. This logic:

- Interprets the system configuration register contents
- Generates control signals for ISA-bus cycles
- Generates CPU cycles for main memory accesses from the controlling bus master
- Monitors local bus cycles and triggers the non-maskable interrupt signal under certain conditions
- Synchronizes data transfers between CPU and ISA buses when using asynchronous clocks
- Participates in system bus arbitration logic control and system command and interface logic control

Command Delay and Wait State Software Programing

By programming the command delay register, the user can dynamically select how long an ISA-bus cycle will be delayed after the address latch is enabled. This feature permits maximum performance from high-speed expansion boards while maintaining compatibility with slower boards.

The user can program the number of wait states from 0 to 3.

DRAM Access Time (ns)

	12 MHz	16 MHz	20 MHz
Page Mode			
0 Wait State	120	100	80
Normal Mode			
0 Wait State	80	60	—

Reset and Shutdown

There are three separate reset signals. A power supply signal drives the total system reset. A signal from either the keyboard, shutdown logic, or configuration register drives the processor-only reset. A CPU signal drives the coprocessor-only reset.

CPU and I/O Interface

The address latch holds the 24-line address from the CPU for further processing. The address decoder decodes chip-select signals for the internal peripheral devices at industry-standard addresses. It decodes configuration register access addresses at specified addresses. The internal data latches and the byte-swapping logic handle transfers between 8-bit and 16-bit buses. The logic generates wait states to allow multi-cycle transfers between the different width buses.

MEMORY CONTROL UNIT

Page/Interleave

Interleaved page-mode operation permits DRAMs with slower access times to be used at, or near, the highest possible speed of the processor. Combining page-mode operation with two interleaved banks of DRAM increases the chances that a given access will occur without wait states. Increasing the number of DRAM banks to four, while retaining the use of page mode, further reduces the average number of CPU wait states. Different sized DRAMs (64K, 256K, 1M) can be used in separate banks if the interleaved-memory feature is disabled.

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LIM-EMS Support

The TACT82411 chip supports LIM-EMS 4.0 which allows four 16K pages within the MS-DOS® address space to be designated as windows. The bits in the EMS page register and EMS extension register specify where each page is relocated in the expansion area.

Memory Control Configuration

The system configuration registers determine the action of the memory control configuration logic, which in turn, controls timing and DRAM operating modes (device type, interleaving, and page mode).

Fast Reset for Real/Protect Memory Mode Switch

A reset-CPU signal in response to a bit transition in a configuration register provides a quick way for an operating system, such as OS/2, to switch from protected mode to real mode.

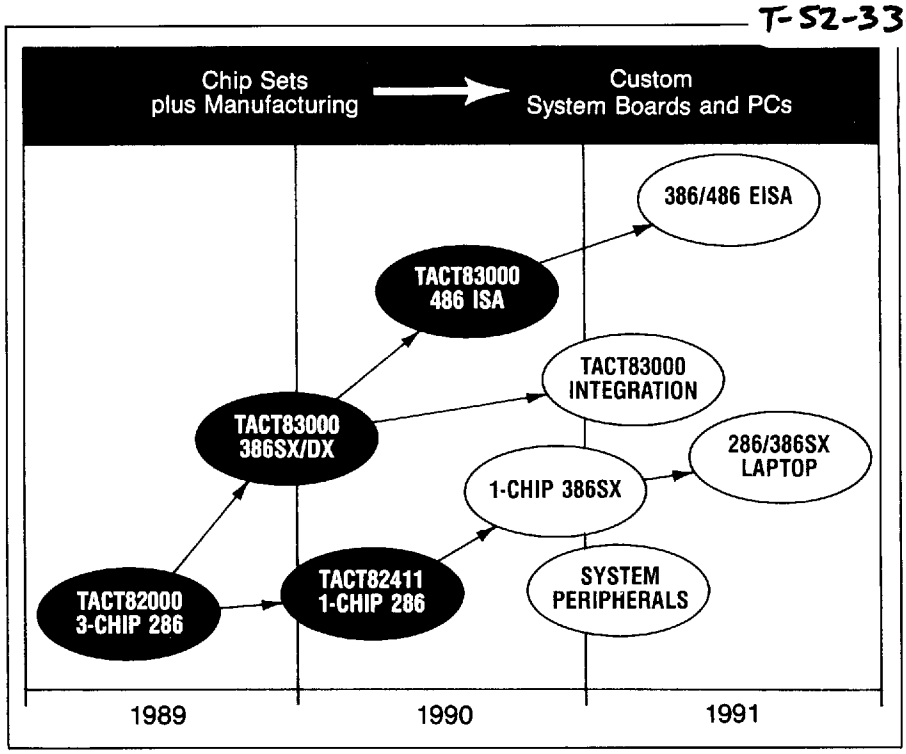
Shadow RAM

Copying the BIOS ROM into the shadow RAM improves system performance when an application makes frequent BIOS calls. The BIOS calls are serviced from this dedicated portion of high-speed RAM instead of the slower BIOS. If the shadow-RAM feature is not enabled in a system that has only 1M of DRAM, the top 384K can be remapped for use as EMS memory, RAM disk, or other purpose.

Memory Address Multiplexer

This logic multiplexes the latched address to generate DRAM row-address and column-address strobes, DRAM memory addresses, DRAM write enable, and BIOS ROM chip select. The multiplexer can be controlled by the memory-mode control, DMA control, refresh counter, or system bus arbitration and control.

The main memory DRAM is organized as one to four banks of 16 data bits plus two parity bits. Each bank has its own row address signal and two (one for each byte) column address signals. The memory data bus, which is common to all banks, is connected to the ISA data bus or SD bus via a bidirectional bus transceiver.



TI's growing family of chip sets is the key to complete PC integration.

THE PC FOR THE 1990s

TI is currently developing its next generation of chip sets, including chips specifically tailored to the size, power, and display constraints of laptop systems.

But TI offers much more for the PC than just AT chip sets. TI's cache memory products and TMS380 token ring LAN products complement the chip sets' core logic. Applications which benefit from high resolution could use a TMS340 graphics processor and the Texas Instruments Graphics Architecture (TIGA™) standard while multi-media and modem applications could use the TMS320 DSP. Future generations of TI chip sets which take advantage of these advanced capabilities are planned.

In addition, TI's wide range of linear, ASIC, and memory products, as well as programmable and general-purpose logic, provide virtually everything you need to build the high-performance PC of today and tomorrow.

Finally, TI's Custom Manufacturing Services can satisfy your PC manufacturing needs—from core systems using TI application-specific processors and chip sets, to system board manufacture and turnkey system integration. TI has the capability to make your system more competitive in the 1990s.

GETTING STARTED

To receive a copy of the TACT82411 User's Guide, please return the attached reply card.

For additional information on this or other Texas Instruments semiconductor products, contact your local TI representative.

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