MSM6388

ADPCM SOLID STATE RECORDER

GENERAL DESCRIPTION

The MSM6388 is a "solid-state recorder" LSI developed using ADPCM (Adaptive Differential Pulse Code Modulation) technology. When an external microphone, speaker driving amplifier, and OKI's original 1M-bit serial voice registers for ADPCM data storage are connected to the MSM6388, it can be used to record and play back voice or other sounds in a manner similar to that of a tape recorder.

FEATURES

- 4bit ADPCM
- Built-in 12bit A/D converter
- Built-in 12bit D/A converter
- Built-in microphone pre-amplifier
- Built-in low pass filter (Attenuation characteristics -40dB/oct)
- Serial voice register
  1Mbit serial voice register (MSM6389):
  Direct drive for 4 serial voice registers
  512Kbit serial voice register (MSM6587):
  Direct drive for 1 serial voice register
  256Kbit serial voice register (MSM6586):
  Direct drive for 1 serial voice register
- Serial Voice ROMs
  1Mbit serial voice ROM (MSM6595-XXX)
  2Mbit serial voice ROM (MSM6596-XXX)
  3Mbit serial voice ROM (MSM6597-XXX)
- Maximum recording time: 262 seconds (when the sampling frequency is 4.0kHz)
- Power supply voltage: 5 V only
- 44 pin V 1 plastic QFP (QFP44-P-910-V1K)

(WHEN USED AS A STANDALONE LSI)

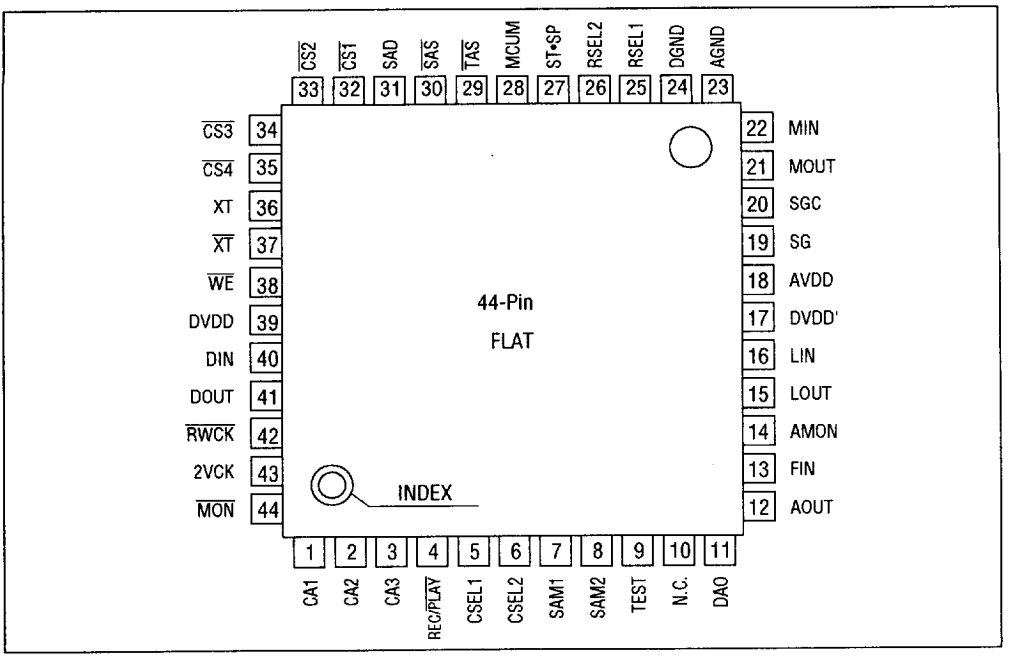
- Oscillator frequency:
  1.5MHz ~ 4MHz
- Sampling frequencies:
  5.2, 5.9, 6.7kHz
  (when the oscillator operates at 1.5MHz)
  3.9, 6.9, 7.8, 8.9 kHz
  (when the oscillator operates at 2.0MHz)
  7.8, 13.9, 15.6kHz
  (when the oscillator operates at 4.0MHz)
- Number of phrases to be recorded
  When one, two, or four serial voice registers are connected, one, two, four or eight phrases can be selected. When three serial voice registers are connected, one, two, three, or six phrases can be selected.
  For the maximum recording time of each channel, the time divided by the number of phrases shall be assigned.

(WHEN INTERFACED WITH A MICRO-CONTROLLER)

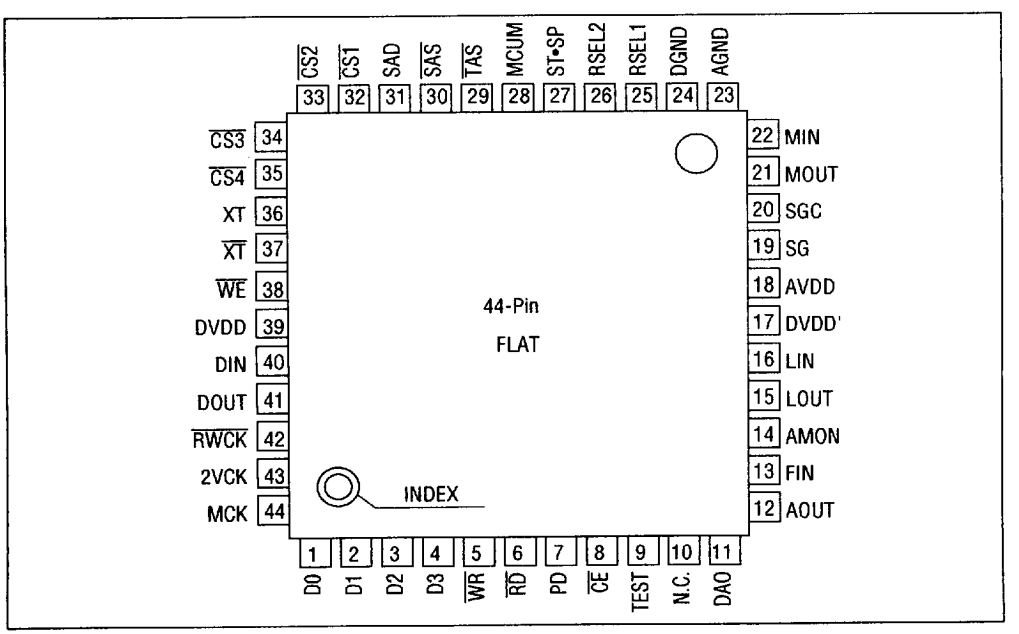
- Oscillator frequency:
  1.5MHz ~ 4MHz
  (when a serial voice register is used)
  1.5MHz~ 8MHz
  (when other memories are used)
- Sampling frequencies:
  3.2kHz ~ 16kHz
  (when a serial voice register is used)
  2.9kHz ~ 32kHz
  (when the other memories are used)
  2.6, 2.9, 3.3, 5.2, 5.9, 6.7kHz
  (when the oscillator operates at 1.5MHz)
  3.5, 3.9, 4.5, 6.9, 7.8, 8.9kHz
  (when the oscillator operates at 2.0MHz)
  6.9, 7.8, 8.9, 13.9, 15.6, 17.8kHz
  (when the oscillator operates at 4.0MHz)
- Number of phrases to be recorded
  To be controlled externally
  The maximum recording time at each channel can be set freely.
- 44 pin V1 plastic QFP (QFP44-P-910-V1K)

PIN LAYOUT

- Stand-alone mode (MCUM pin = "L")

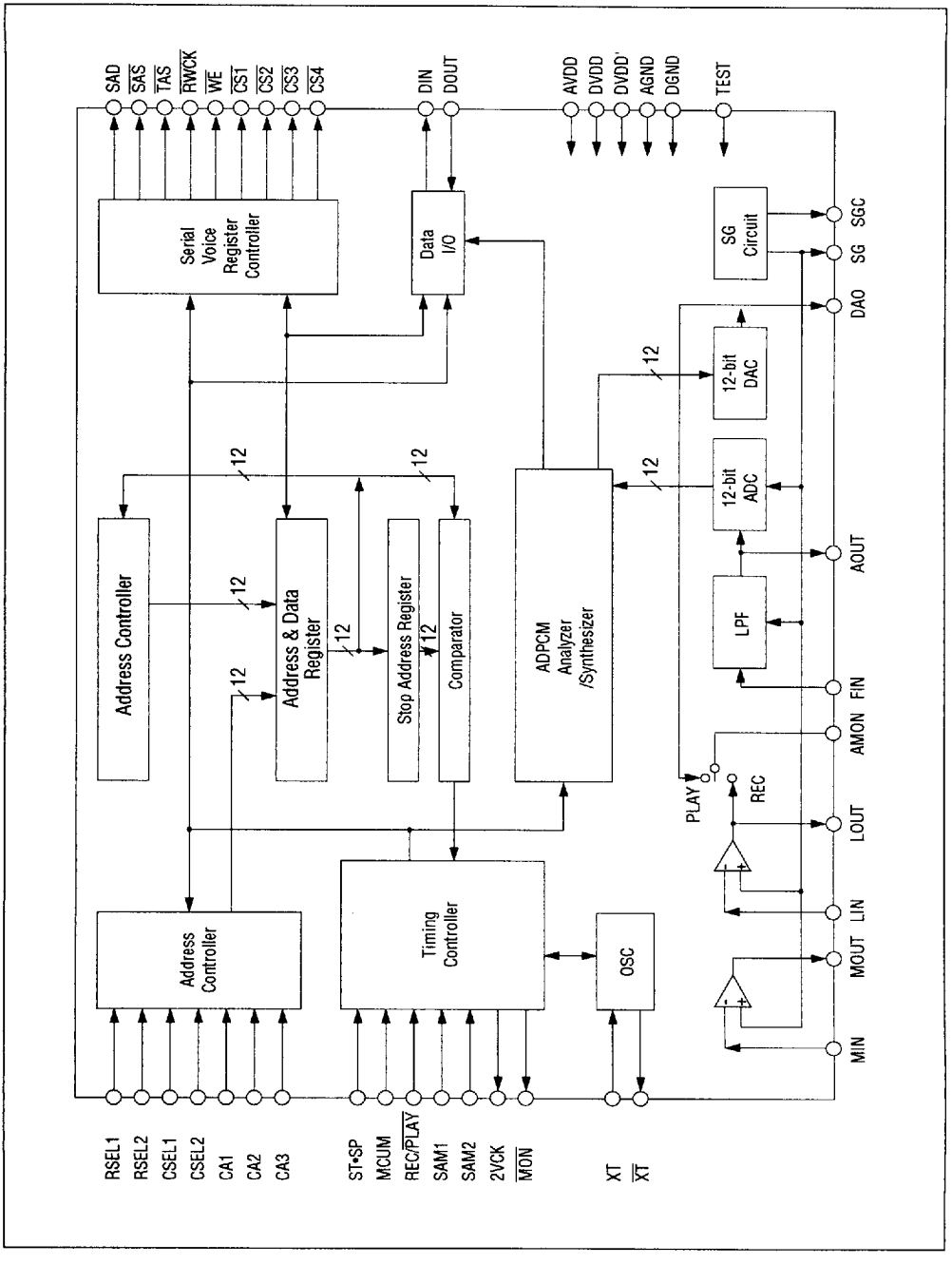


- Microcontroller interface mode (MCUM pin "H")

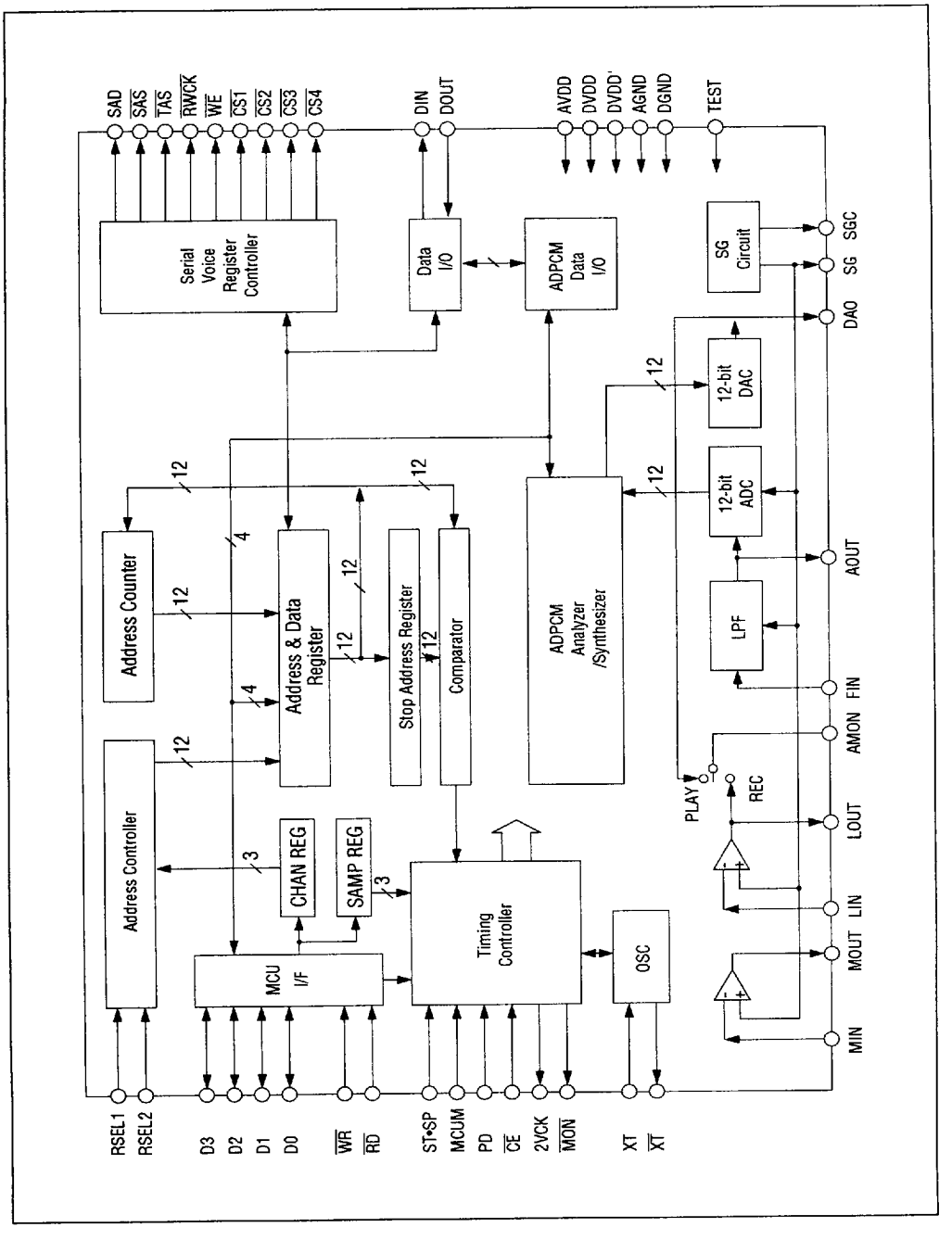


Note: Leave the NC pin open.

CIRCUIT DIAGRAM (Stand-alone application)



CIRCUIT DIAGRAM (microcontroller interface application)



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Item	Symbol	Conditions	Rating	Unit
Power supply voltage	VDD	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Range

Item	Symbol	Conditions	Range	Unit
Power supply voltage	VDD	DGND = AGND = 0V	+3.5 ~ +5.5	V
Operating temperature range	T_{op}	—	−40 ~ +85	°C
Oscillator frequency	f_{OSC}	—	1.5 ~ 8	MHz

• DC Current Characteristics

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High input voltage (Note 1)	V_{IH1}	—	3.6	—	—	V
High input voltage (Note 2)	V_{IH2}	—	0.8×VDD	—	—	V
Low input voltage (Note 1)	V_{IL1}	—	—	—	0.8	V
Low input voltage (Note 2)	V_{IL2}	—	—	—	0.8	V
High output voltage	V_{OH}	I_{OH} = −40μA	4.2	—	—	V
Low output voltage	V_{OL}	I_{OL} = 2mA	—	—	0.45	V
High input current (Note 3)	I_{IH1}	V_{IH} = VDD	—	—	10	μA
High input current (Note 2)	I_{IH2}	V_{IH} = VDD	—	—	20	μA
High input current (Note 4)	I_{IH3}	V_{IH} = VDD	20	—	400	μA
Low input current (Note 1)	I_{IL1}	V_{IL} = GND	−10	—	—	μA
Low input current (Note 2)	I_{IL2}	V_{IL} = GND	−20	—	—	μA
Operating current (1)	I_{DD}	f_{OSC} = 4.0MHz, without load	—	5	10	mA
Operating current (2)	I_{PD}	At power down, without load	—	—	10	μA

Note 1: Applies to the input pins excluding the XT pins.
Note 2: Applies to the XT pin.
Note 3: Applies to the pins not connected to pull-down resistors and excluding the XT pin.
Note 4: Applies to the pins connected to pull-down resistors and excluding the XT pin.

• Analog Characteristics

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Relative DA output error	$\|V_{DAE}\|$	Under no load	—	—	10	mV
DA output impedance	R_{DAO}	—	12	20	28	kΩ
Fin input voltage	V_{FIN}	—	1	—	VDD-1	V
Fin input impedance	R_{FIN}	—	1	—	—	MΩ
Operational amplifier open loop gain	G_{OP}	f_{IN} = 0 ~ 4kHz	40	—	—	dB
Operational amplifier input impedance	R_{INA}	—	1	—	—	MΩ
Operational amplifier load resistance	R_{OUTA}	—	200	—	—	kΩ
AOUT load resistance	R_{AOUT}	—	50	—	—	kΩ

• A.C. Characteristics

1. Stand-alone Application

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C, f_{OSC}=2.048MHz, and f_{sam}=8.0kHz)

Item		Symbol	Min.	Typ.	Max.	Unit
ST・SP pulse width	*	t_{STP}	70	—	—	ms
$\overline{MON}$ clock output time during recording	*	t_{ALW}	—	4	—	S
$\overline{MON}$ clock cycle during recording	*	t_{ALC}	—	256	—	ms
Time before starting record or playback after start pulse input	*	t_{ANA}	—	260	—	ms
Time required for AOUT/DAOUT output to reach 1/2 VDD from GND level	*	t_{DAR}	—	44	—	ms
Time required from the end of playback to power down state	*	t_{DAF}	—	128	—	ms
Time required for voice to be output again during a repeated playback	*	t_{MS}	—	1	—	ms

Note: * Duration of items with "*" is proportional to the cycle of the sampling frequency f_{sam}.

2. Microcontroller Interface Application

(DVDD=AVDD=DVDD'=4.5~5.5V, DGND=AGND=0V, Ta=−40~+85°C, f_{OSC}=2.048MHz, and f_{sam}=8.0kHz)

Item		Symbol	Min.	Typ.	Max.	Unit
PD pulse width		t_{PP}	2	—	—	µs
Time from PD release to $\overline{WR}$ pulse input (Note 2)		t_{PDW1}	10	—	—	ms
		t_{PDW2}	2	—	—	µs
$\overline{RD}$ pulse width		t_{RR}	200	—	—	ns
$\overline{CE}$ setup and hold times to $\overline{RD}$		t_{CR}	50	—	—	ns
Time from $\overline{RD}$ fall to data valid		t_{DRE}	—	60	150	ns
Time from $\overline{RD}$ rise to data float		t_{DRF}	—	40	90	ns
$\overline{WR}$ pulse width		t_{WW}	200	—	—	ns
$\overline{CE}$ setup and hold times to $\overline{WR}$		t_{CW}	50	—	—	ns
Data setup time to $\overline{WR}$ rise		t_{DWS}	100	—	—	ns
Data hold time to $\overline{WR}$ rise	*	t_{DWH}	30	—	—	ns
$\overline{RD}$ and $\overline{WR}$ disable time	*	t_{DRW}	250	—	—	ns
2VCK "H" level time	*	t_{VH}	—	125	—	µs
2VCK "L" level time	*	t_{VL}	—	125	—	µs
MCK "H" level time	*	t_{MH}	—	62.5	—	µs
MCK "L" level time		t_{ML}	—	62.5	—	µs
Time required from 2VCK rise to MCK rise		t_{VM}	—	23.4	—	µs
Time required from MCK rise to the rise of the first shot of $\overline{RD}$ and $\overline{WR}$ pulse	*	t_{RW1}	250	—	—	ns
Time required from MCK rise to the rise of the second shot of $\overline{RD}$ and $\overline{WR}$ pulse		t_{RW2}	—	—	62.5	µs

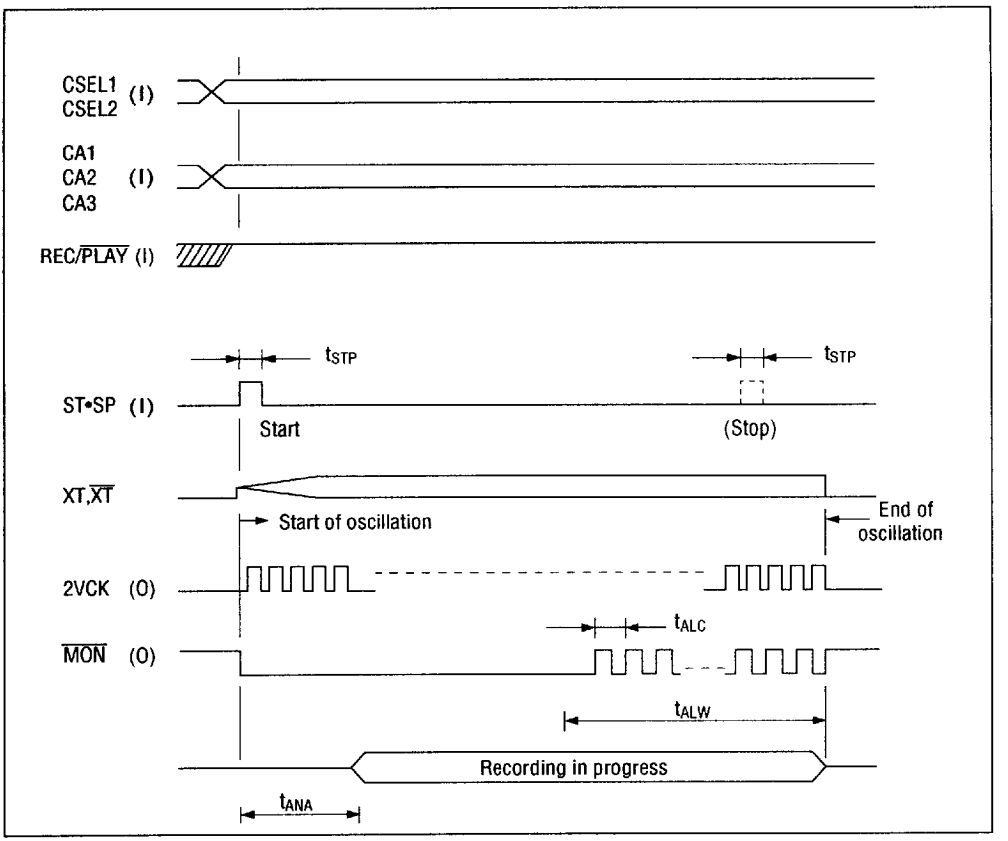
Note 1: * Duration of items marked with "*" is proportionate to the cycle of the sampling frequency f_{sam}.

Note 2: The oscillation stable time is added to t_{PDW1}.
The oscillation stable time is a few tenths of a ms for crystal oscillators and is a few hundredths of a ms for ceramic oscillators.

TIMING CHARTS

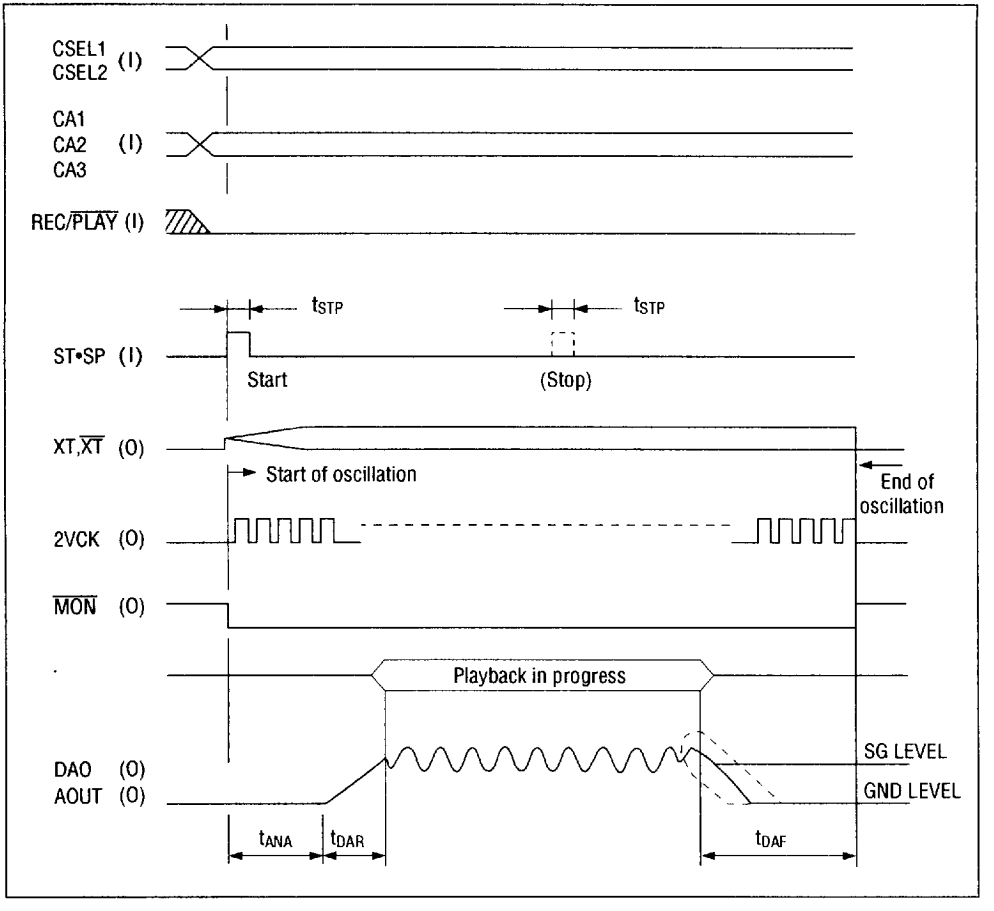
- **Standalone Application**

1. Recording timing

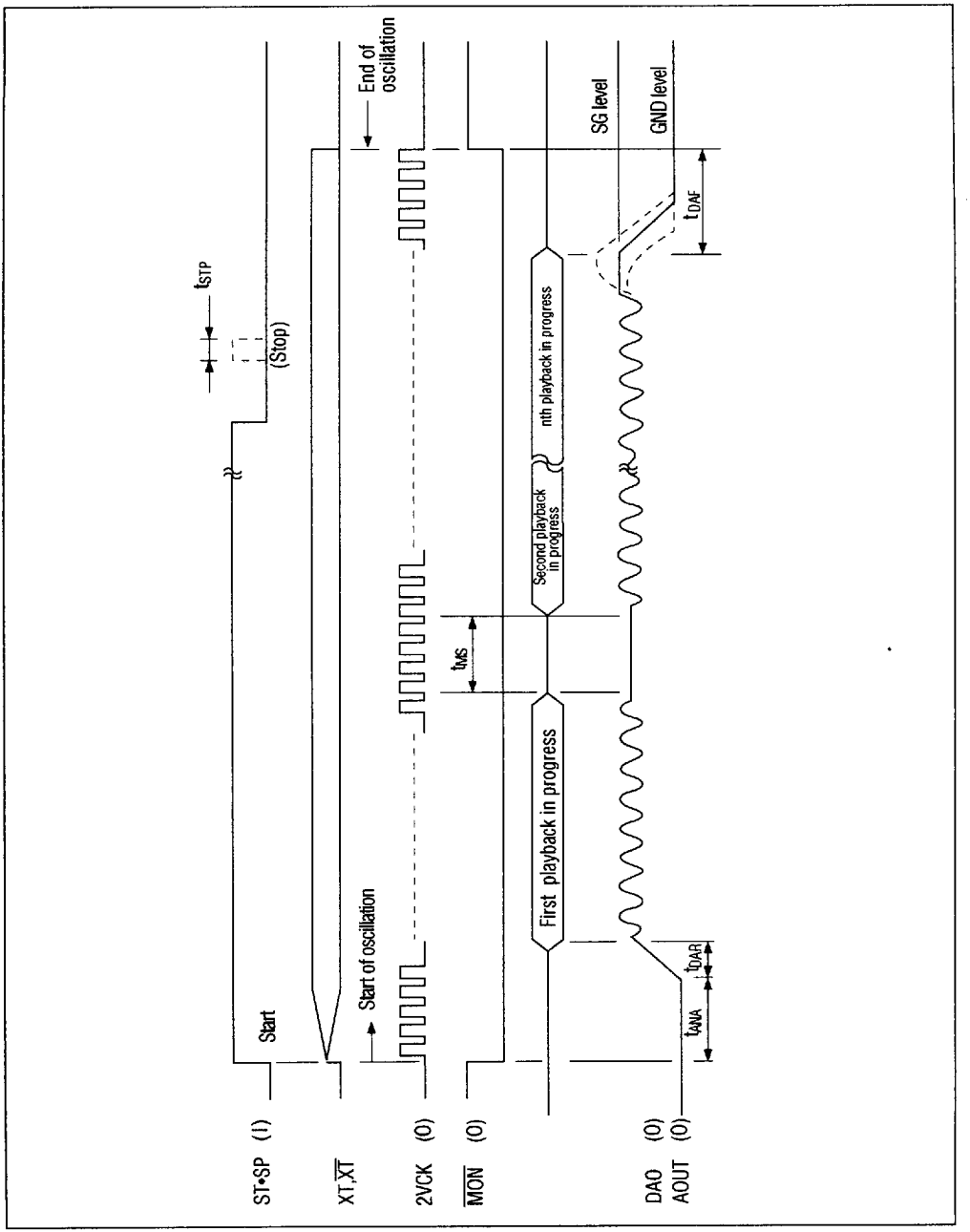


Note: When the remaining capacity of available memory of the selected channels falls to 128K-bit (last four seconds) during recording, a 4Hz clock is output from the MON pin. (f_{sam}=8kHz)

2. Playback Timing



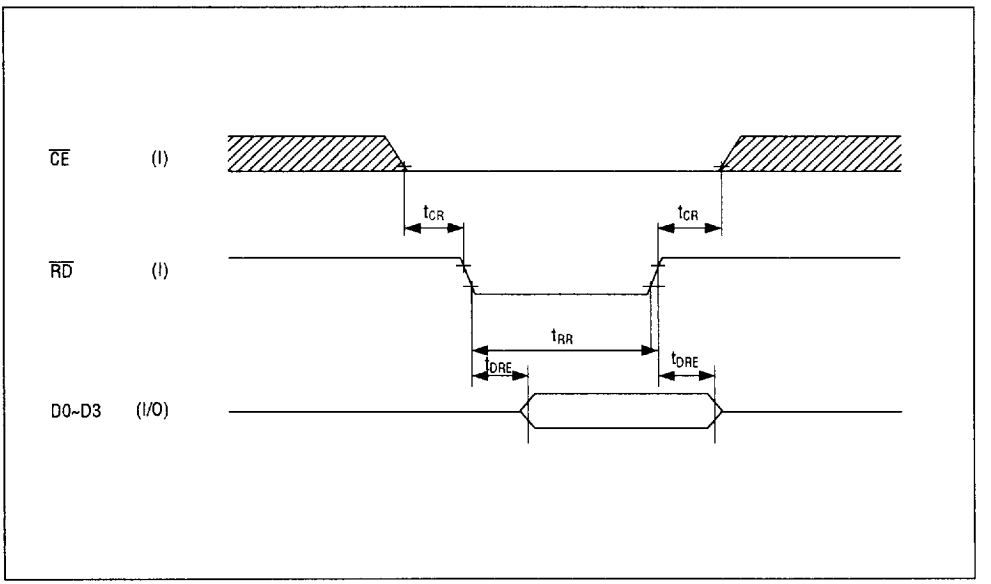
3. Repetitive playback timing



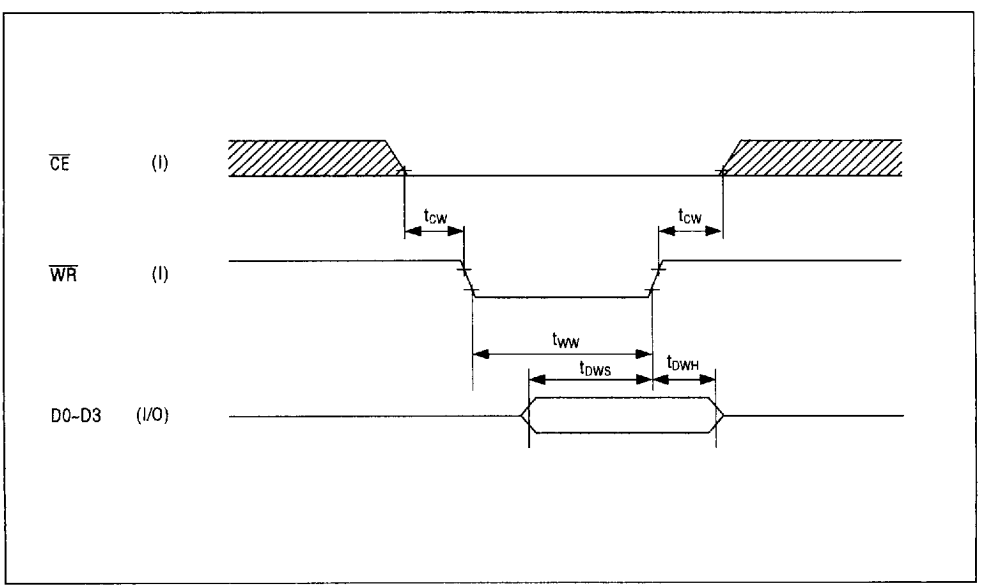
Note: Playback is peformed repeatedly while the ST•SP pin is maintained at the high level. When the pin goes low then a Stop pulse is input or playback proceeds up to the end of the channel memory and is stopped.

• Microcontroller interface application

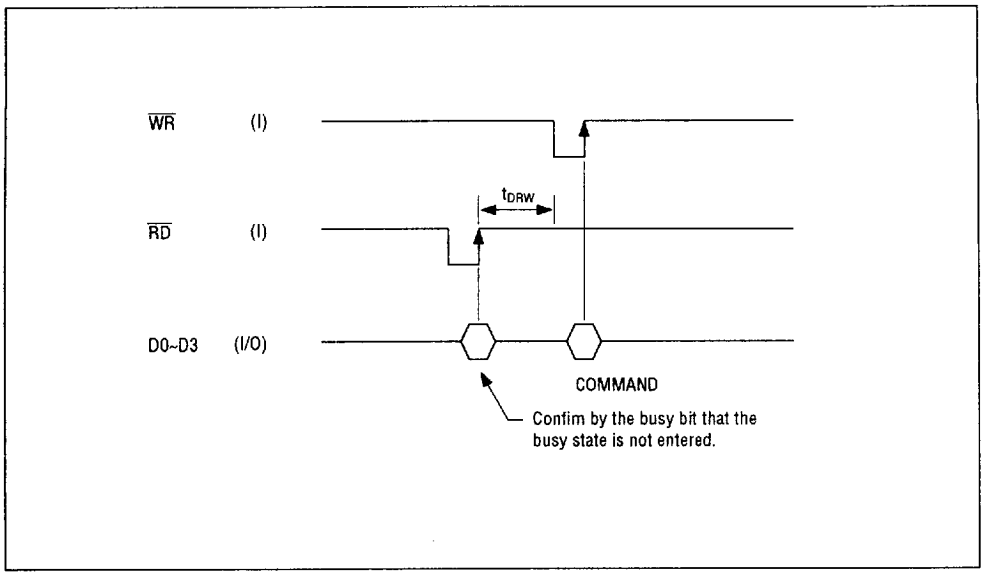
1. Data Read ($\overline{RD}$ pulse)



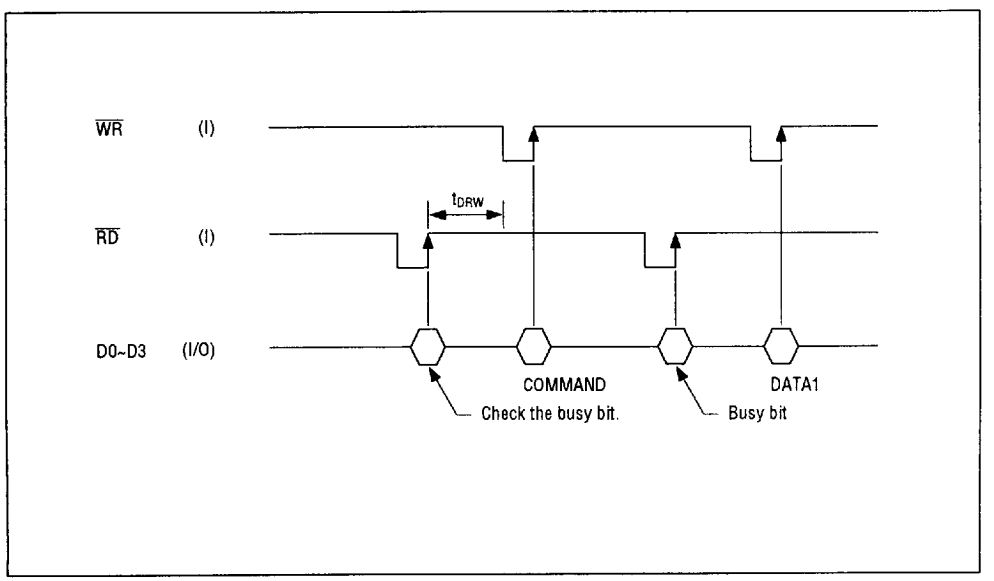
2. Data Write ($\overline{WR}$ pulse)



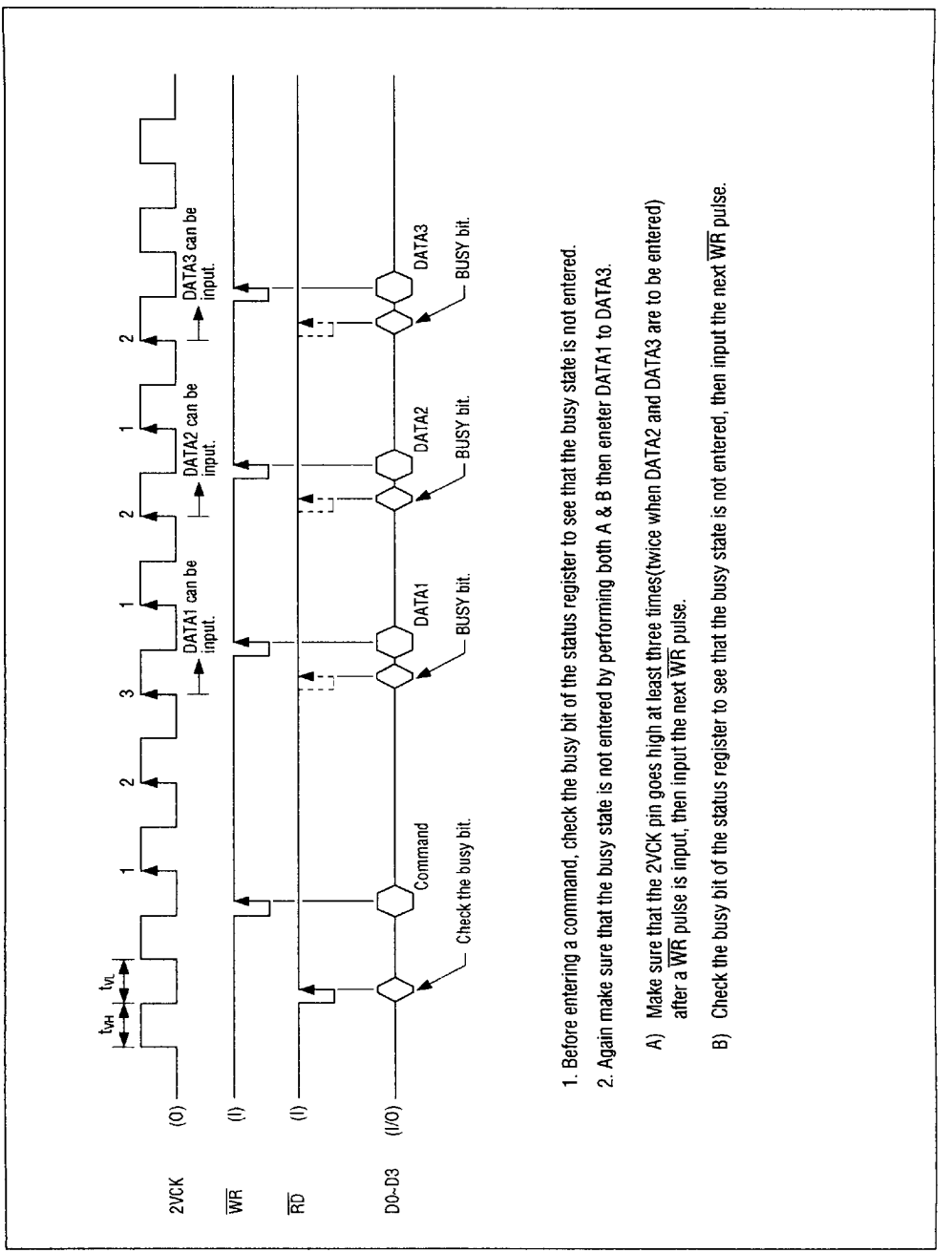
3. How to Input One-nibble Commands, NOP, INIT, PLAY, REC, START and STOP



4. How to Input Two-nibble Commands, SAMP and CHAN

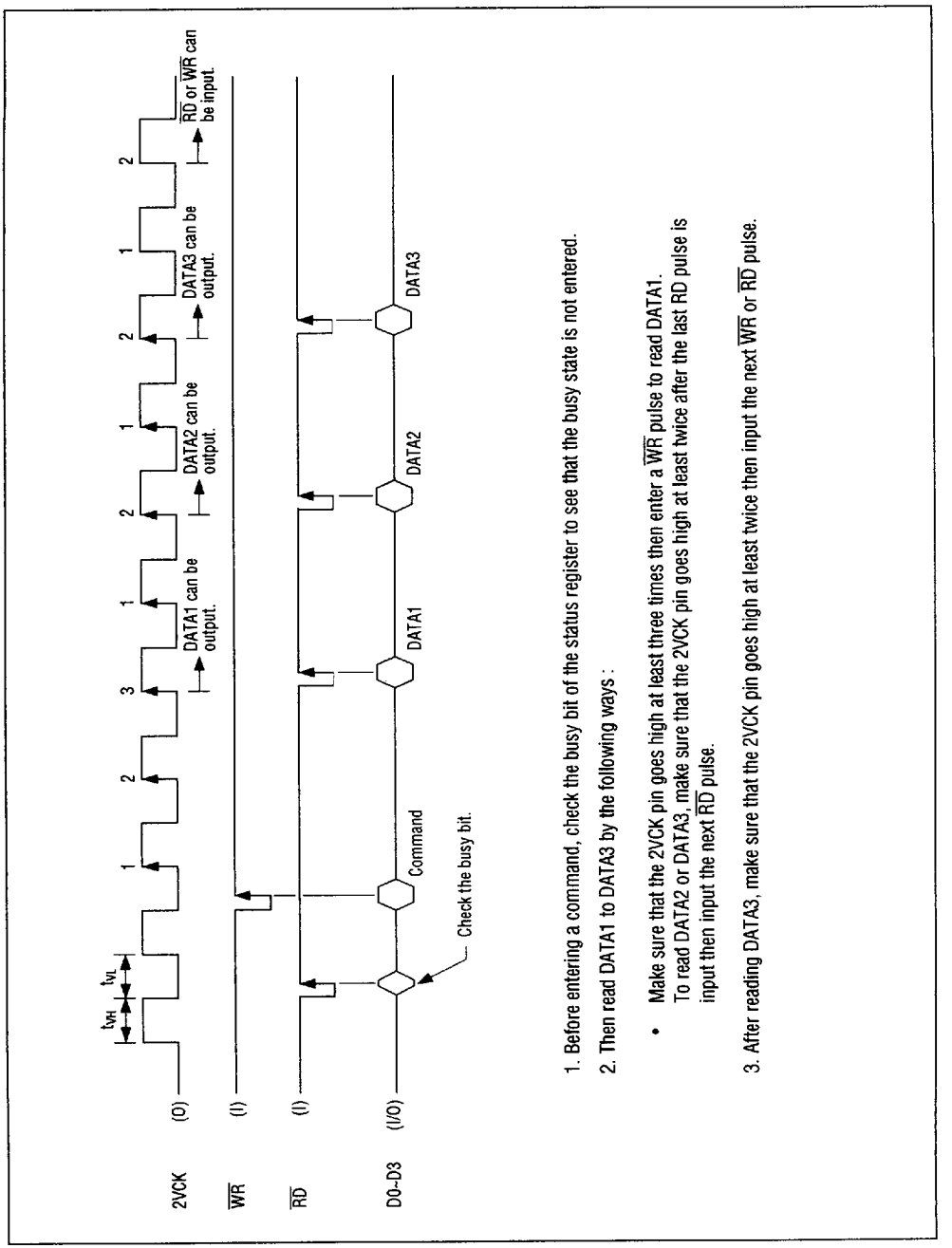


5. How to Enter STWR and SPWR Commands



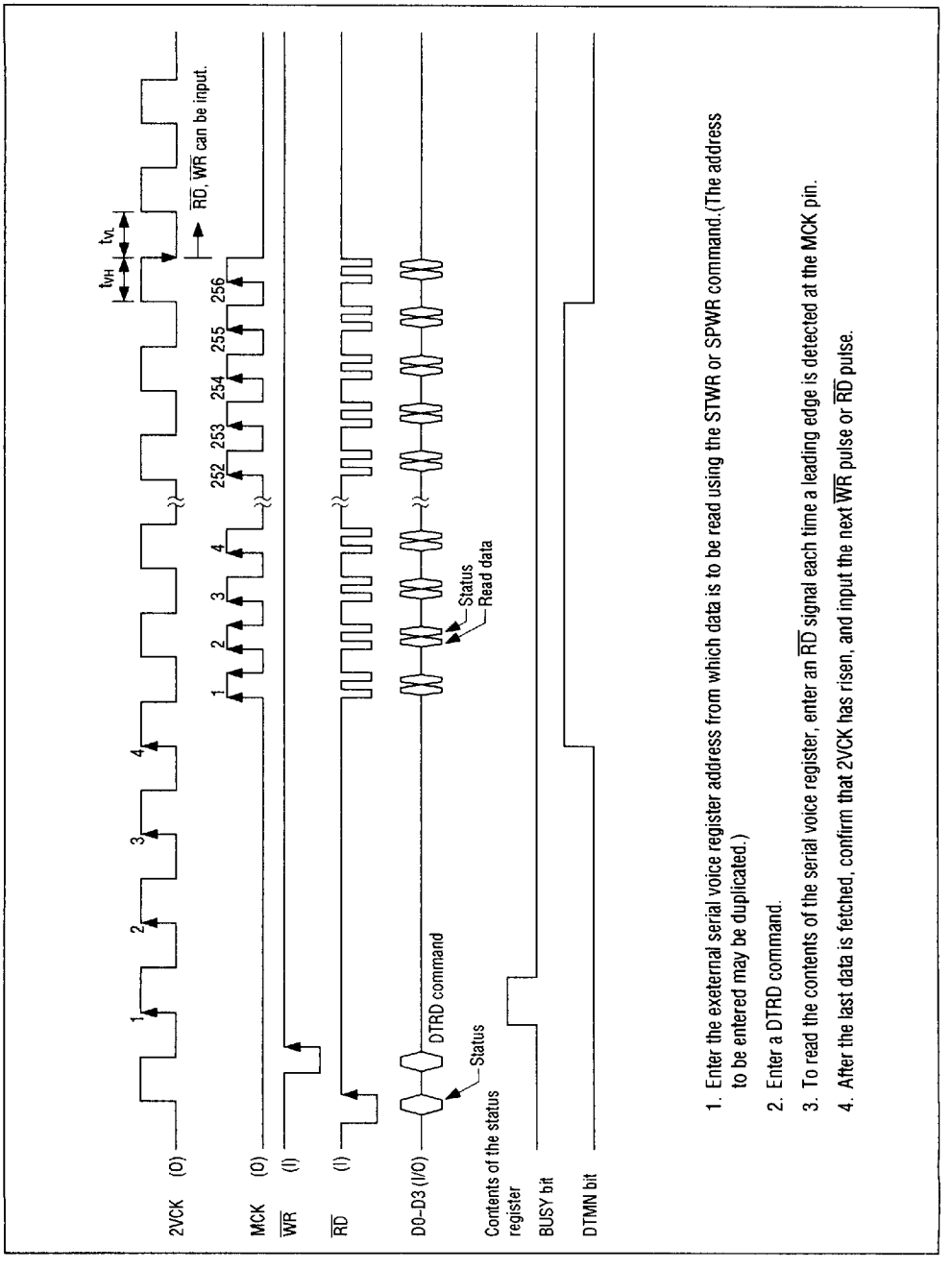
1. Before entering a command, check the busy bit of the status register to see that the busy state is not entered.
2. Again make sure that the busy state is not entered by performing both A & B then eneter DATA1 to DATA3.
   A) Make sure that the 2VCK pin goes high at least three times(twice when DATA2 and DATA3 are to be entered) after a $\overline{WR}$ pulse is input, then input the next $\overline{WR}$ pulse.
   B) Check the busy bit of the status register to see that the busy state is not entered, then input the next $\overline{WR}$ pulse.

6. How to Enter STRD and SPRD Commands

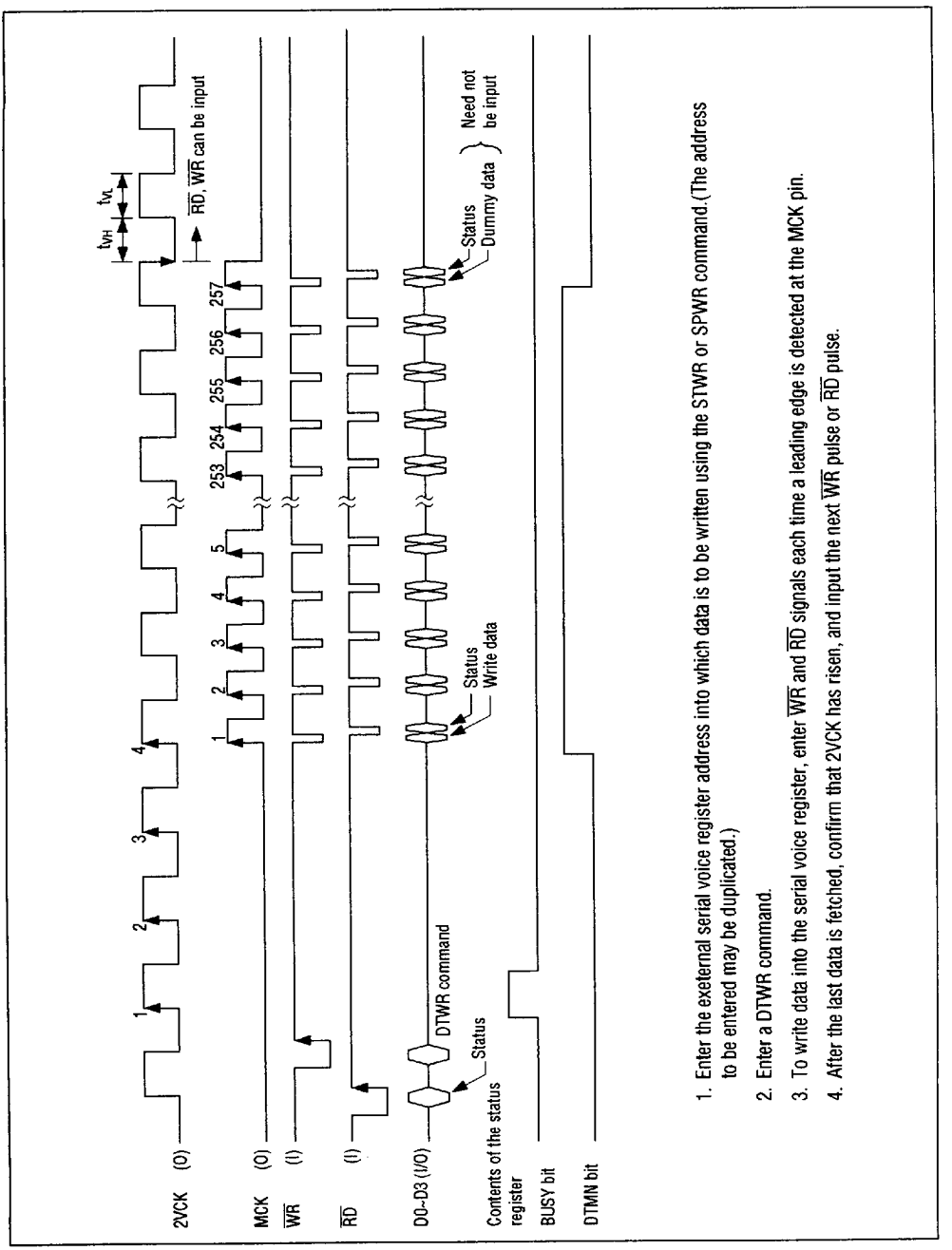


1. Before entering a command, check the busy bit of the status register to see that the busy state is not entered.
2. Then read DATA1 to DATA3 by the following ways :
   - Make sure that the 2VCK pin goes high at least three times then enter a $\overline{WR}$ pulse to read DATA1. To read DATA2 or DATA3, make sure that the 2VCK pin goes high at least twice after the last RD pulse is input then input the next $\overline{RD}$ pulse.
3. After reading DATA3, make sure that the 2VCK pin goes high at least twice then input the next $\overline{WR}$ or $\overline{RD}$ pulse.

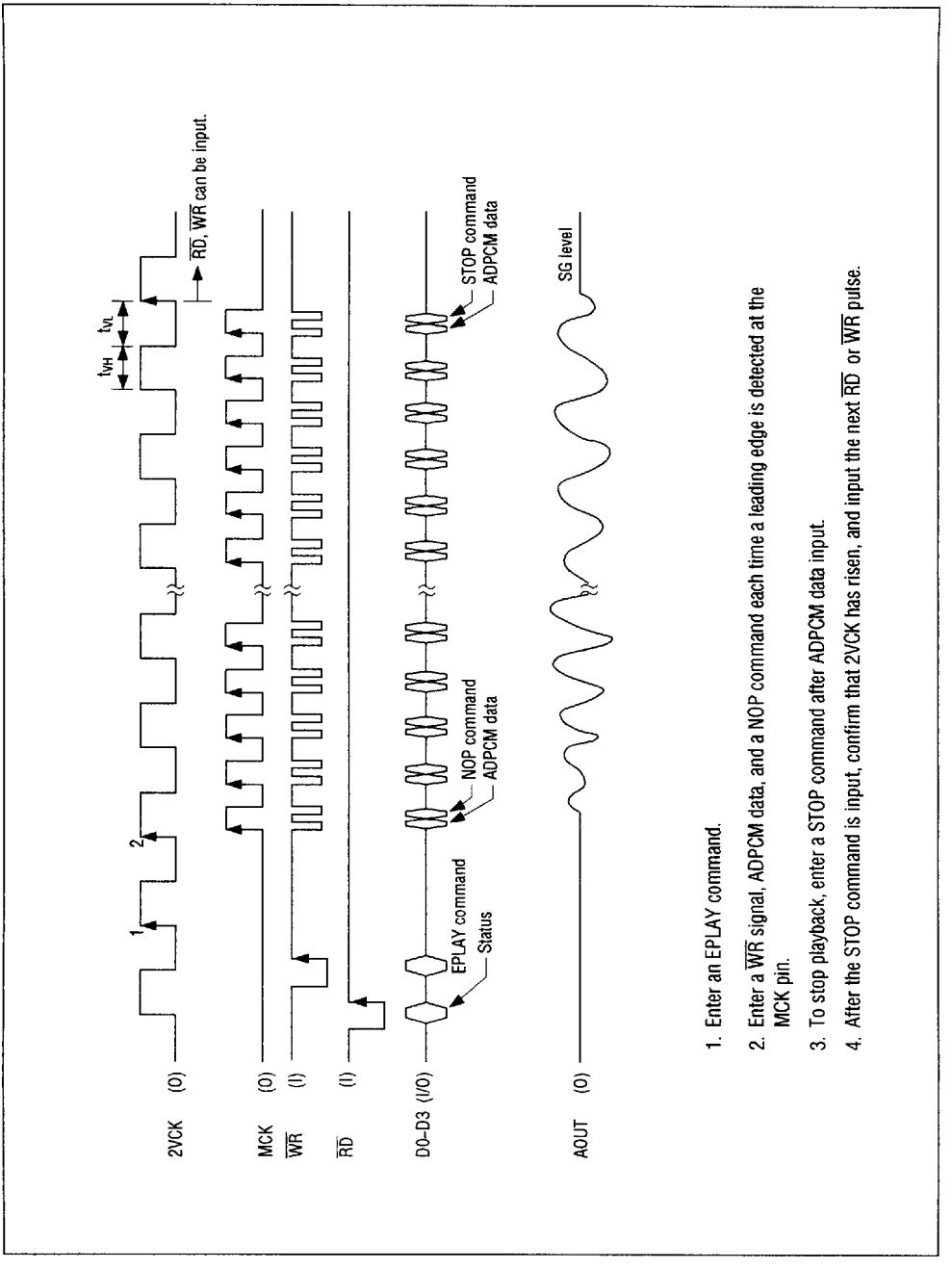
7. How to Read Data from a Serial Voice Register Using a DTRD Command



8. How to Write Data into a Serial Voice Register Using a DTWR Command

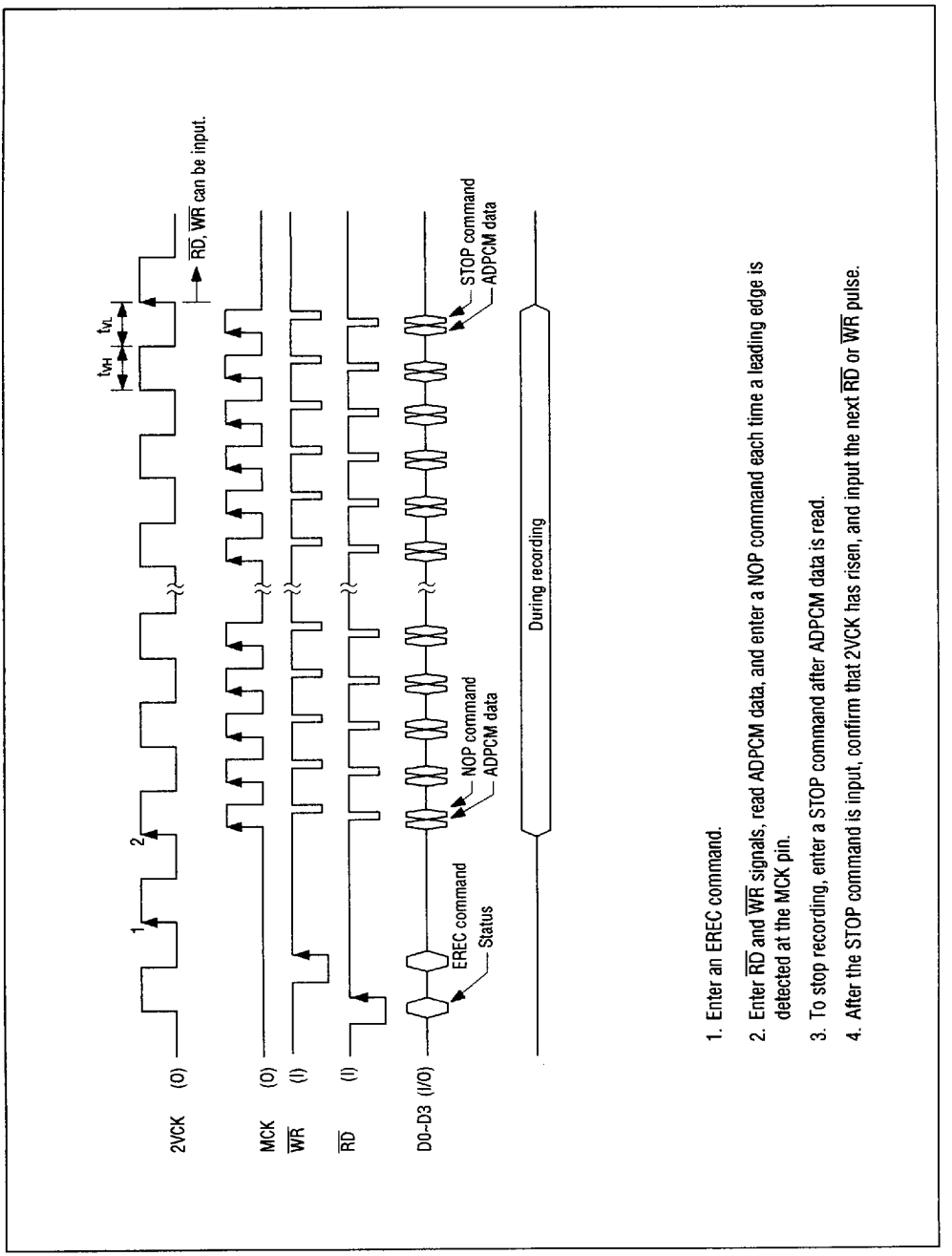


9. How to Playback Using an EPLAY Command



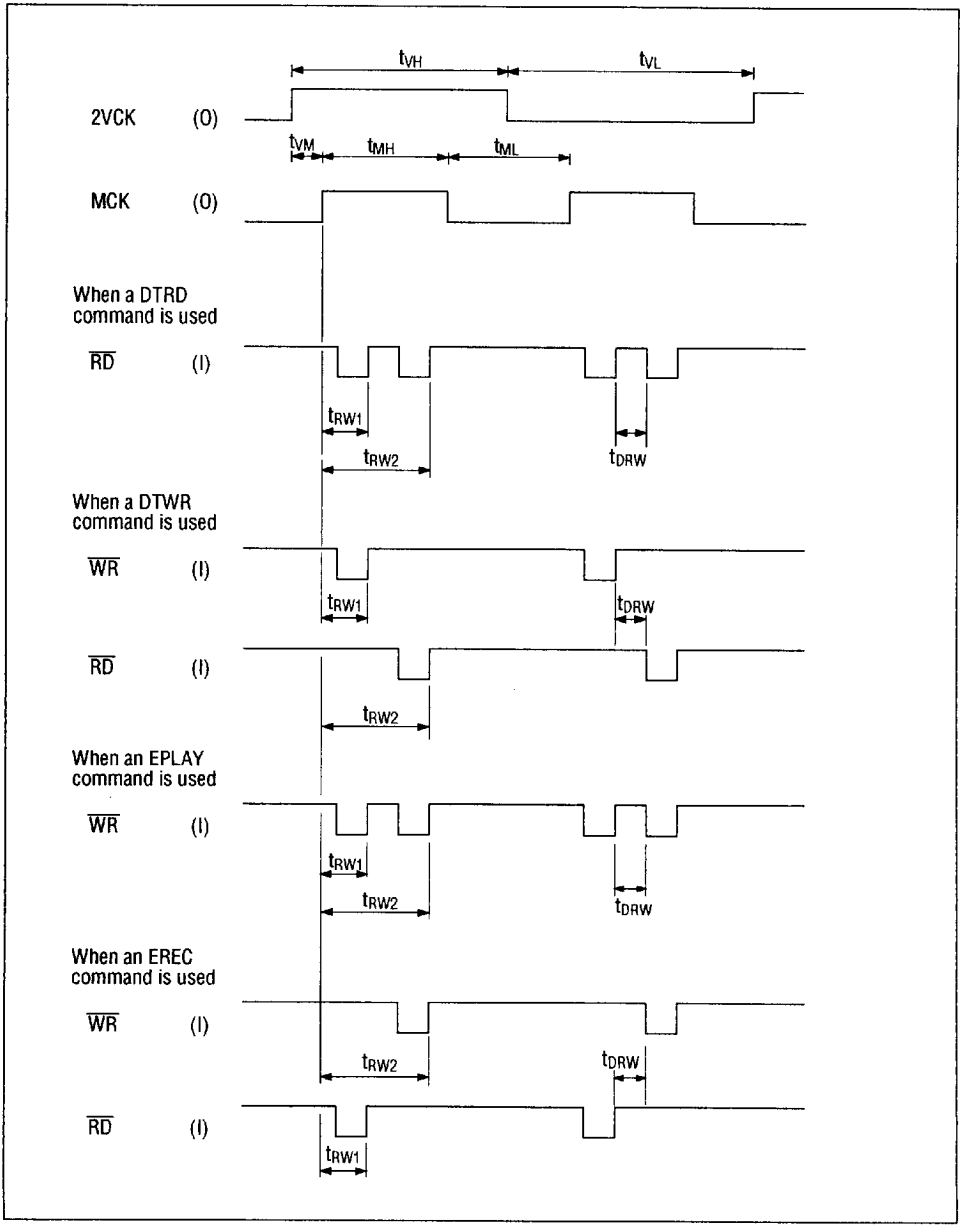
1. Enter an EPLAY command.
2. Enter a WR signal, ADPCM data, and a NOP command each time a leading edge is detected at the MCK pin.
3. To stop playback, enter a STOP command after ADPCM data input.
4. After the STOP command is input, confirm that 2VCK has risen, and input the next RD or WR pulse.

10. How to Record Using an EREC Command

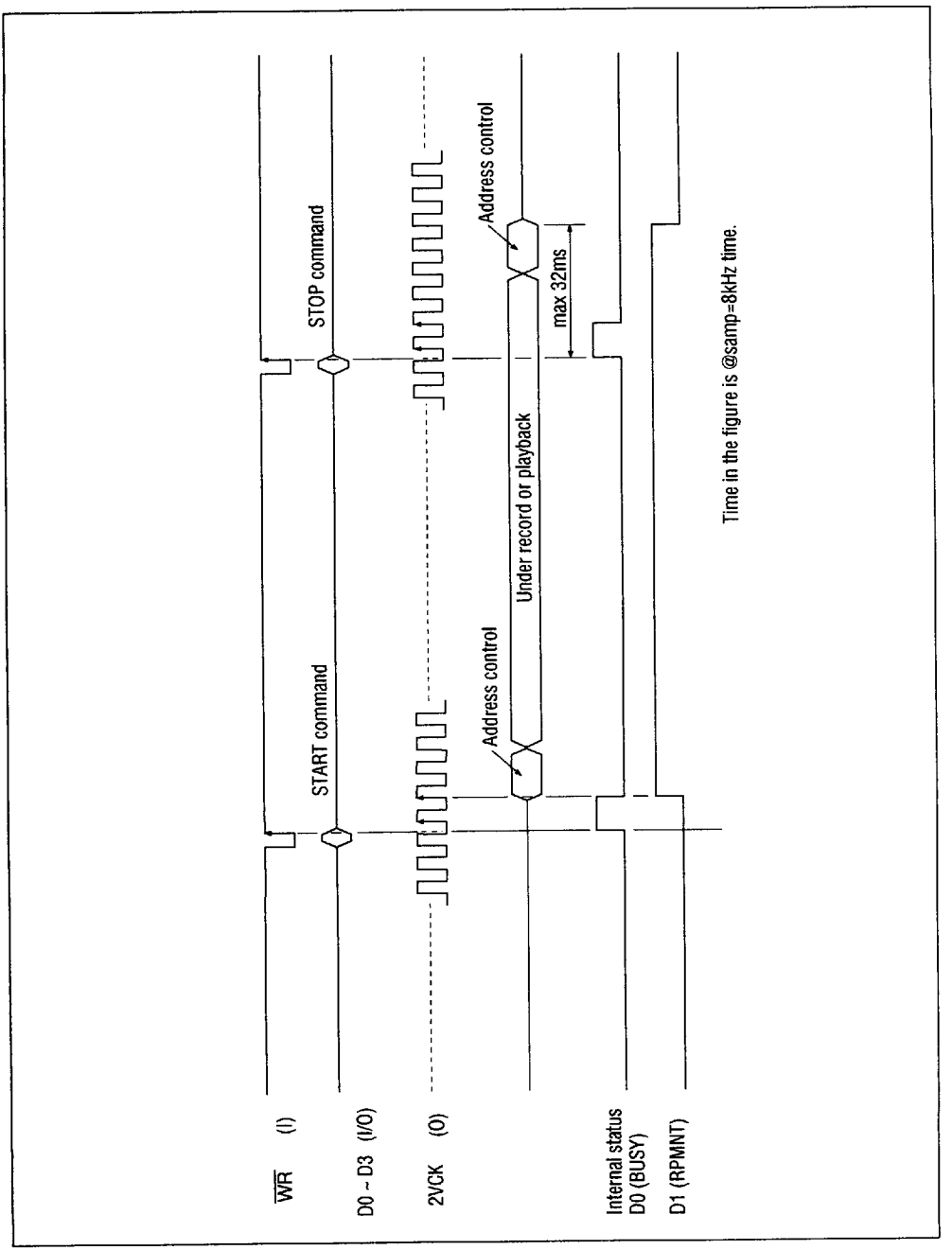


1. Enter an EREC command.
2. Enter $\overline{RD}$ and $\overline{WR}$ signals, read ADPCM data, and enter a NOP command each time a leading edge is detected at the MCK pin.
3. To stop recording, enter a STOP command after ADPCM data is read.
4. After the STOP command is input, confirm that 2VCK has risen, and input the next $\overline{RD}$ or $\overline{WR}$ pulse.

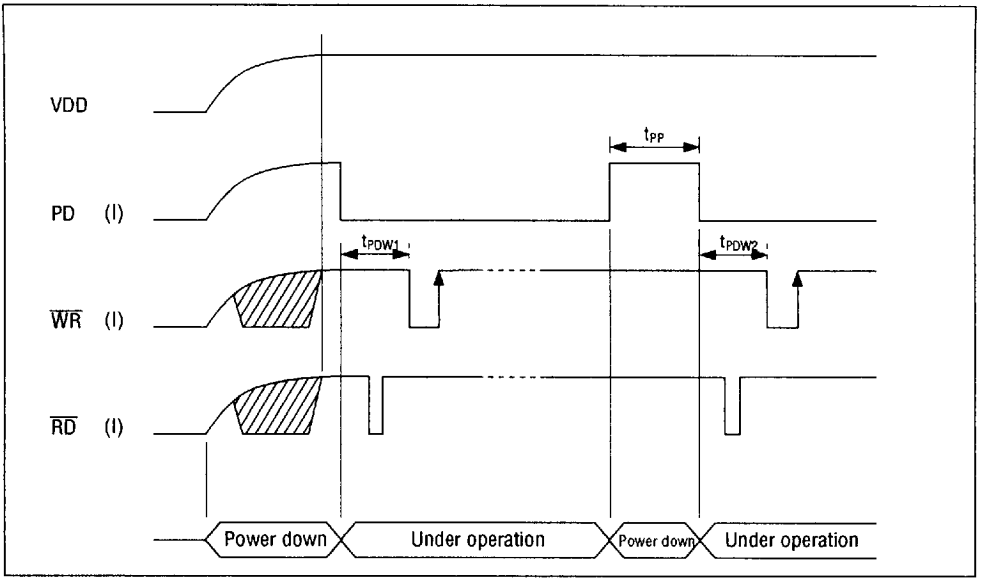
11. How to enter $\overline{WR}$ and $\overline{RD}$ signals in one sampling cycle when a DTRD, DTWR, EPLAY, or EREC command is used



12. Start and Stop of Playback by START Command and STOP Command

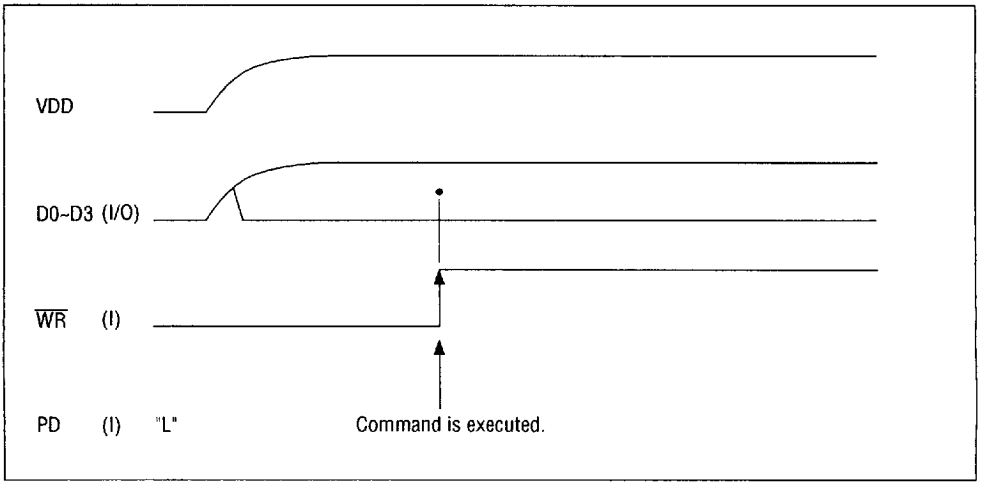


13. Power down, reset timing



Power-down state occurs by inputting "H" level to PD pin and at the same time, the control circuit is reset. However, this is not a forced reset pin, but is invalid during performing DTRD and DTWR commands, and during recording and playback.

After power-on, input "H" level to PD pin until the VDD voltage is stabilized. For instance, after power is put on as illustrated below, the "H" edge is generated at $\overline{WR}$ pin and then the commands of the contents for D_0~D_3 pins are executed. At this time, if a START command or the DTRD and DTWR commands are carried out, the reset by PD pin becomes impossible.



FUNCTION OF PINS

- **Pins for Both Stand-alone and Microcontroller Interface Application**

Pin Name	I/O	Function
DVDD	–	Digital power supply pin
AVDD	–	Analog power supply pin
DVDD'	–	Power supply pin
DGND	–	Digital ground pin
AGND	–	Analog ground pin
SGC SG	O	Outputs the reference voltage (signal ground (SG)) of the analog circuit. A capacitor is connected between this pin and the GND pin to stabilize the voltage.
MIN LIN	I	Input pin that inverts the input to the built-in operational amplifier. Non-inverted pins are connected to the SG internally.
MOUT LOUT	O	MOUT is an output pin of the built-in operational amplifier corresponding to the MIN input pin. The LOUT output pin corresponds to the LIN input pin.
AMON	O	Connected to the LOUT pin during recording and to the DA converter output pin during playback. Connect to the FIN input pin of the built-in amplifier.
FIN	I	Input pin ot the built-in low-pass filter
AOUT	O	Analog voice output pin
DAO	O	Output pin of the built-in 12-bit DA conveter
SAD	O	(Serial Address Data) Connected to the SAD pin of the serial voice register to output the first address for read/write operation.
$\overline{SAS}$	O	(Serial Address Strobe) Clock pin connected to the $\overline{SAS}$ pin of the serial voice register to write serial addresses
$\overline{TAS}$	O	(Transfer Address Strobe) Connected to the $\overline{TAS}$ pin of the serial voice register. The $\overline{TAS}$ pin sets serial addresses to the internal address counter of the serial voice register.
$\overline{RWCK}$	O	(Read/Write Clock) Clock terminal connected to the $\overline{RWCK}$ pin of the serial voice register to read data from and write it into the serial voice register
$\overline{WE}$	O	(Write Enable) Output pin connected to the $\overline{WE}$ pin of the serial voice register to select the write or read mode
DIN	O	(Data Input) Connected to the DIN pin of the serial voice register to outputwrite data

Pin Name	I/O	Function
DOUT	I	(Data Output) Connected to the DOUT pin of the serial voice register to fetch read data. **When used at stand-alone mode, insert a pull-down register of about 100kΩ between DOUT pin and GND.**
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	O	(Chip Select) Connected to the $\overline{CS}$ pin of the serial voice register
MCUM	I	Determines whether the LSI is used in stand-alone mode or connected to a microcontroller interface. High level: Connected to a microcontroller interface Low level: Used as a stand-alone LSI
RSEL1 RSEL2	I	(Register Select) Selects the number of serial voice registers. For details, see Explanation of Functions described later.
2VCK	O	Outputs a clock at a frequency half the sampling frequency. Used as a synchronizing clock when the LSI is connected to a microcontroller interface.
XT	I	Connected to the resonator. When an external clock is used, clock pulses are supplied through this pin. When the power goes down, it is set to the ground level.
$\overline{XT}$	O	Connected to the resonator. When an external clock is used, it must be left open.
TEST	I	LSI test pin. Connected to a pull-down resistor in the LSI. This pin must be set at the low level.

- **Stand-alone Application**

Pin Name	I/O	Function
CSEL1 CSEL2	I	Selects the number of phrases to be recorded. For details, see Explanaiton of Functions described later.
CA1 CA2 CA3	I	Specifies a channel. For details, see Explanation of Functions described later.
SAM1 SAM2	I	Sample frequency selection. The relationships between the oscillator frequency (f_{OSC}) and the sampling frequency (f_{sam}) are as follows (the frequencies in parentheses are measured at f_{OSC}=2.048MHz):
REC/$\overline{PLAY}$	I	Selects the recording mode when the input is at the high level or the playback mode when it is at the low level.
ST•SP	I	Allows the starting or ending of recording or playback to be commanded by inputting a high pulse. It also allows repetitive playback when the high level is maintained during playback.
$\overline{MON}$	O	Set at the low level during recording or playback. When the remaining memory capacity of the channel is almost full, this pin outputs a clock.

SAM2	L	L	H	H
SAM1	L	H	L	H
f_{sam}	$\frac{f_{OSC}}{512}$ (4.0kHz)	$\frac{f_{OSC}}{288}$ (7.1kHz)	$\frac{f_{OSC}}{256}$ (8.0kHz)	$\frac{f_{OSC}}{224}$ (9.1kHz)

- **Microcontroller Interface Application**

Pin Name	I/O	Function
D3 D2 D1 D0	I/O	Connects to a bidirectional data bus to transfer data and commands to and from an external microcontroller.
$\overline{WR}$	I	Write pulse input pin to write commands or data
$\overline{RD}$	I	Read pulse input pin to read status or data
PD	I	When a high Power Down is input, the LSI enters the power down state.
$\overline{CE}$	I	When a high Chip Enable is input, the write pulse $\overline{WR}$ and read pulse $\overline{RD}$ cannot be accepted and pins D0 to D3 go high impedance.
MCK	O	Outputs a synchronizing clock when ADPCM data is tranferred directly to and from a microcontroller by an EREC or EPLAY command or when data is transferred directly between a microcontroller and serial registers by a DTWR or DTRD command.
ST•SP	I	Not used. Since it is connected to a pull-down resistor in the LSI, it must be set at the low level.

EXPLANATION OF FUNCITONS

• Recording time and memory capacity

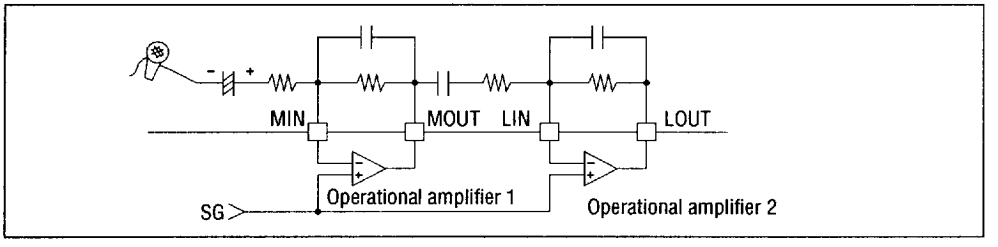
The recording time depends on the capacity of the external serial voice register, sampling frequency, and ADPCM bit length. The relationship between these factors is represented by the following expression:

$$\text{Recording time} = \frac{1.024 \times \text{memory capacity (K-bit)}}{4(\text{kHz}) \times 4(\text{bit})}(\text{S})$$

• Analog input amplifier circuit

The LSI described in this manual has two operational amplifiers configured as a microphone preamplifier. The LSI is provided with pins for inverted input and output of each amplifier.

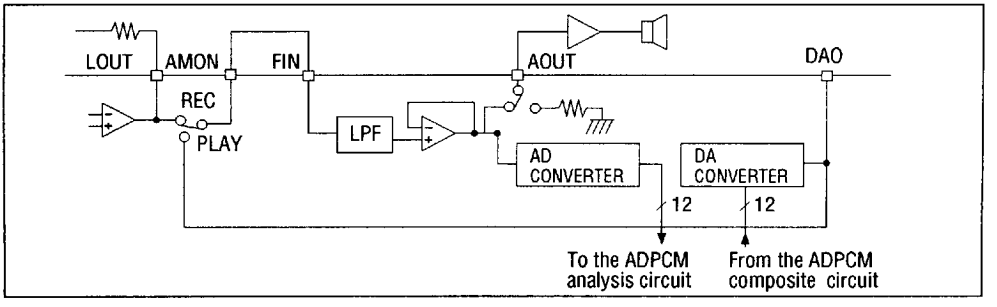
The noninverted input pins are connected to the signal ground (SG) used as the analog circuit reference voltage in the LSI. For amplification, an inverted amplifier circuit is formed. The gain of the amplifier can be adjusted by an external resistor.



• Connection of the low-pass filter circuit periphery

In the LSI, the amplifier circuit from the LOUT pin is connected to the AMON pin. During playback, the D/A converter output from DAO pin is connected to the AMON pin.

The LSI incorporates a fourth-order low-pass filter employing switched capacitor filter technology. Input is provided to the low-pass filter through the FIN pin. Therefore, the AMON pin is connected to the FIN pin directly.

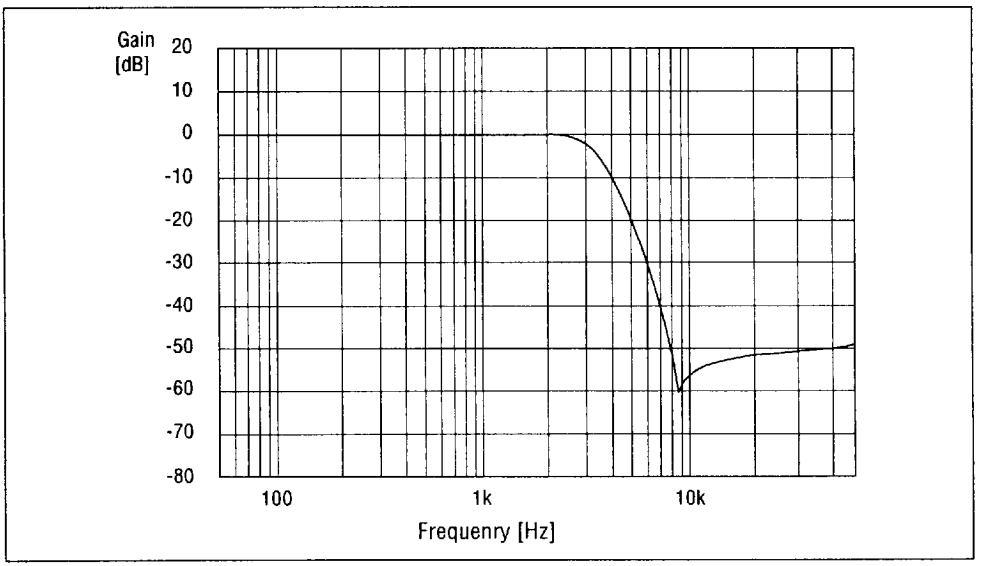


- **LPF characteristics**

The LPF attentuation characteristics of this LSI are about -40dB/oct, and the cutoff frequency and frequency characteristics vary in proportion to the sampling frequency (fsam).

The cutoff frequency is about 3.2kHz when the sampling frequency is 8kHz.

The LPF frequency characteristics are shown below.



LPF Frequency Characteristics (f_{sam}=8.0kHz)

- **Analog (voice) output**

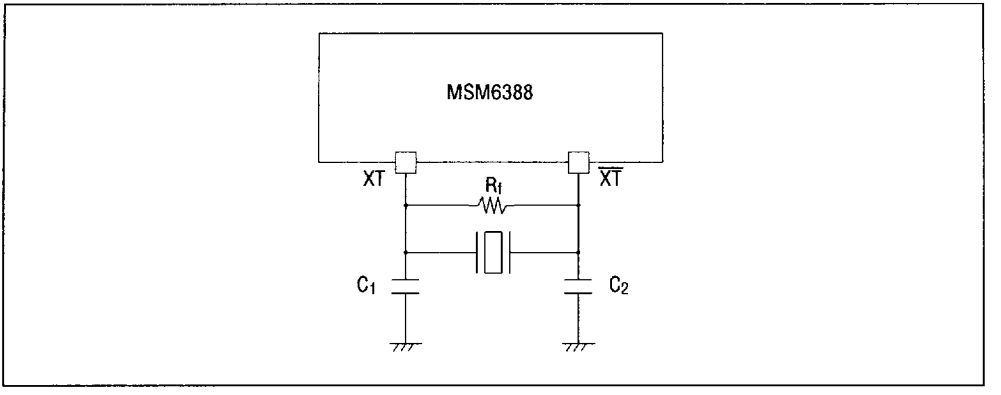
During playback this signal is output from the AOUT pin. Connect the output to a speaker through a power amplifier suitable for driving speakers of from 4 to 16Ω impedance.

The amplitude of the built-in 12bit D/A converter output, provided from the DAO pin, is a maximum of 4095/4096 × VDD. When not using the built-in low-pass filter, connect it to the DAO pin.

- **How to connect the oscillator**

The ceramic oscillator or crystal oscillator are connected to the XT and $\overline{XT}$ terminals as shown below.

For reference, when the ceramic oscillator manufactured by KYOCERA or Murata Seisakusho is connected, the optimum load capacity value is as shown below.



Ceramic oscillator			Optimum load capacity value		Feedback resistance
Model Name		Frequency (Hz)	C_1(PF)	C_2(PF)	R_f(Ω)
Murata Seisakusho	CSA 1.500MK	1.5M	30	30	(1M)
	CSA 2.00MG	2.0M			
	CSA 4.00MG	4.0M			
	CSA 8.00MT	8.0M			
KYOCERA	KBR 2.0MS	2.0M	33	33	—
	KBR 4.0MS	4.0M			
	KBR 8.0MS	8.0M			

- **Battery back up of the 1M serial voice registers**

When backing up the 1M serial voice register, back up MSM6388 at the same time. When backing up only a 1M serial voice register, the bootstrap function works and cannot be played back when the power supply is turned on.

An example of the circuit that obtains VDD supply power is shown below. In this case, VDD and VDD at back up is about respectively 0.7V lower than the system power supply voltage and battery voltage due to the drop of the diode forward voltage.

The non-volatile battery backup circuit has the following conditions:

(1) When the VDD supply voltage is dropped, the H level of the input signal must not exceed VDD +0.3V.

(2) VDD at the time of backup must be in the range of 3.5 to 5.5V.

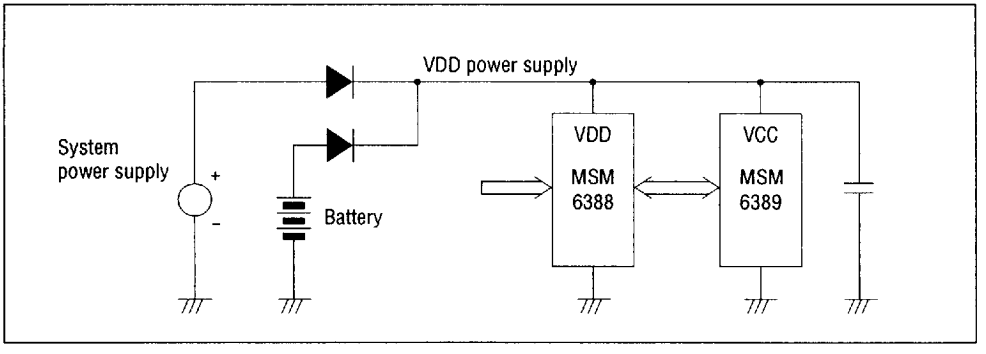


Figure: Example of Battery Backup Circuits of MSM6388 and MSM6389

- **Battery driving**

An example of the estimated battery life when a +4.5V power supply is operated by serially connecting four MSM6389's, MSM6388, speaker driver, and speaker (example of application circuit and circuit diagram 1) with three dry cell batteries is shown below.

For the current capacity, assume a 3 SUM Mn dry cell battery (R6P), and the capacity up to the drop of the voltage to 1.2V of about 600 mAhrs. When the section consuming current in Circuit Diagram 1 is divided into the MSM6388, four MSM6389's, amplifier, and speaker, the current consumed in each section is as shown in the table below, corresponding to each operation mode.

Circuit	Operation mode		
	At recording	At playback	At data retention
MSM6388	5mA	5mA	—
MSM6389 (four)	1mA	1mA	30μA × 4 = 120μA
Amplifier, speaker	—	20mA	—
Total	6mA	26mA	0.12mA

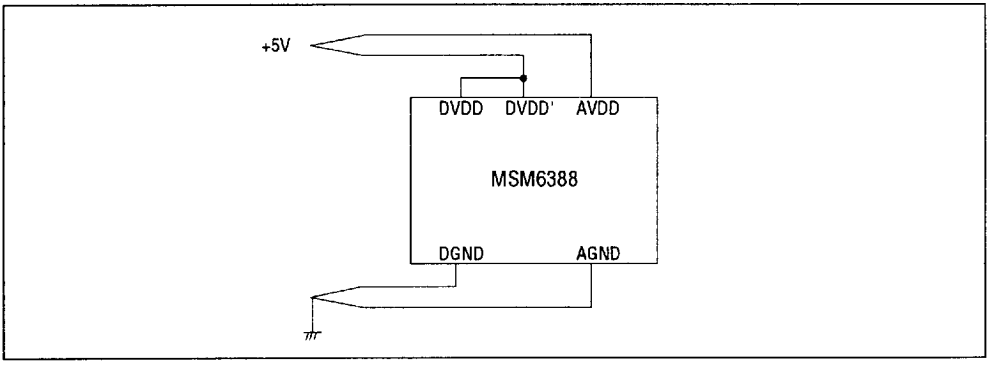
When the recording time per day is 4 minutes, playback time 4 minutes, and the data retention time is 10 hours as the standard time, the current consumption per day is:

At recording:
$$6mA \times \frac{4}{60} = 0.4mAhrs$$
At playback:
$$26mA \times \frac{4}{60} = 1.73mAhrs$$
At data retention:
$$0.12mA \times 10 = 1.2mAhrs$$

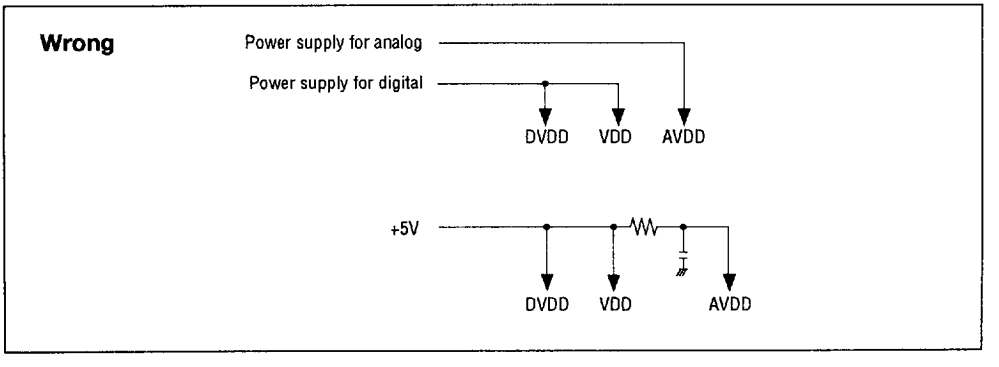
The total consumption per day is 3.3 mAhrs. In other words, if a battery of 600 mAhrs is used for the capacity,a service life of 600 mAhrs/3.3 mAhrs = 180 days is provided. The battery can be used for six months without replacement.

- **Power supply wiring**

Supply the power supply of this LSI from the same power source as illustrated below, while separating the analog portion and logic portion in wiring.



If the analog portion and logic portion are suppied from a separate power source, make sure the voltage difference between both power sources does not exceed ±3 volts or latch-up may occur.



- **Increasing Power supply**

The internal power-on reset circuit of MSM6388 requires that the common supply voltage to AVDD, DVDD, and DVDD' is increased from 0 to +3.5V exponentially and smoothly within 20ms. If the voltages of less than 20ms is provided or if by accident the voltage drops once during the increasing period the MSM6388 may behave unpredictable.

- **Power OFF/ON**

During an interval between a power OFF and a subsequent power ON, the level on VDD input must be less than 0.05V at the instant of a new power ON. Also, this measure accounts for the nature of the internal power-on reset circuit.

- **Operations in the standalone application**

1. Power down function

When the LSI is not recording or playing back data, the power down function is enabled and oscillation is stopped. At power down when an external clock is used, be sure to set the XT pin to the ground level to lower current consumption.

2. Oscillator frequency and sampling frequency

The oscillator frequency fosc can be used between 1.5MHZ and 4MHZ. The sampling frequency (fsam) is related to the oscillator frequency as follows, according to the settings of the SAM1 and SAM2 pins:

SAM2	L	L	H	H
SAM1	L	H	L	H
f_{sam}	$\frac{fosc}{512}$ (4.0kHz)	$\frac{fosc}{288}$ (7.1kHz)	$\frac{fosc}{256}$ (8.0kHz)	$\frac{fosc}{224}$ (9.1kHz)

Note: Sampling frequencies in parentheses are measured at an oscillator frequency of 2.048 MHz.

If the sampling frequency during playback is varied from fsam during recording, fast and slow playback are possible. In this case, the sound level is also varied.

Example:
Sampling frequency during recording:
8.0kHz
Sampling frequency during playback:
7.1kHz: Slow playback
9.1kHz: Fast playback

3. Use of channels

Set the RSEL1 and RSEL2 input pins according to the number of 1Mbit serial voice registers connected to the LSI (see the table below).

RSEL2	L	L	H	H
RSEL1	L	H	L	H
Number of serial voice registers	1	2	3	4

The number of the phrases to be recorded can be set to 1, 2, 4, or 8 according to the setting of the CSEL1 and CSEL2 input pins. (When three external serial voice registers are used, the phrase count can be set to 1, 2, 3, or 6.)

The memory capacity of the external serial voice registers available to each channel equals the total available memory divided by the number of phrases being recorded. IE: When the phrase count is set to 8, for example, one-eighth of the entire memory capacity is assigned as the memory capacity of each channel, and when the phrase count is 4, one-fourth of the entire memory capacity is assigned. (The memory capacity divided and assigned to each channel is called the channel memory capacity.)

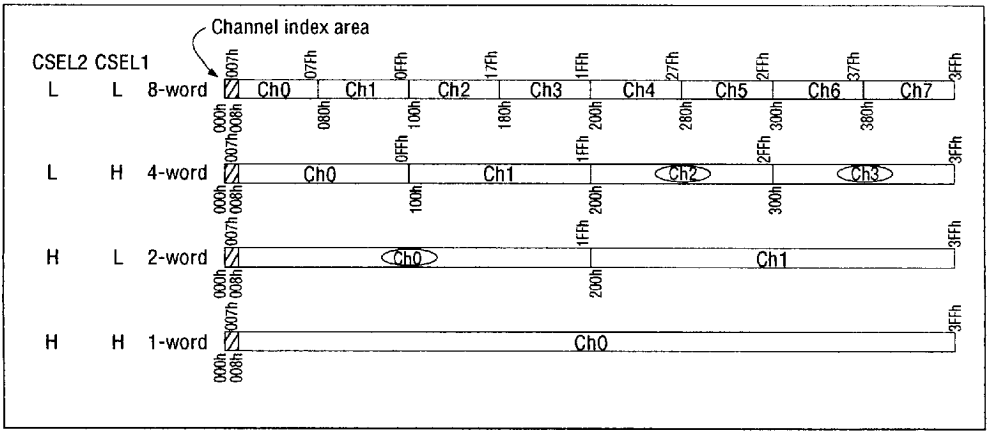
Each channel memory capacity can be assigned to a particular channel by the CA1, CA2, and CA3 input pins.

The relationships between the number of external serial voice registers used, the number of phrases to be recorded, channels, and channel memory capacities are shown in the following table.

CSEL 2	CSEL 1	Number of phrases 1,2, or 4 (Note1)	Number of phrases 3 (Note1)	CA3	CA2	CA1	Channel 1,2, or 4 (Note1)	Channel 3 (Note1)	Channel memory capacity (bit) 1 (Note1)	2 (Note1)	3 (Note1)	4 (Note1)
L	L	8	6	L	L	L	**ch0	ch0	128K (4 s)	256K (8 s)	512K (16 s)	
				L	L	H	**ch1	ch1				
				L	H	L	*ch2	ch2				
				L	H	H	*ch3	ch3				
				H	L	L	ch4	ch4				
				H	L	H	ch5	ch5				
				H	H	L	ch6	ch4				
				H	H	H	ch7	ch5				
L	H	4	3	L	L	–	**ch0	ch0	256K (8 s)	512K (16 s)	1M (32 s)	
				L	H		*ch1	ch1				
				H	L		ch2	ch2				
				H	H		ch3	ch2				
H	L	2		L	–	–	*ch0		512K (16 s)	1M (32 s)	1536K (50 s)	2M (65 s)
				H			ch1					
H	H	1		–	–	–	ch0		1M (32 s)	2M (65 s)	3M (98 s)	4M (131 s)

Note: The number of seconds in parentheses is a recording time measured at f_{sam}=8.0kHz.
The first 8Kbit of the serial voice registers are allocated as a channel index area.
Therefore, the channel memory capacity of channel "0" is 8Kbit less than the value listed in the table above.
1) Number of external serial voice registers
2) When 512Kbit serial voice registers use, only can use (*) (**) mark channel
3) When 256Kbit serial voice regisrers use, only can use (**) mark channel

Allocation for Channel and Channel Memory Capacity in Using 1 Piece of 1M-Bit Serial Voice Register.



Note: By the combination of CSEL1, CSEL2, CA1, CA2 and CA3, the circled channel memory capacities can be allocated as Ch0=16sec., Ch2=8 sec. and Ch3=8 sec. (@f_{sam}=8kHz).

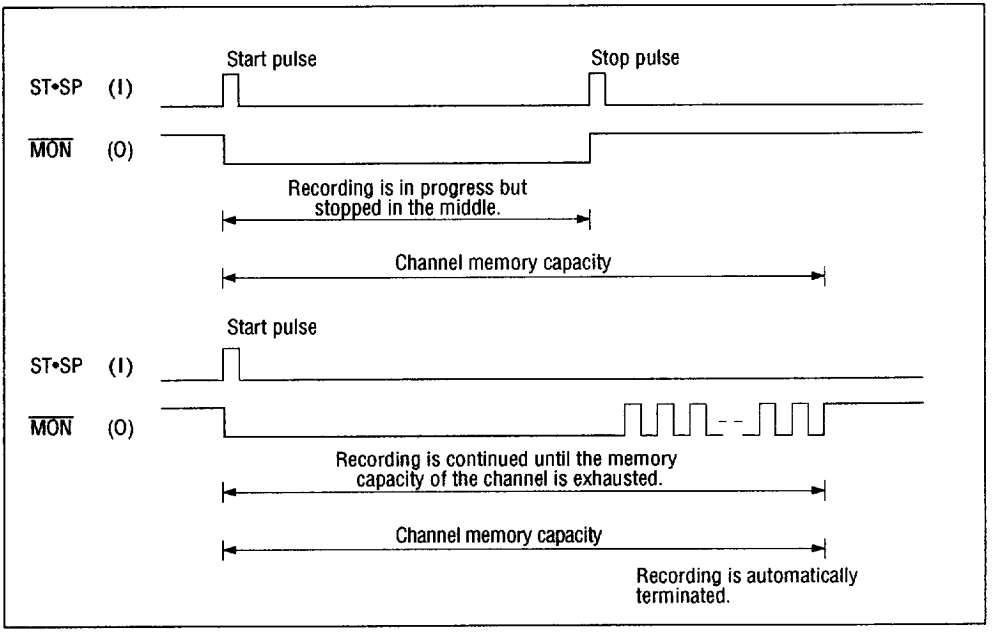
4. Recording

Pull the REC/$\overline{\text{PLAY}}$ pin high. Then, select the number of the phrase to be recorded with the CSEL1 and CSEL2 input pins and select a channel with the CA1 to CA2 input pins.

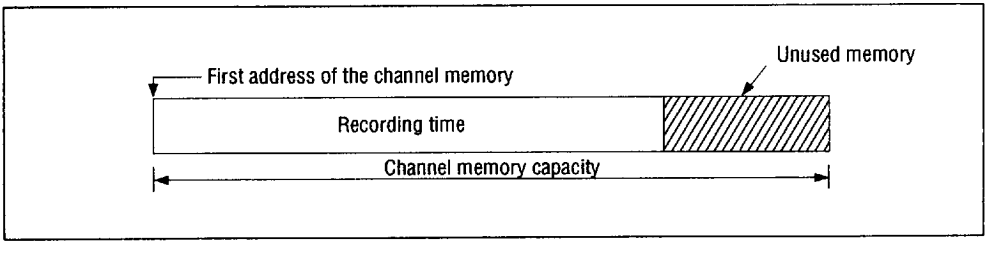
To stop recording in the middle of a phrase, input a pulse to the ST.SP pin again. The recording duration is the time between these two pulses.

When recording is initiated by inputting a pulse to the ST.SP pin, and continued until the memory capacity of the specified channel is exhausted, recording is automatically terminated.

During recording, the $\overline{\text{MON}}$ pin is low.

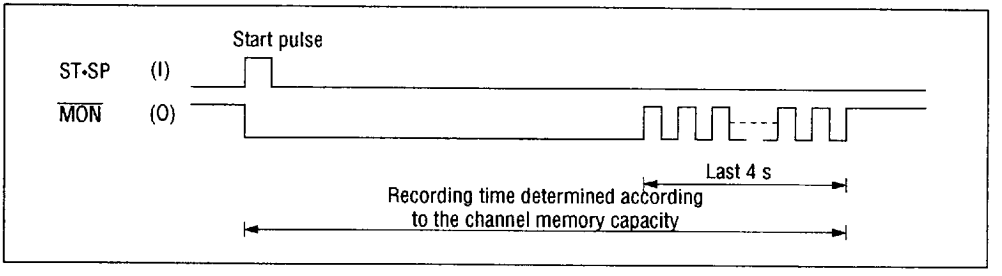


Note: As mentioned above, the memory capacity of the external serial registers is divided by the number of phrases and is assigned as the channel memory capacity. During recording, ADPCM data is written, starting from the first address of the memory of the specified channel. When recording is terminated in the middle of the channel memory capacity by a stop pulse, the subsequent memory area remains unused.



5. Alarm for remaining recording time

When recording is initiated by inputting a pulse to the ST•SP pin and the available recording time reaches the last four seconds, the $\overline{MON}$ pin outputs a 4Hz clock for the last seconds as an "out of available memory" alarm.



Note : During the last four seconds a clock frequency of 4 Hz described above is output, when the sampling frequency (f_{sam}) of 8.0 kHz is selected. The duration of the alarm clock is proportional to the length of the cycle of the sampling frequency and the clock frequency is proportional to the sampling frequency used.

6. Playback

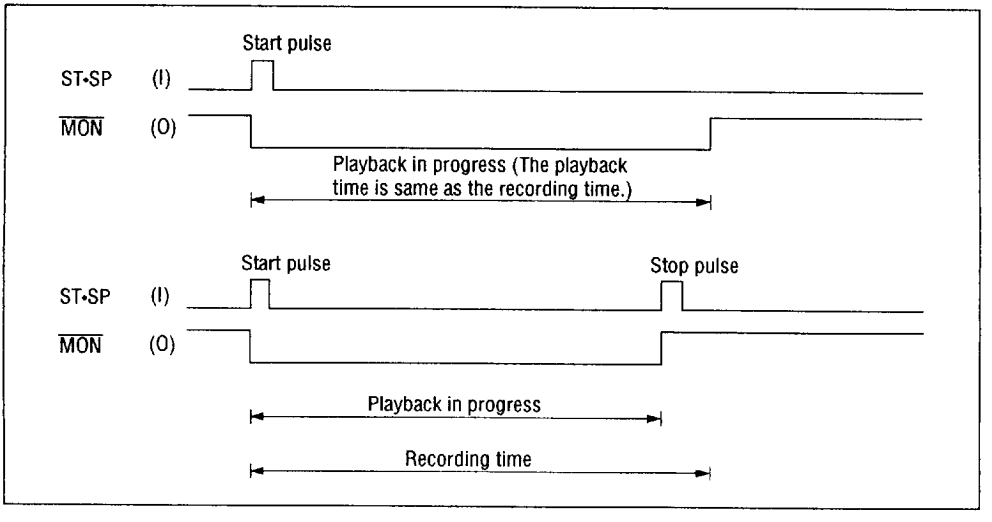
Set the REC/$\overline{PLAY}$ pin low. Then, select the number of the phrase recorded with the CSEL1 and CSEL2 input pins and select a channel with the CA1 to CA3 input pins. To initiate playback, input a pulse to the ST•SP pin. Playback is automatically stopped when the recording time is expired.

To stop playback in the middle of a phrase, input a pulse to the ST•SP pin again.

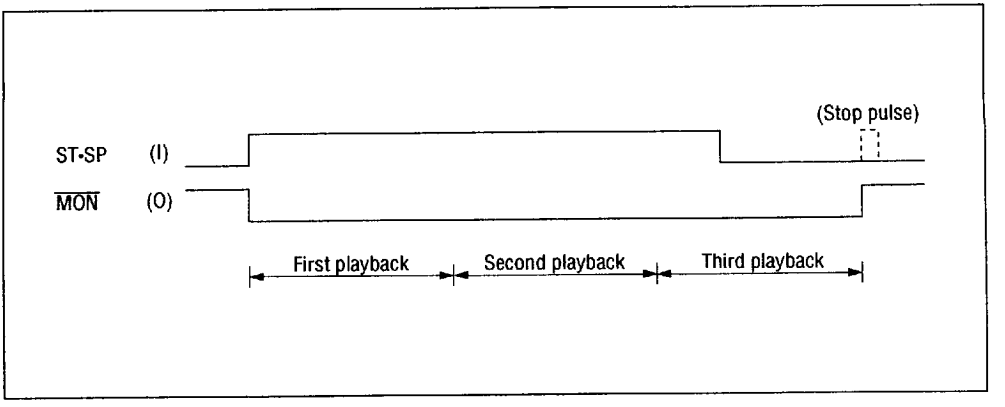
During playback, the $\overline{MON}$ pin is kept low.

Do not start playback in channels not recorded because the playback data and time are undefined.

However, playback under these conditions can be halted by a stop pulse.

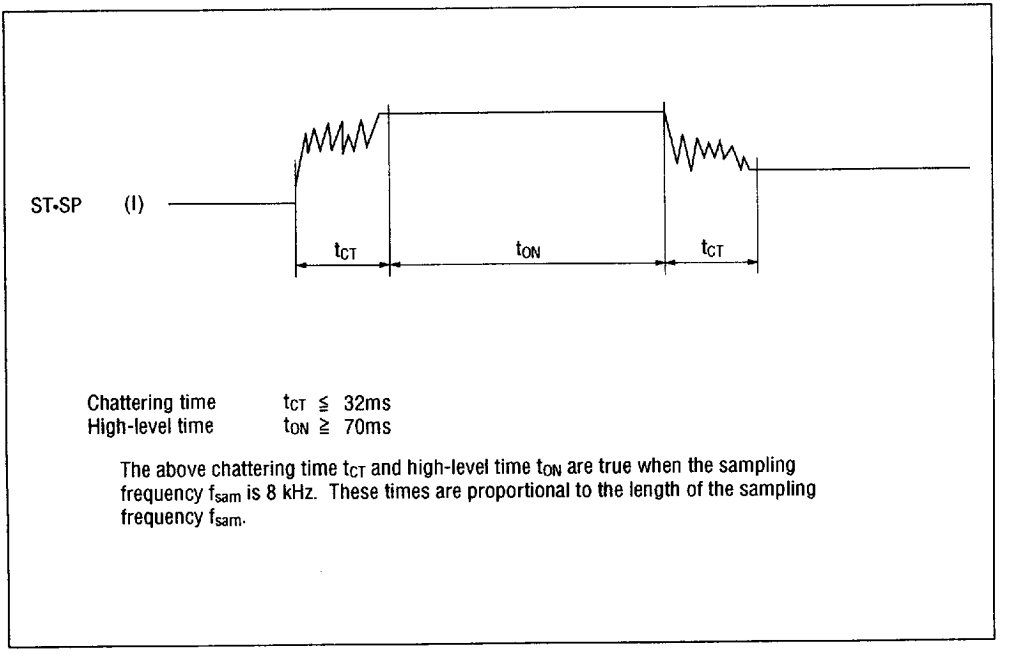


Playback can be repeated by maintaining the ST•SP pin high.



7. Debounce circuit for the ST.SP pin

A debounce circuit functions to prevent the ST.SP pin from malfunctioning due to switch contact bounce. The debounce time is 32 ms. Be sure to set the time during which the ST.SP pin is kept high for at least 70 ms.



Chattering time $t_{CT} \leqq 32ms$
High-level time $t_{ON} \geqq 70ms$

The above chattering time t_{CT} and high-level time t_{ON} are true when the sampling frequency f_{sam} is 8 kHz. These times are proportional to the length of the sampling frequency f_{sam}.

- **Operations in the microcontroller interface application**

The MSM6388 LSI operations are controlled by pins 2VCK, MCK, PD and 16 commands using pins D0 to D3, $\overline{WR}$ and $\overline{RD}$.

1. Explanation of Commands

Command	Code D3	D2	D1	D0	Function
NOP	0	0	0	0	(NON OPERATION) Has no particular function but is used during execution of a EPLAY or EREC command.
INIT	0	0	0	1	(INITIALIZE) • Writes the last address of the external serial voice regisrers as the start and stop addresses of each of channels 0 to 7 to set the channel memory in the unrecorded state. • Sets channel 0 in the channel register.
PLAY	0	0	1	0	(PLAY BACK) Set the playback mode.
REC	0	0	1	1	(RECORD) Set the recording mode.
START	0	1	0	0	(START) Starts recording or playback. At the same time, it writes the start and stop addresses stored in the channel index area into the LSI.
STOP	0	1	0	1	(STOP) Stops recording or playback. When this command is executed during recording, it stores the contents of the address counter at the stop time in the channel index area as the stop address.
SAMP	0	1	1	0	(SAMPLING FREQUENCY) Specifies a sampling frequency together with the next nibble.
CHAN	0	1	1	1	(CHANNEL) Specifies a channel together with the next nibble.
STWR	1	0	0	0	(START ADDRESS WRITE) Stores the start address in the channel index area together with the next three nibbles.
SPWR	1	0	0	1	(STOP ADDRESS WRITE) Stores the stop address in the channel index area together with the next three nibbles.
STRD	1	0	1	0	(START ADDRESS READ) Reads the start address stored in the channel index area through the next three read accesses. During this operation, the contents of the status register cannot be read.
SPRD	1	0	1	1	(STOP ADDRESS READ) Reads the stop address stored in the channel index area through the next three read accesses. During this operation, the contents of the status register cannot be read.

Command	Code D3	D2	D1	D0	Function
DTRD	1	1	0	0	(DATA READ) Reads the contents of external serial voice registers 1K bit sequentially through the data bus on the specified timing. When this command is issued, the LSI enters the playback mode.
DTWR	1	1	0	1	(DATA WRITE) Writes data into external serial voice registers 1Kbit sequentially through the data bus on the specified timing. When this command is issued, the LSI enters the recording mode.
EPLAY	1	1	1	0	(EXTERNAL PLAYBACK) Plays back ADPCM data while reading it from the data bus on the specified timing. When this command is issued, the LSI enters the playback mode.
EREC	1	1	1	1	(EXTERNAL RECORDS) Starts recording and outputs ADPCM data to the data bus on the specified timing. When this command is issued, the LSI enters the recording mode.

- MSM6388 Commands

Command	First nibble command D3	D2	D1	D0	Second nibble command D3	D2	D1	D0	Third nibble command D3	D2	D1	D0	Fourth nibble command D3	D2	D1	D0
NOP	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
INIT	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—
PLAY	0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—
REC	0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—
START	0	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—
STOP	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
SAMP	0	1	1	0	–	S2	S1	S0	—	—	—	—	—	—	—	—
CHAN	0	1	1	1	–	C2	C1	C0	—	—	—	—	—	—	—	—
STWR	1	0	0	0	A3	A2	A1	A0	A7	A6	A5	A4	A11	A10	A9	A8
SPWR	1	0	0	1	A3	A2	A1	A0	A7	A6	A5	A4	A11	A10	A9	A8
STRD	1	0	1	0	A3	A2	A1	A0	A7	A6	A5	A4	A11	A10	A9	A8
SPRD	1	0	1	1	A3	A2	A1	A0	A7	A6	A5	A4	A11	A10	A9	A8
DTRD	1	1	0	0	Operates on the specified timing.											
DTWR	1	1	0	1												
EPLAY	1	1	1	0												
EREC	1	1	1	1												

- Sampling frequency specification (SAMP command)

S2	S1	S0	Sampling frequency		
0	0	0	SA0	$f_{OSC}/576$	(3.6kHz)
0	0	1	SA1	$f_{OSC}/512$	(4.0kHz)
0	1	0	SA2	$f_{OSC}/448$	(4.6kHz)
0	1	1			
1	0	0	SA3	$f_{OSC}/288$	(7.1kHz)
1	0	1	SA4	$f_{OSC}/256$	(8.0kHz)
1	1	0	SA5	$f_{OSC}/224$	(9.1kHz)
1	1	1			

Note: Frequencies in parentheses are used when the oscillator frequency f_{OSC} is 2.048MHz.

- Channel specification

C2	C1	C0	Channel
0	0	0	Ch0
0	0	1	Ch1
0	1	0	Ch2
0	1	1	Ch3
1	0	0	Ch4
1	0	1	Ch5
1	1	0	Ch6
1	1	1	Ch7

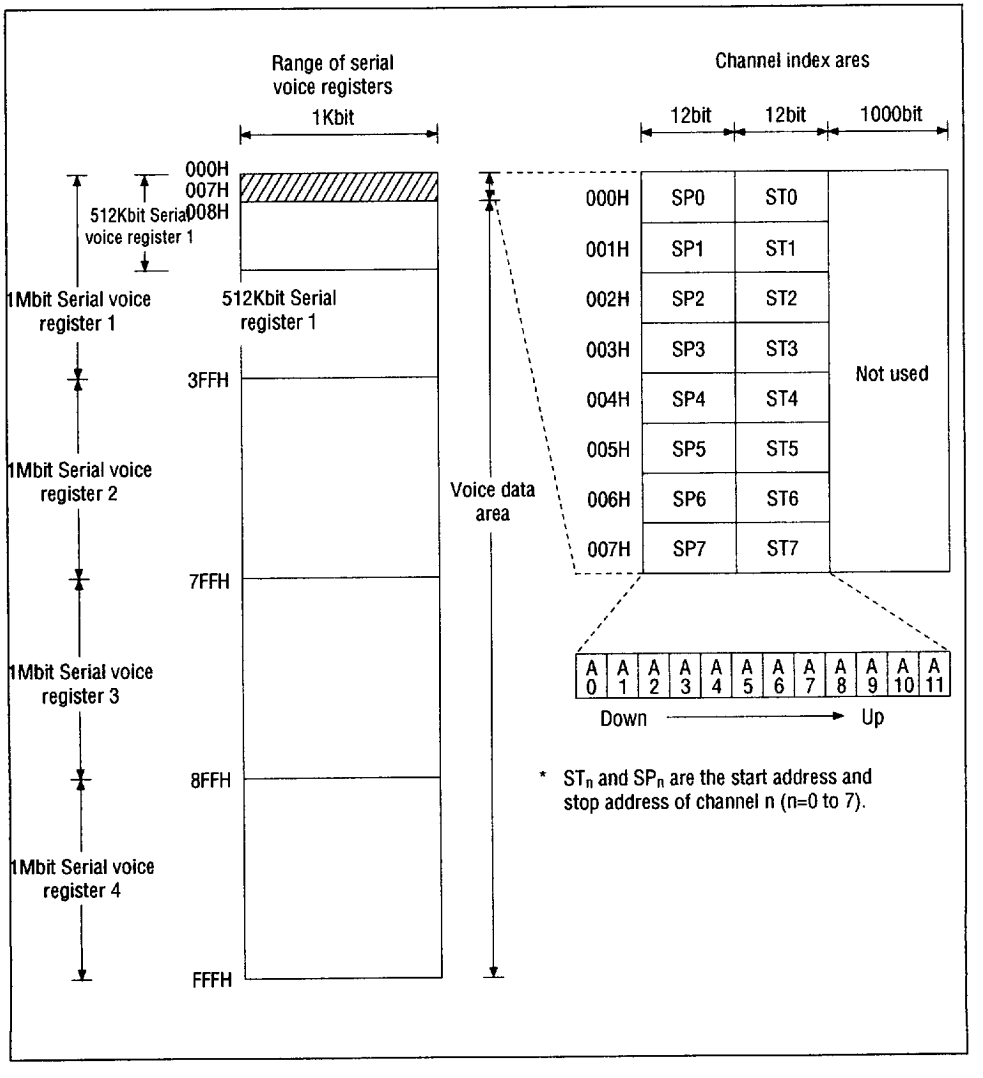
- Start and stop addresses (STWR, SPWR, STRD, and SPRD commands)

The start and stop addresses used to control recording time is managed by 12bit. The available memory capacity varies depending on the number of serial voice registers to be connected externally.

Regardless of the number of serial voice registers, the area between addresses 000H and 007H is allocated as the channel index area to store the start and stop addresses for each channel. The area starting from address 008H can be used to store voice data (ADPCM data).

When on use 512Kbit serial voice register, can use 008H ~ 1FF address.

When on use 256K serical voice register, can use 008H~0FF address.



2. Explanation of the status register

The status register consists of three bits. When a negative-going pulse is supplied to the/RD pin, the status of these bits is output to D0 ~ D2. Note that the status is not output during the execution of an STRD or SPRD command. During execution of a DTRD, DTWR, EPLAY, or EREC command, Status must be read only when the timing is correct.

D3	D2	D1	D0
"L"	DTMNT	RPMNT	BUSY

(1) Busy

The busy bit is high when the LSI is being initialized or when it is executing a command.

When the busy bit is high, do not issue a command from the microcomputer.

BUSY Timing

BUSY conditions		BUSY time max.
NOP, PLAY, REC, START, STOP command		4/f_{sam} (500μs)
INIT command		34/f_{sam} (4.75ms)
SAMP, CHAN command	First nibble	4/f_{sam} (500μs)
	Second nibble	4/f_{sam} (500μs)
STWR, SPWR command	First nibble	6/f_{sam} (750μs)
	After second nibble	4/f_{sam} (500μs)
STRD, SPRD command	First nibble	6/f_{sam} (750μs)
	After second nibble	4/f_{sam} (500μs)

Note: The inside of parentheses shows the time of f_{sam}=8kHz.
BUSY time is porportional to f_{sam} frequency.

(2) RPMNT (Record Playback MoNiTor)

The RPMNT bit is high when the LSI is recording or playing back data. When the RPMNT bit is high, do not input a command except the STOP command.

(3) DTMNT (Data Read Write MoNiTor)

The DTMNT bit is high when data is being transferred to or from serial voice registers by the DTRD or DTWR command.

3. Recording

(1) Sampling frequency select:

To select a sampling frequency fsam, enter a SAMP command.

(2) Channel select:

To select a channel, enter a CHAN command. Usually, specify channel 0.

(3) Start and stop addresses select:

To allocate an area for recording voice data, enter STWR and SPWR commands to store a start address and a stop address in the specified channel field in the channel index area.

(4) To enter the recording mode, enter an REC command.

(5) To start recording, enter a START command. The LSI fetches the start and stop addresses of the specified channel from the channel index area and stores the start address in the address counter and the stop address in the stop address register, then starts recording.

(6) Stopping recording:

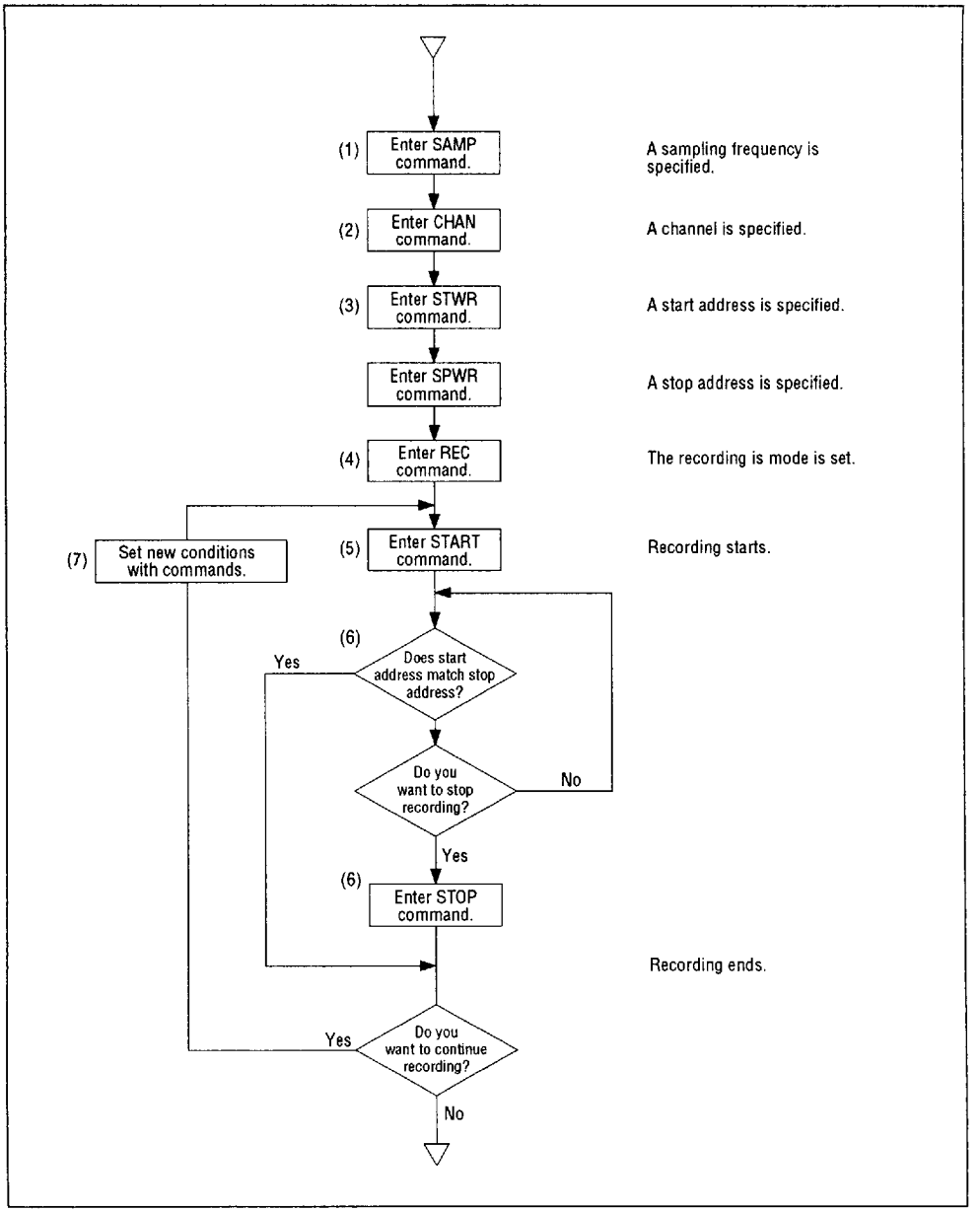
When the contents of the address counter match those of the stop address register, recording is stopped automatically. To stop recording in the middle, enter a STOP command. In this case, the contents of the address counter at recording stop are stored in the channel index area as the stop address.

(7) To resume recording, specify new conditions with commands as described in items (1) to (3) above and follow the procedure described above.

The start and stop address of each channel can be read by STRD and SPRD commands.

When these addresses are controlled by a microcomputer, the memory capacity of external serial voice registers can be used efficiently.

Recording Flowchart when the LSI is Interfaced with a Microcontroller



4. Playback

(1) Sampling frequency select:

To select a sampling frequency, enter a SAMP command.

(2) Channel select:

To select a channel, enter a CHAN command. Usually, specify channel 0.

(3) To enter the playback mode, enter a PLAY command.

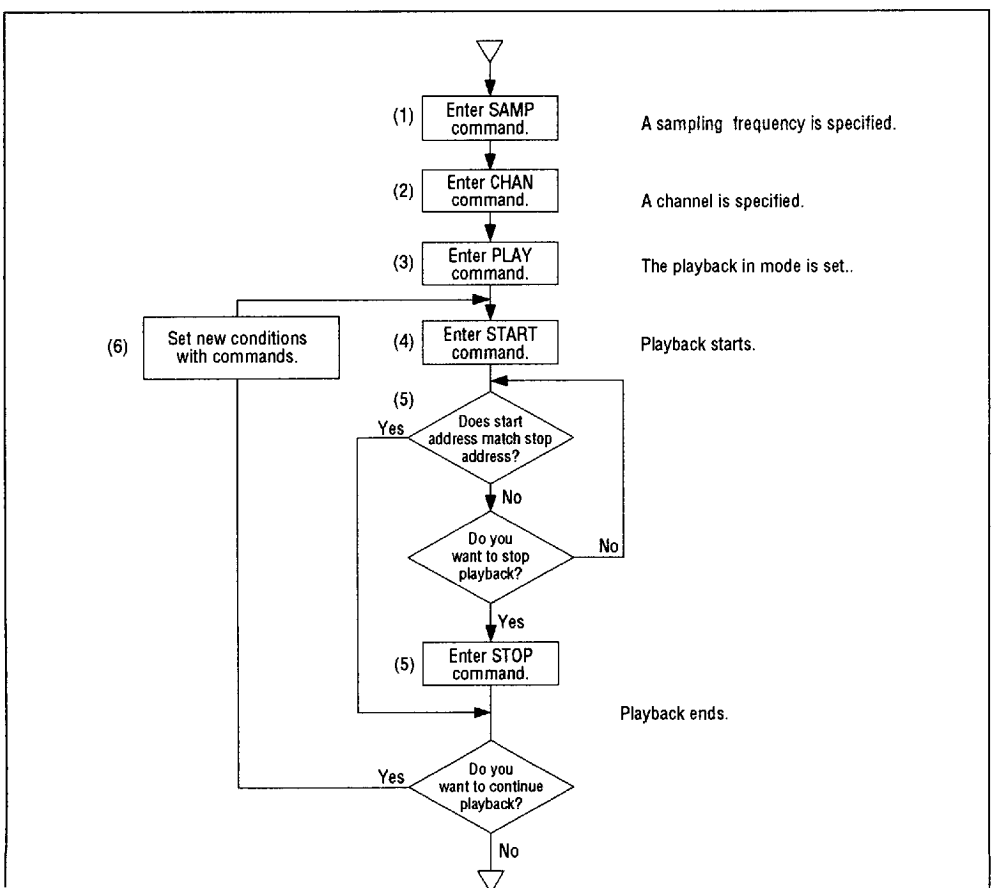
(4) To start playback, enter a START command. The LSI fetches the start and stop addresses of the specified channel index area and then starts playback.

(5) Stopping playback:

When the contents of the address counter match those of the stop address register, playback is stopped automatically. To stop playback in the middle, enter a STOP command.

(6) To resume playback, specify new conditions with commands as described in items (1) and (2) above and follow the procedure described above.

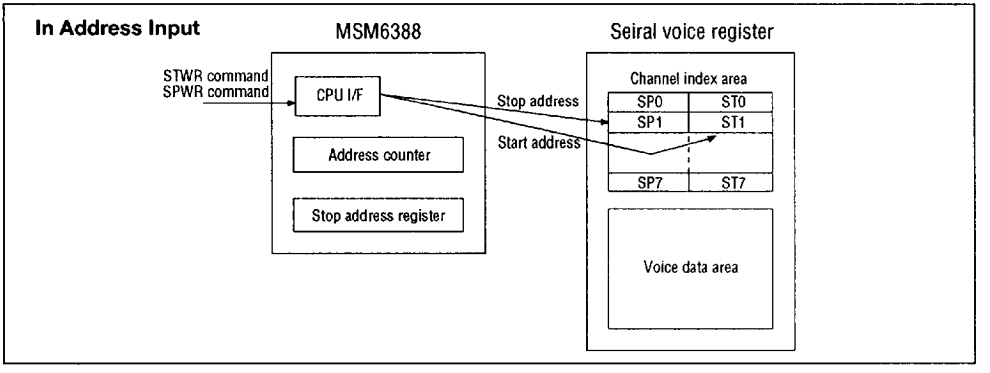
Playback flowchart when the LSI is connected to a microcontroller interface



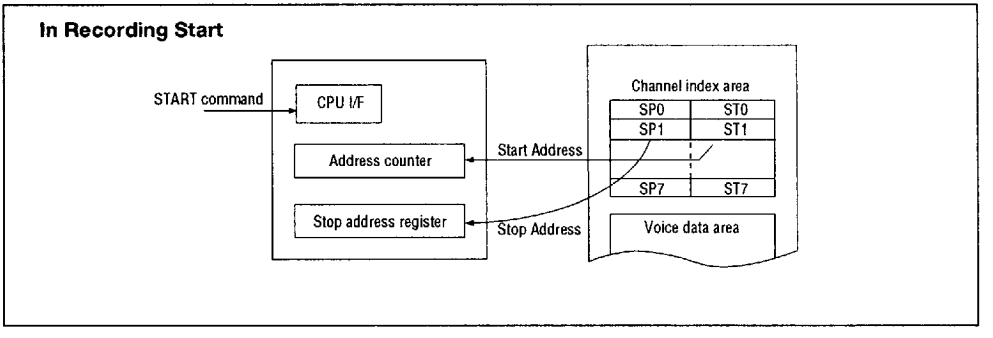
5. Channel Index Area

Operation for channel index area in recording is shown below.

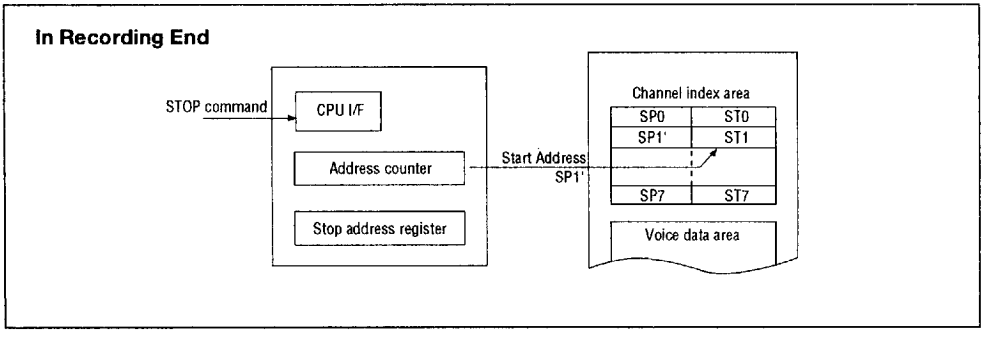
START address and STOP address area written to the channel that designated the channel index area by STWR and SPWR commands.



When START command is inputted, the recording is started after the start addresses of channel index area are automatically set to respective address counter and STOP address register.

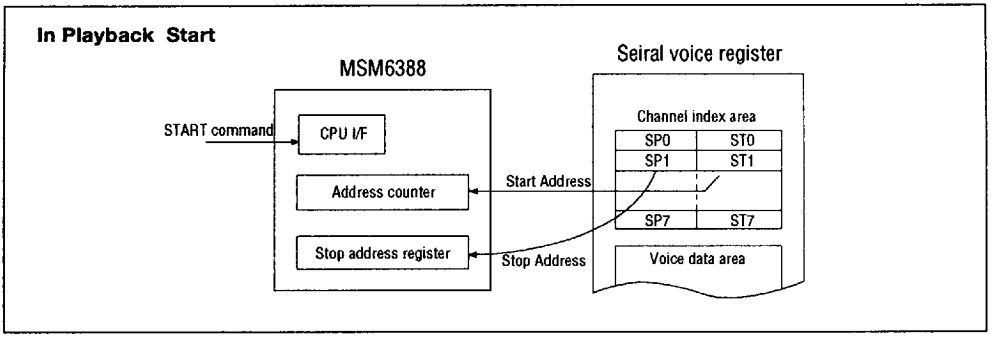


When STOP command is inputted, the contents for the address counter of that time is automatically set to the channel index area as a new STOP address.

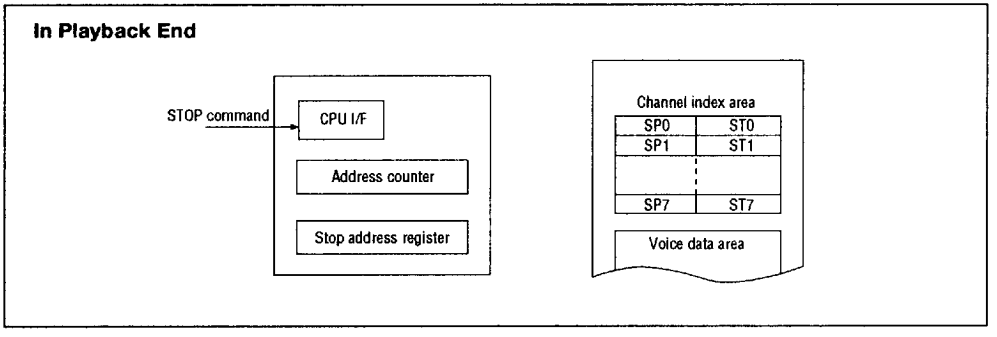


Operation for channel index area in playback is shown below.

When START command is inputted, the playback is started after the START address and STOP address of the channel that designated the channel index area are automatically set to respective address counter and STOP address register.



When STOP command is inputted, the playback finishes. The MSM6388 does not exchange the data with the channel index area.



6. Recording and playback for nine or more channels

When the start and stop addresses of each channel are stored in memory in a microcontroller or external circuitry, recording and playback for nine or more channels is possible. Voice data can be recorded on the same way as for recording described in item 3 above. However, channel 0 must be set.

To play back voice data, enter a STWR command specifying the start address of the voice data area from which to start playback and a SPWR command specifying the stop address of the area to write these addresses in channel 0 field of the channel index area. When a START command is entered, the LSI fetches the start and stop addresses from the channel 0 field in the same way as for playback described in item 4 above, then starts playback.

7. Reading and writing data in external serial voice registers with DTRD and DTWR commands

DTRD and DTWR commands can be used to read from and write to the external serial voice registers.

To read the contents of the serial voice registers, enter an STWR command specifying a start address of the area to be read and an SPWR command specifying a stop address of the area to write these addresses in the channel index area. When a DTRD command is entered, data is read 4bit at a time during each cycle of the sampling frequency.

To write data to the serial voice registers, first write start and stop addresses then enter a DTWR command. Data is written 4bit at a time on the correct RD and WR timings.

Data transfer using DTRD and DTWR commands is performed in 1Kbit units. These two commands can be used to move voice data stored in serial voice registers to different addresses, providing a useful way to use the memory capacity of the serial voice registers.

8. Recording and playing back voice data through the data bus with EREC and EPLAY commands

Specify the sampling frequency with a SAMP command, and input an EREC command.

When an EREC command is entered, the LSI enters the recording mode and recording starts.

Voice data (ADPCM data) is output to the data bus on the correct $\overline{RD}$ and $\overline{WR}$ timings. To stop recording, enter a STOP command on the correct timing.

To perform playback, enter an EPLAY command. The LSI enters the playback mode and starts to play back voice data–the data is input from the data bus on the correct WR timing. To stop playback, enter a STOP command.

During execution of an EREC or EPLAY command, address management and external serial voice register driving are not performed.

9. Initialization by the INIT command

When an INIT command is entered, the channel memory is set in the unrecorded state.

- The INIT command writes the last address of the external serial voice registers as the start and stop addresses in individual fields of channels 0 to 7 in the channel index area. This sets the channel memory in the unrecorded state.
- The command then sets channel 0 in the channel register.

10. Power down function (pin PD)

When pin PD is set at the high level, the LSI enters the power down state. Note that this function is invalid during recording or playback.

- Oscillation is stopped and all operation of the internal circuitry is stopped.
- Data bus pins D0 to D3 are set in the high impedance state.
- Output pins $\overline{CS1}$ to $\overline{CS4}$ are set at the high level, minimizing the current required by the external serial voice registers.

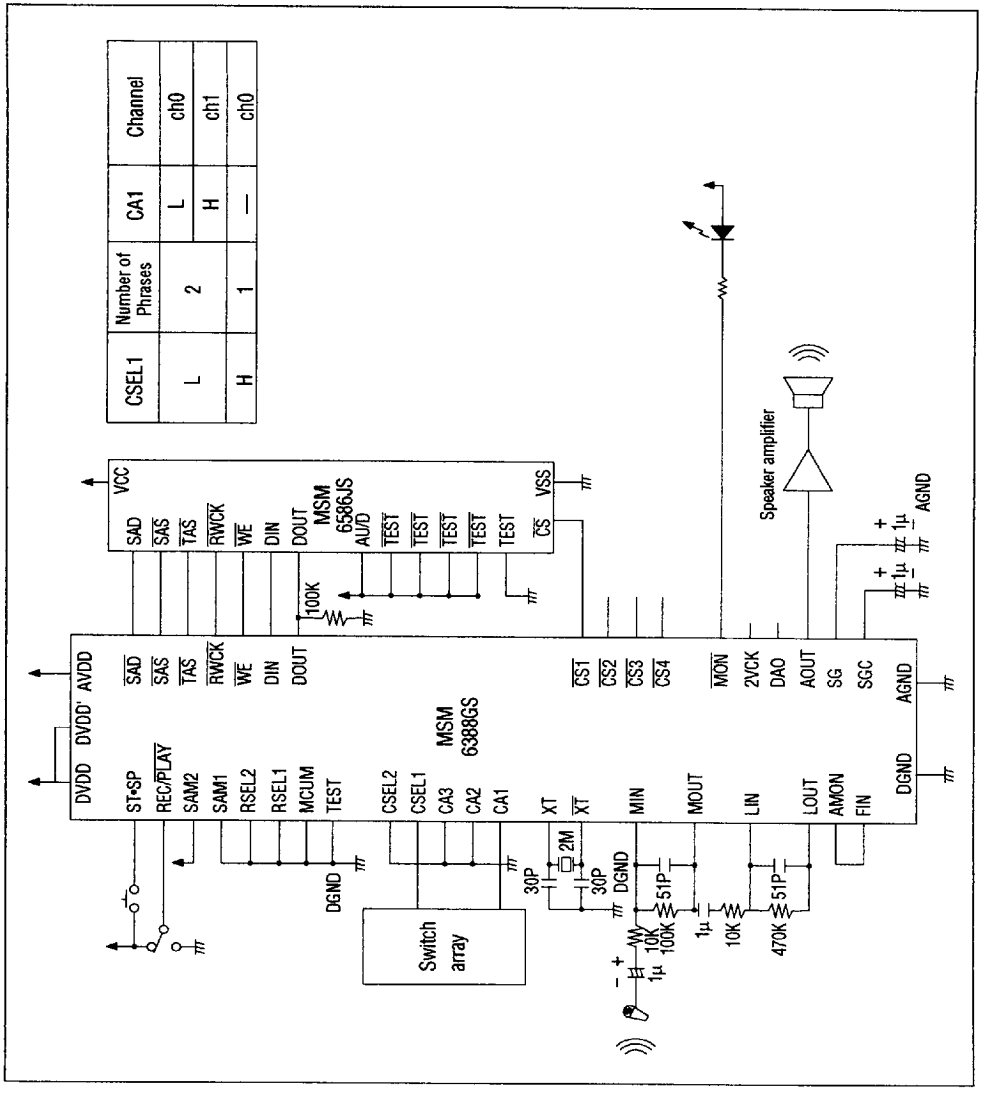
  D0~D3 ..... H~Z
  SAD, $\overline{SAS}$, $\overline{TAS}$, $\overline{WE}$, DIN,
  $\overline{RWCK}$, $\overline{CS1}$~$\overline{CS4}$ ..... "H"
  2VCK, MCK ..... "L"
  AOUT, DAO, SGC ..... GND level

11. Command enable function (pin $\overline{CE}$)

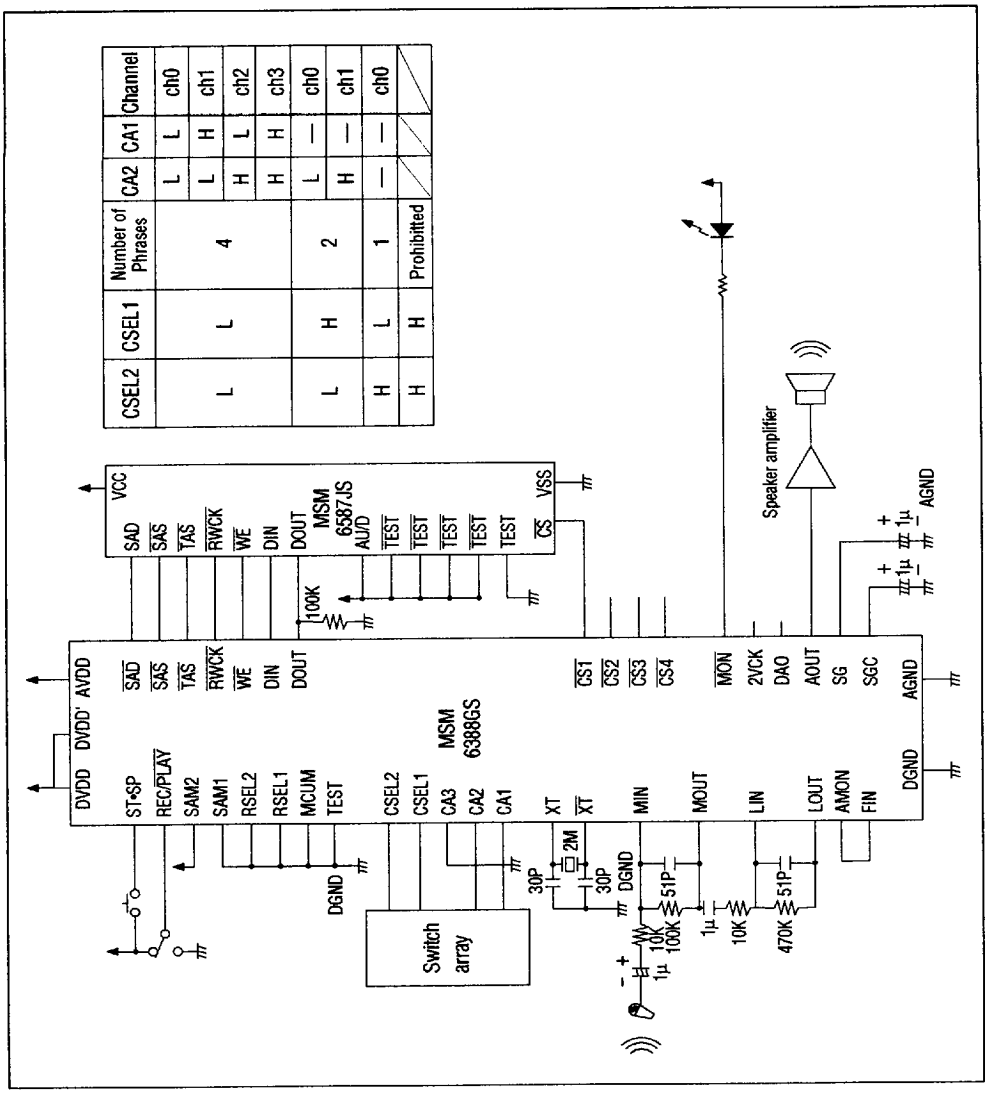
When the pin $\overline{CE}$ is set at the high level, the LSI enters the command enable state, rejecting $\overline{RD}$ and $\overline{WR}$ pulses. In this state, data bus pins D0 to D3 are set in the high impedance state.

SAMPLE APPLICATION CIRCUITS

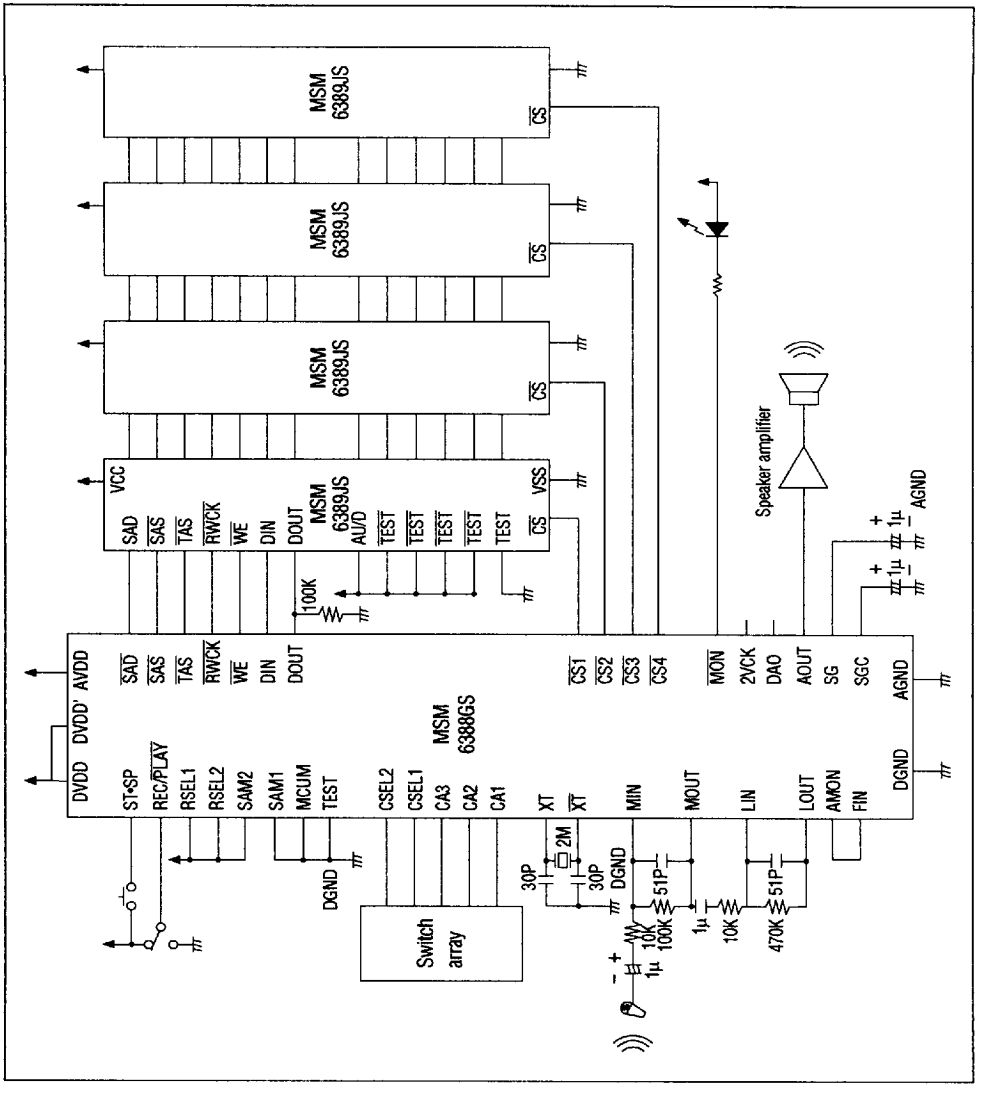
- The circuit diagram 1 shows an example of an application's circuit with the MSM6388 and one 256Kbit serial voice register
- The circuit diagram 2 shows an example of an applications's circuit with the MSM6388 and one 512Kbit serial voice register.
- The circuit diagram 3 shows an example of an application's circuit with the MSM6388 and four 1Mbit serial voice registers.
- Circuit diagram 4 shows an example of the interface with the MSM80C51 when the MSM6388 is used with a microcomputer interface.
- Circuit diagram 5 shows an example of an application using greater than 4-1Mbit serial voice register's with the MSM6388.
- Circuit diagram 6 shows an example of an application's circuit for recording and playback by the EREC and EPLAY commands of the MSM6388.



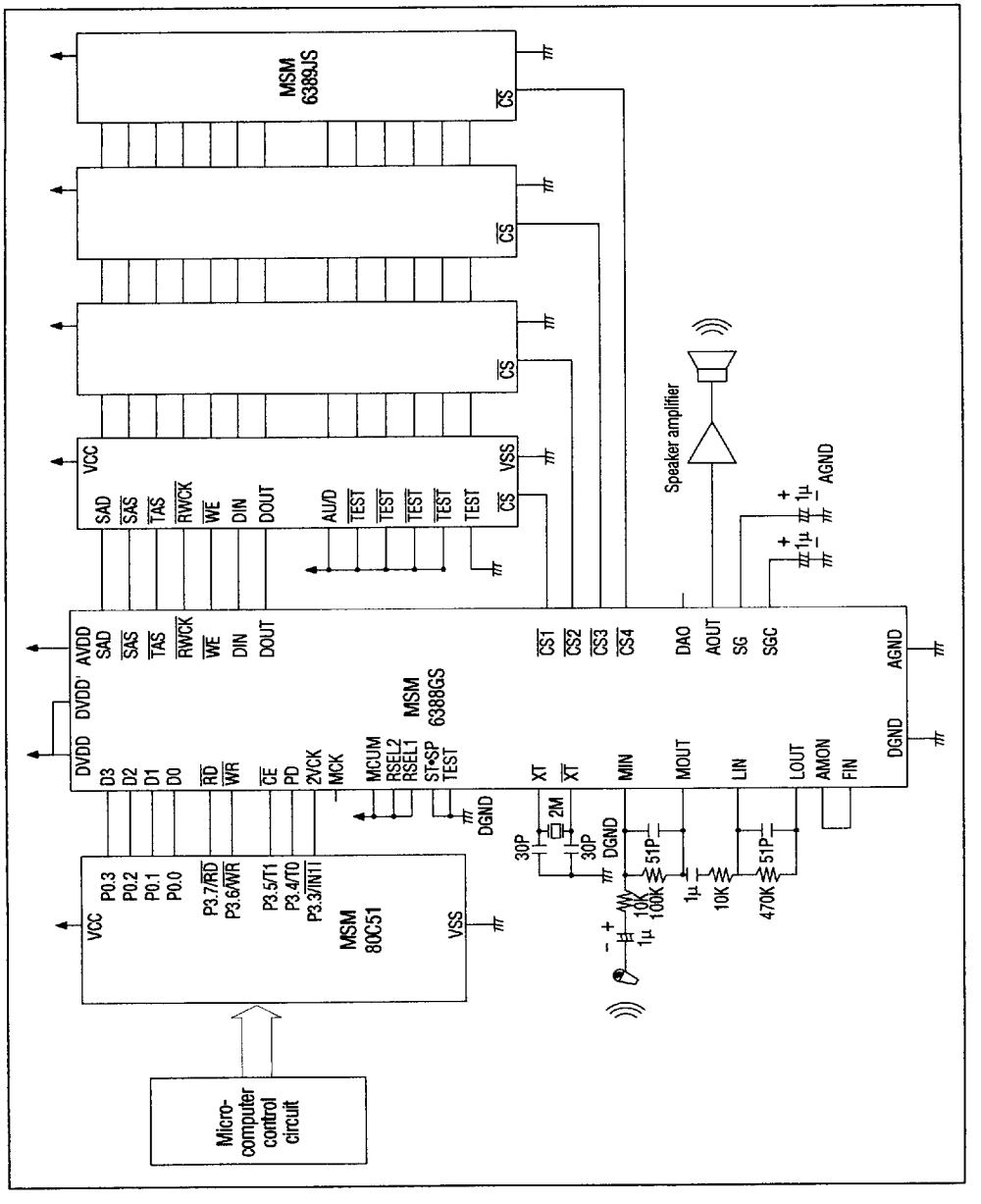
Circuit Diagram 1



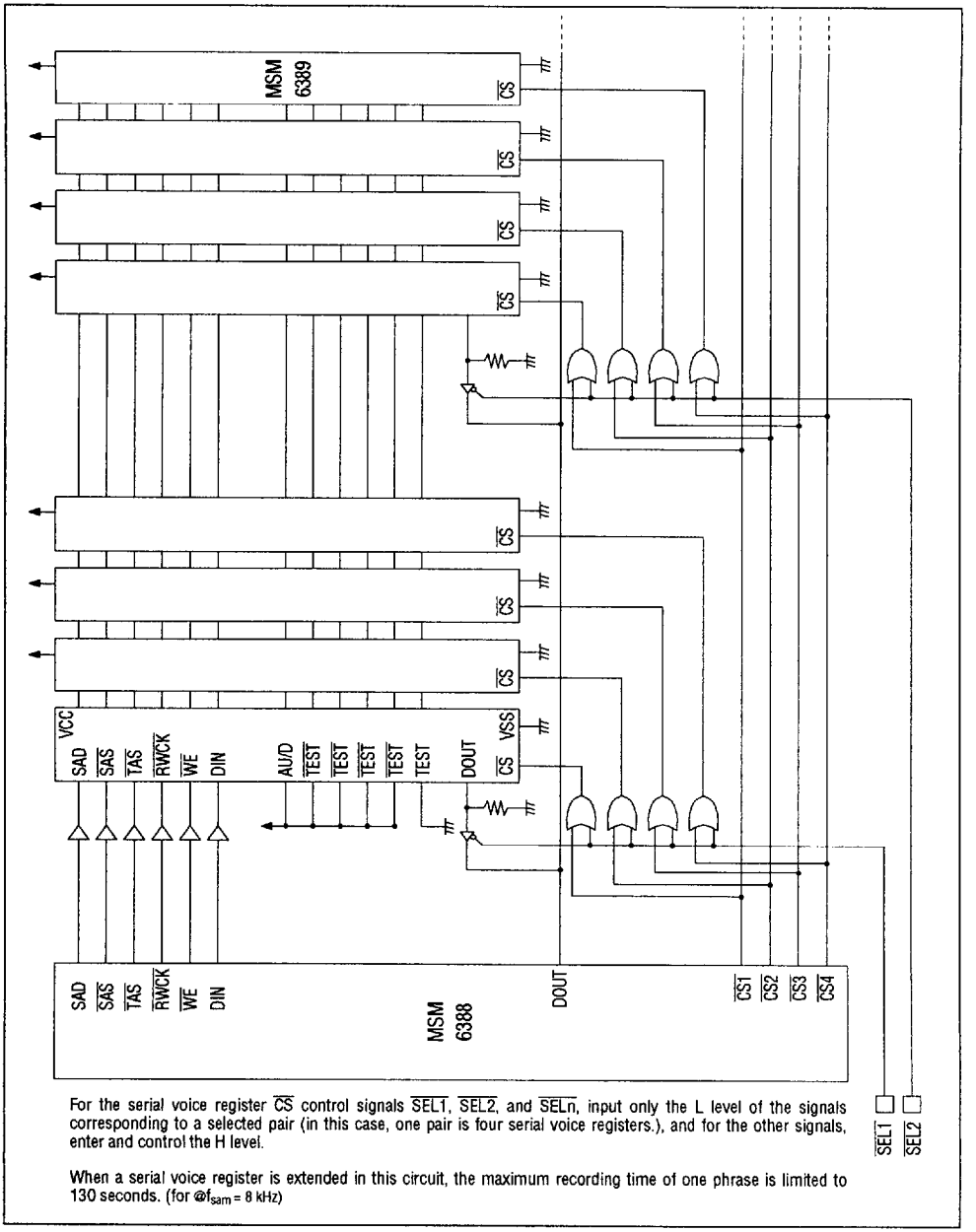
Circuit Diagram 2



Circuit Diagram 3



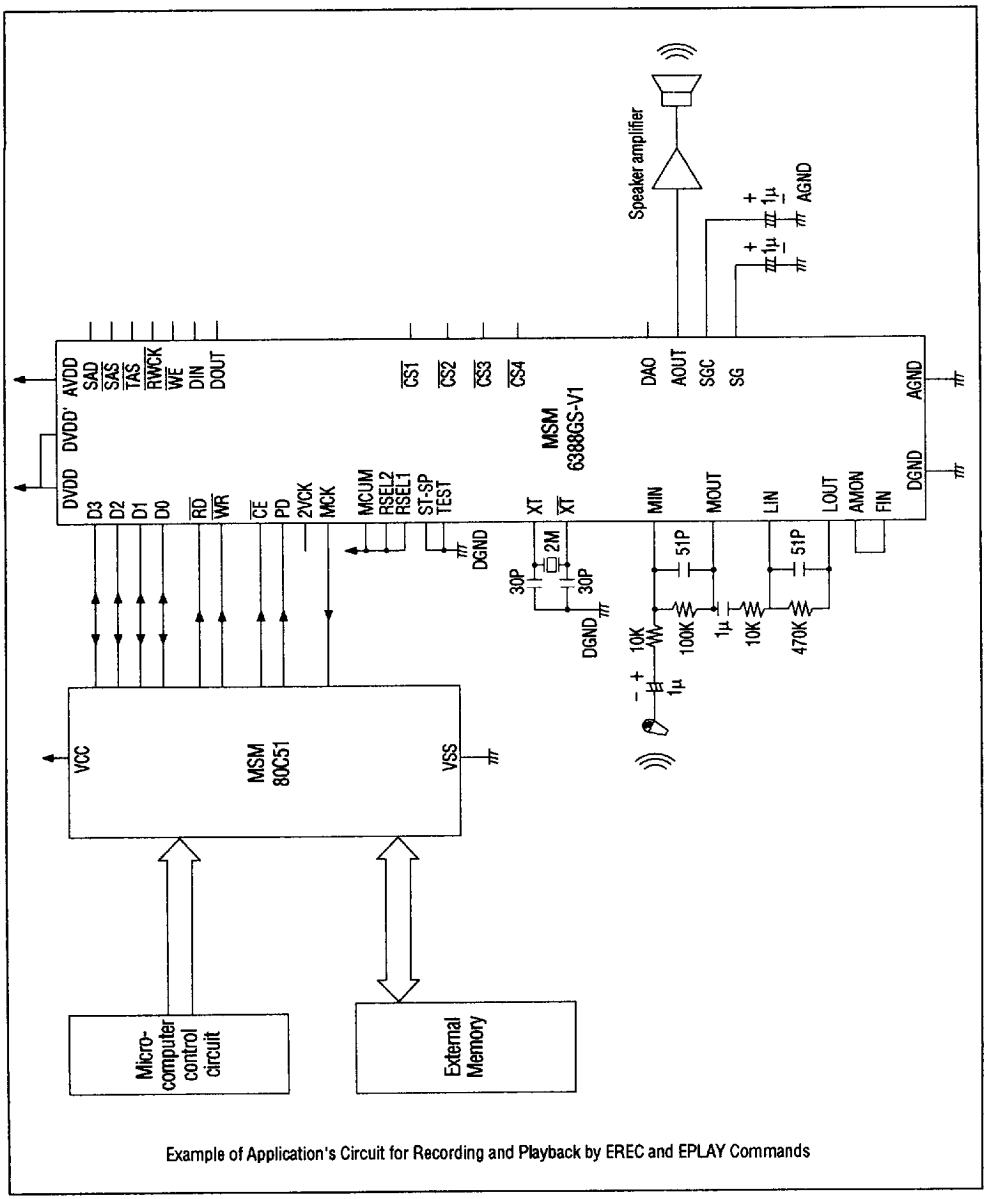
Circuit Diagram 4



For the serial voice register $\overline{CS}$ control signals $\overline{SEL1}$, $\overline{SEL2}$, and $\overline{SELn}$, input only the L level of the signals corresponding to a selected pair (in this case, one pair is four serial voice registers.), and for the other signals, enter and control the H level.

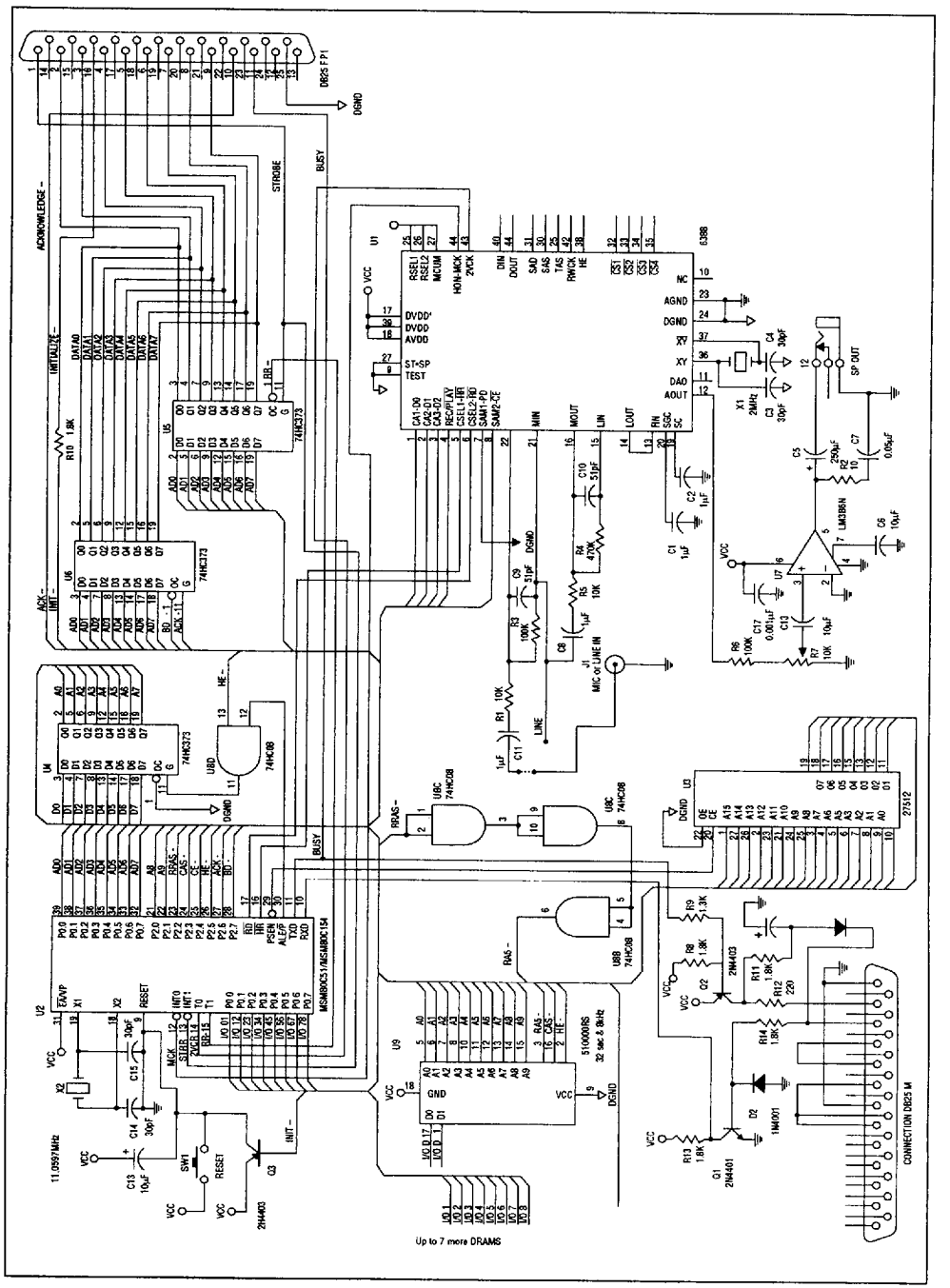
When a serial voice register is extended in this circuit, the maximum recording time of one phrase is limited to 130 seconds. (for @f_{sam} = 8 kHz)

Circuit Diagram 5

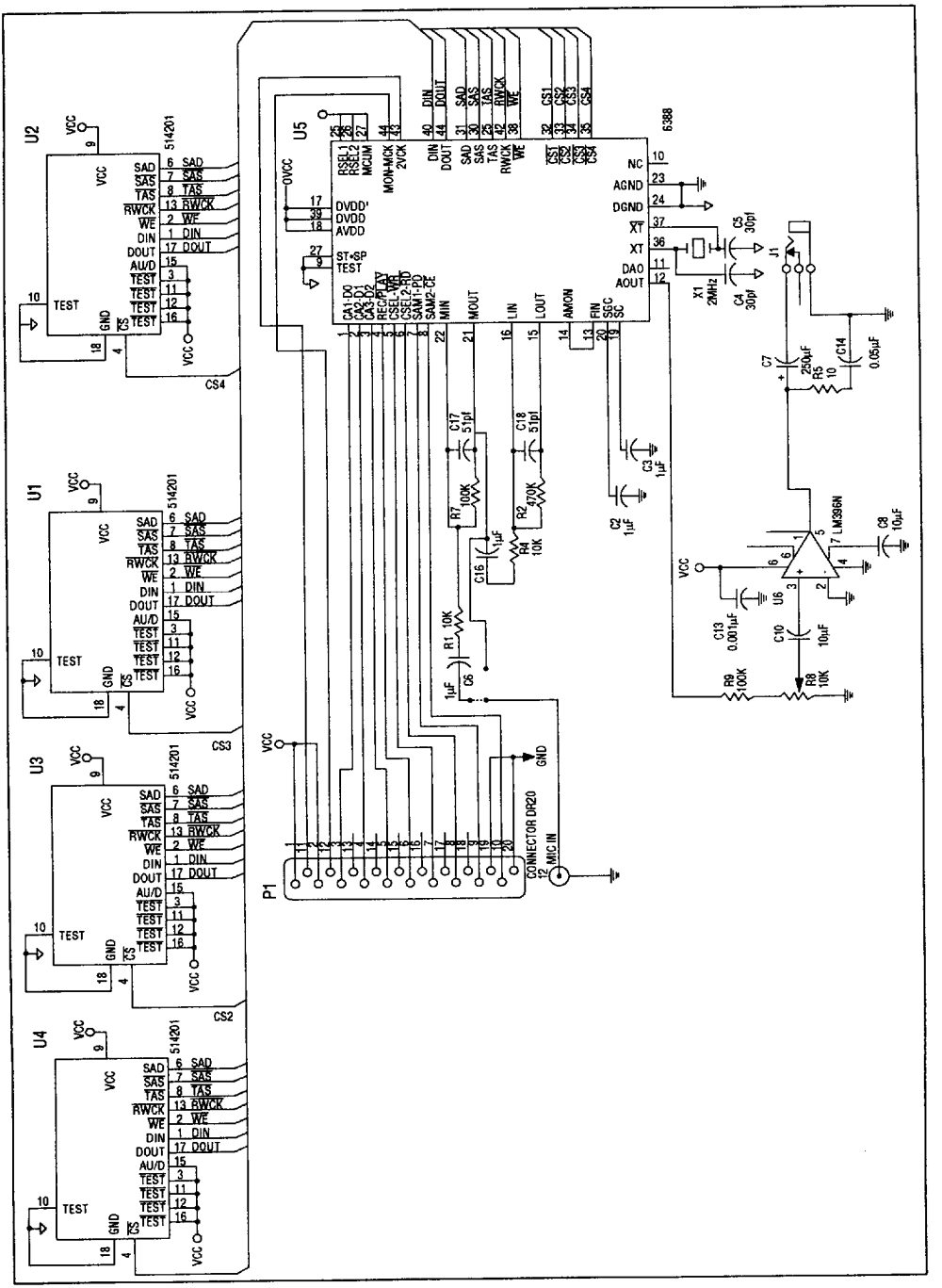


Example of Application's Circuit for Recording and Playback by EREC and EPLAY Commands

Circuit Diagram 6



MSM6388 with 80C154 and DRAMS



MSM6388 Development System