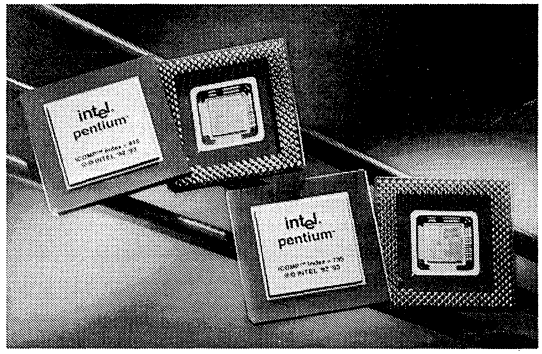
PENTIUM® PROCESSOR at iCOMP® INDEX 610\75 MHz
PENTIUM PROCESSOR at iCOMP INDEX 735\90 MHz
PENTIUM PROCESSOR at iCOMP INDEX 815\100 MHz
PENTIUM PROCESSOR at iCOMP INDEX 1000\120 MHz

- Compatible with Large Software Base
  - MS-DOS‡, Windows‡, OS/2‡, UNIX‡
- 32-Bit CPU with 64-Bit Data Bus
- Superscalar Architecture
  - Two Pipelined Integer Units Are Capable of 2 Instructions/Clock
  - Pipelined Floating Point Unit
- Separate Code and Data Caches
  - 8K Code, 8K Write Back Data
  - MESI Cache Protocol
- Advanced Design Features
  - Branch Prediction
  - Virtual Mode Extensions
- 3.3V BiCMOS Silicon Technology
- 4M Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Dual Processing Configuration
- Multi-Processor Support
  - Multiprocessor Instructions
  - Support for Second Level Cache
- On-Chip Local APIC Controller
  - MP Interrupt Management
  - 8259 Compatible
- Internal Error Detection Features
- Upgradable with a Future Pentium® OverDrive® Processor
- Power Management Features
  - System Management Mode
  - Clock Control
- Fractional Bus Operation
  - 120-MHz Core/60-MHz Bus
  - 100-MHz Core/66-MHz Bus
  - 100-MHz Core/50-MHz Bus
  - 90-MHz Core/60-MHz Bus
  - 75-MHz Core/50-MHz Bus

The Pentium® processor 75/90/100/120 extends the Pentium processor family, providing performance needed for mainstream desktop applications as well as for workstations and servers. The Pentium processor is compatible with the entire installed base of applications for DOS, Windows, OS/2, and UNIX. The Pentium processor 75/90/100/120 superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. The pipelined floating point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor 75/90/100/120 has 3.3 million transistors and is built on Intel's advanced 3.3V BiCMOS silicon technology. The Pentium processor 75/90/100/120 has on-chip dual processing support, a local multiprocessor interrupt controller, and SL power management features.



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†Since publication of documents referenced in this document, registration of the Pentium, OverDrive, and iCOMP trademarks has been issued to Intel Corporation.

March 1995 Order Number: 241997-004

PENTIUM® PROCESSOR at iCOMP® INDEX 610\75 MHz
PENTIUM PROCESSOR at iCOMP INDEX 735\90 MHz
PENTIUM PROCESSOR at iCOMP INDEX 815\100 MHz
PENTIUM PROCESSOR at iCOMP INDEX 1000\120 MHz

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1.0 MICROPROCESSOR ARCHITECTURE OVERVIEW

The Pentium® processor at iCOMP® rating 610\75 MHz, iCOMP rating 735\90 MHz, and iCOMP rating 815\100 MHz extends the Intel Pentium family of microprocessors. It is 100% binary compatible with the 8086/88, 80286, Intel386™ DX CPU, Intel386 SX CPU, Intel486™ DX CPU, Intel486 SX CPU, Intel486 DX2 CPUs, and Pentium processor at iCOMP Index 510\60 MHz and iCOMP Index 567\66 MHz.

The Pentium processor family consists of the Pentium processor at iCOMP rating 610\75 MHz, iCOMP rating 735\90 MHz, and iCOMP rating 815\100 MHz (product order code 80502), described in this document, and the original Pentium processor 60/66 (order code 80501). The name "Pentium processor 75/90/100/120" will be used in this document to refer to the Pentium processor at iCOMP rating 610\75 MHz, iCOMP rating 735\90 MHz, iCOMP rating 815\100 MHz and iCOMP rating 1000\120 MHz. Also, the name "Pentium processor 60/66" will be used to refer to the original 60- and 66-MHz version product.

The Pentium processor family architecture contains all of the features of the Intel486 CPU family, and provides significant enhancements and additions including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 8K Code and 8K Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Functional Redundancy Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions

In addition to the features listed above, the Pentium processor 75/90/100/120 offers the following enhancements over the Pentium processor 60/66:

- iCOMP performance rating of 1000 at 120 MHz in single processor configuration
- iCOMP performance rating of 815 at 100 MHz in single processor configuration
- iCOMP performance rating of 735 at 90 MHz in single processor configuration
- iCOMP performance rating of 610 at 75 MHz in single processor configuration
- Dual processing support
- SL power management features
- Upgradable with a Future Pentium OverDrive® processor
- Fractional bus operation
- On-chip local APIC device

1.1 Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of CPUs.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the BTB so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 CPU. Faster algorithms provide up to 10X speed-up for common operations including add, multiply, and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache is 8 Kbytes in size, with a 32-byte line size and is 2-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be write back or write through on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst write back cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' Memory Management Unit contains optional extensions to the architecture which allow 2-Mbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking, and internal parity checking features have been added along with a new exception, the machine check exception. In addition, the Pentium processors have implemented functional redundancy checking to provide maximum error detection of the processor and the interface to the processor. When functional redundancy checking is used, a second processor, the "checker" is used to execute in lock step with the "master" processor. The checker samples the master's outputs and compares those values with the values it computes internally, and asserts an error signal if a mismatch occurs.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified 4 breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 shows a block diagram of the Pentium processor 75/90/100/120.

For Pentium Processor (610\75) designs which use the TCP package, Intel document 242323 must be referenced for correct TCP pinout, mechanical, thermal, and AC specifications.

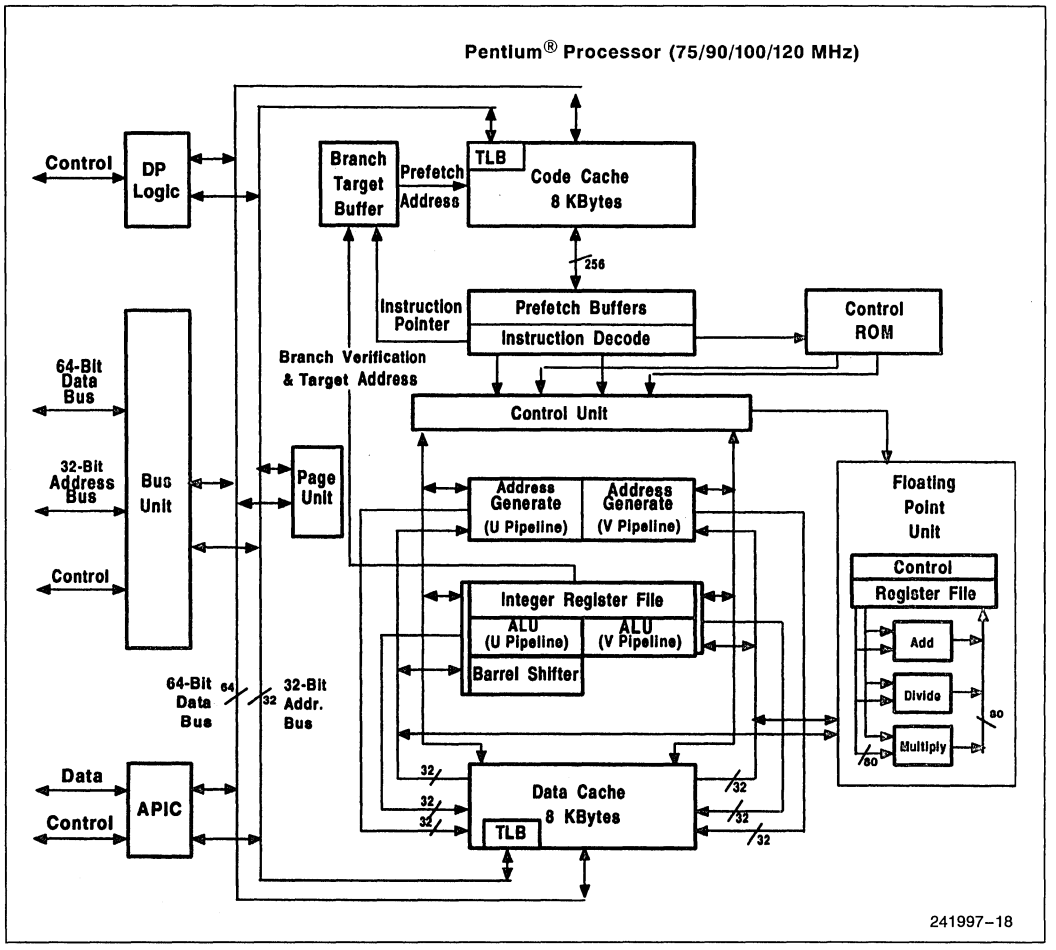


Figure 1. Pentium® Processor Block Diagram

The block diagram shows the two instruction pipelines, the "u" pipe and the "v" pipe. The u-pipe can execute all integer and floating point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate caches are shown, the code cache and data cache. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processors can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that

must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

The architectural features introduced in this chapter are more fully described in the *Pentium™ Family User's Manual.*

1.2 Pentium® Processor 75/90/100/120

In addition to the architecture described above for the Pentium processor family, the Pentium processor 75/90/100/120 has additional features which are described in this section.

The Pentium processor 75/90/100/120 offers higher performance and higher operating frequencies than the Pentium processor 60/66. The 120-MHz version of the Pentium processor 75/90/100/120 offers core operation at 120 MHz, external bus interface at 60 MHz, and achieves an iCOMP index of 1000, while the 100-MHz version of the Pentium processor 75/90/100/120 offers core operation at 100 MHz, external bus interface at 50 or 66 MHz, and achieves an iCOMP index of 815, while the 90-MHz version offers core operation at 90 MHz, external bus interface at 60 MHz, and achieves an iCOMP index of 735, and the Pentium processor 75/90/100/120 core operates at 75 MHz and the external bus operates at 50 MHz.

Symmetric dual processing in a system is supported with two Pentium processors 75/90/100/120. The two processors appear to the system as a single Pentium processor 75/90/100/120. Operating systems with dual processing support properly schedule computing tasks between the two processors. This scheduling of tasks is transparent to software applications and the end-user. Logic built into the processors support a "glueless" interface for easy system design. Through a private bus, the two Pentium processors 75/90/100/120 arbitrate for the external bus and maintain cache coherency. **Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.**

In this document, in order to distinguish between two Pentium processors 75/90/100/120 in dual processing mode, one CPU will be designated as the Primary processor with the other being the Dual processor. Note that this is a different concept than that of "master" and "checker" processors described above in the discussion on functional redundancy.

Due to the advanced 3.3V BiCMOS process that it is produced on, the Pentium processor 75/90/100/120 dissipates less power than the Pentium processor 60/66. In addition to the SMM features described above, the Pentium processor 75/90/100/120 supports clock control. When the clock to the Pentium processor 75/90/100/120 is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the Pentium processor 75/90/100/120 a good choice for energy-efficient desktop designs.

Supporting an upgrade socket (Socket 5) in the system will provide end-user upgradability by the addition of a Future Pentium OverDrive processor. Typical applications will realize a 40%–70% performance increase by addition of a Future Pentium OverDrive processor.

The Pentium processor 75/90/100/120 supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies. The external bus frequency operates at a selectable one-half or two-thirds fraction of the internal core frequency.

The Pentium processor 75/90/100/120 contains an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

2.0 PINOUT

2.1 Pinout and Pin Descriptions

2.1.1 PENTIUM® PROCESSOR 75/90/100/120 PINOUT

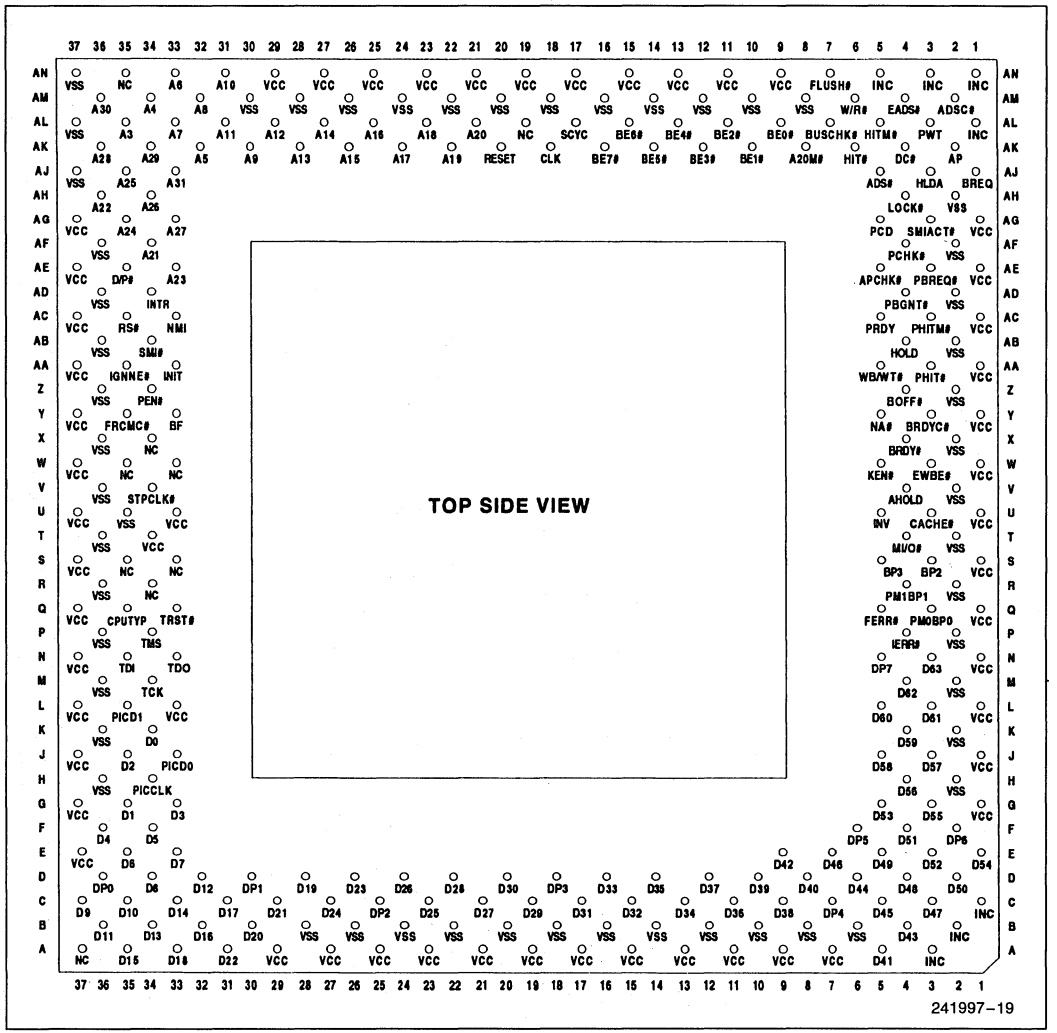


Figure 2. Pentium® Processor 75/90/100/120 Pinout (Top Side View)

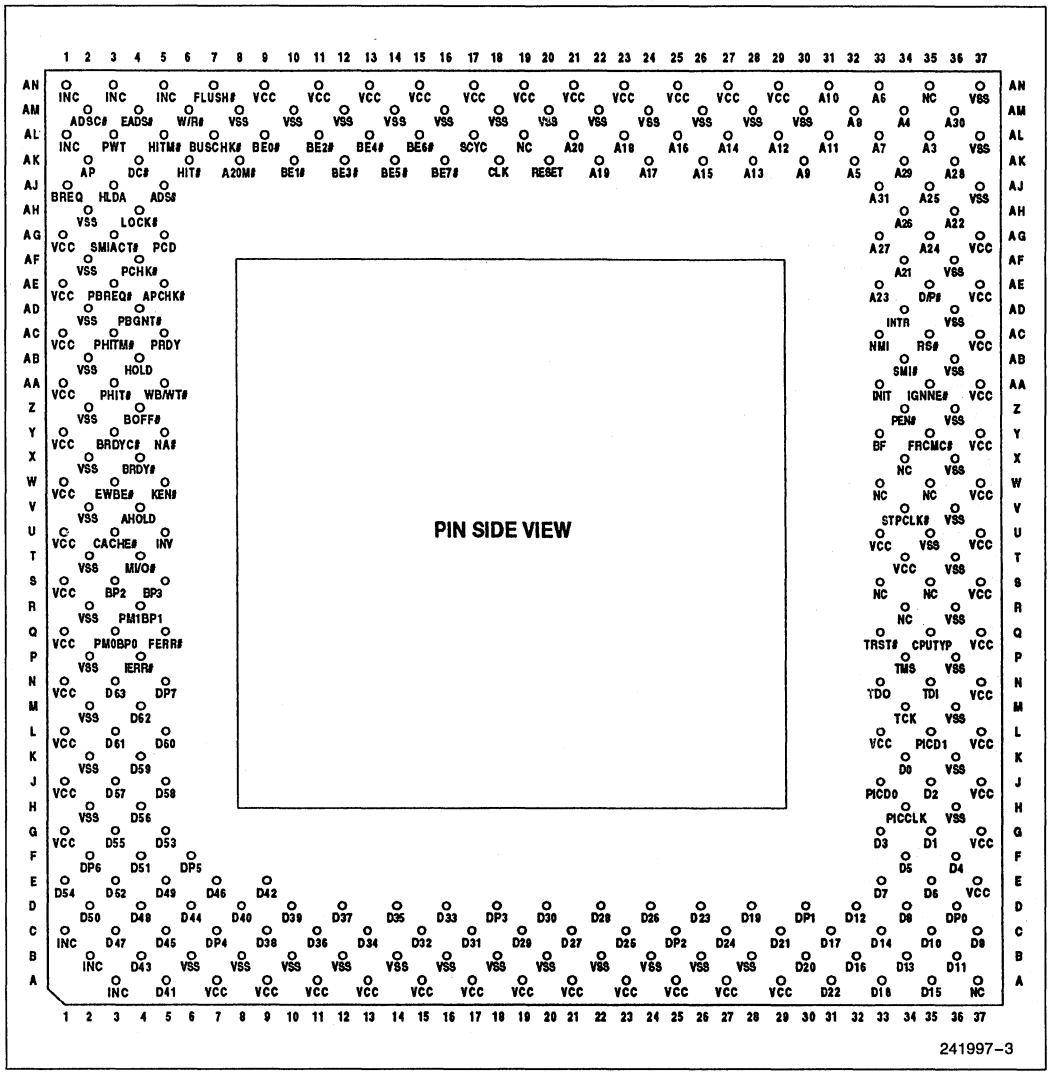


Figure 3. Pentium® Processor 75/90/100/120 (Pin Side View)

2.1.2 PIN CROSS REFERENCE TABLE FOR PENTIUM® PROCESSOR 75/90/100/120

Table 1. Pin Cross Reference by Pin Name

Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 1. Pin Cross Reference by Pin Name (Contd.)

Control							
A20M#	AK08	BRDYC#	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	FRCMC#	Y35	PM0/BP0	Q03
ADSC#	AM02	BUSCHK#	AL07	HIT#	AK06	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HITM#	AL05	PRDY	AC05
AP	AK02	CPUTYP	Q35	HLDA	AJ03	PWT	AL03
APCHK#	AE05	D/C#	AK04	HOLD	AB04	R/S#	AC35
BE0#	AL09	D/P#	AE35	IERR#	P04	RESET	AK20
BE1#	AK10	DP0	D36	IGNNE#	AA35	SCYC	AL17
BE2#	AL11	DP1	D30	INIT	AA33	SMI#	AB34
BE3#	AK12	DP2	C25	INTR/LINT0	AD34	SMIACT#	AG03
BE4#	AL13	DP3	D18	INV	U05	TCK	M34
BE5#	AK14	DP4	C07	KEN#	W05	TDI	N35
BE6#	AL15	DP5	F06	LOCK#	AH04	TDO	N33
BE7#	AK16	DP6	F02	M/IO#	T04	TMS	P34
BOFF#	Z04	DP7	N05	NA#	Y05	TRST#	Q33
BP2	S03	EADS#	AM04	NMI/LINT1	AC33	W/R#	AM06
BP3	S05	EWBE#	W03	PCD	AG05	WB/WT#	AA05
BRDY#	X04	FERR#	Q05	PCHK#	AF04		

APIC		Clock Control		Dual Processor Private Interface	
PICCLK	H34	CLK	AK18	PBGNT#	AD04
PICD0	J33	[BF]	Y33	PBREQ#	AE03
[DPEN#]		STPCLK#	V34	PHIT#	AA03
PICD1	L35			PHITM#	AC03
[APICEN]					

Table 1. Pin Cross Reference by Pin Name (Contd.)

V_{CC}								
A07	A19	E37	L33	S01	W01	AC01	AN09	AN21
A09	A21	G01	L37	S37	W37	AC37	AN11	AN23
A11	A23	G37	N01	T34	Y01	AE01	AN13	AN25
A13	A25	J01	N37	U01	Y37	AE37	AN15	AN27
A15	A27	J37	Q01	U33	AA01	AG01	AN17	AN29
A17	A29	L01	Q37	U37	AA37	AG37	AN19	

V_{SS}						
B06	B22	M02	U35	AB36	AM08	AM24
B08	B24	M36	V02	AD02	AM10	AM26
B10	B26	P02	V36	AD36	AM12	AM28
B12	B28	P36	X02	AF02	AM14	AM30
B14	H02	R02	X36	AF36	AM16	AN37
B16	H36	R36	Z02	AH02	AM18	
B18	K02	T02	Z36	AJ37	AM20	
B20	K36	T36	AB02	AL37	AM22	

NC/INC						
A03	C01	S35	W35	AL01	AN01	AN05
A37	R34	W33	X34	AL19	AN03	AN35
B02	S33					

2.2 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active HIGH inputs should be connected to GND.

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

2.3 Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the "Hardware Interface" chapter in the *Pentium™† Family User's Manual,* Volume 1. **Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior.**

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

The following pins exist on the Pentium processor 60/66 but have been removed from the Pentium processor 75/90/100/120:

- IBT, IU, IV, BT0-3

The following pins become I/O pins when two Pentium processors 75/90/100/120 are operating in a dual processing environment:

- ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC

Table 2. Quick Pin Reference

Symbol	Type*	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor 75/90/100/120 emulates the address wraparound at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the Pentium processor 75/90/100/120 masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the Pentium processor 75/90/100/120 when configured as a Dual processor.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the Pentium processor 75/90/100/120.
ADSC#	O	ADSC# is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold,** the Pentium processor 75/90/100/120 will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium processor 75/90/100/120 with even parity information on all Pentium processor 75/90/100/120 generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium processor 75/90/100/120 during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium processor 75/90/100/120.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium processor 75/90/100/120 has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** is a new pin that enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the **Programmable Interrupt Controller Data** 1 signal.
BE7#-BE5# BE4#-BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Unlike the Pentium processor 60/66, the lower 4-byte enables (BE3#-BE0#) are used on the Pentium processor 75/90/100/120 as APIC ID inputs and are sampled at RESET. After RESET, these behave exactly like the Pentium processor 60/66 byte enables. In dual processing mode, BE4# is used as an input during Flush cycles.

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
[BF]	I	**Bus Frequency** determines the bus-to-core frequency ratio. BF is sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF must not change values while RESET is active. For proper operation of the Pentium processor 75/90/100/120 this pin should be strapped high or low. When BF is strapped to V_{CC}, the processor will operate at a 2/3 bus/core frequency ratio. When BF is strapped to V_{SS}, the processor will operate at a 1/2 bus/core frequency ratio. If BF is left floating, the Pentium processor 75/90/100/120 defaults to a 2/3 bus ratio. Note that core operation at either 75 MHz or 90 MHz does not allow 1/2 bus/core frequency, while core operation at 120 MHz does not allow 2/3 bus core frequency.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium processor 75/90/100/120 will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor 75/90/100/120 restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium processor 75/90/100/120 data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	This signal has the same functionality as BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium processor 75/90/100/120 has internally generated a bus request. This signal is always driven whether or not the Pentium processor 75/90/100/120 is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor 75/90/100/120 will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor 75/90/100/120. will vector to the machine check exception.
CACHE#	O	For Pentium processor 75/90/100/120-initiated cycles the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor 75/90/100/120 will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
CLK	I	The **clock** input provides the fundamental timing for the Pentium processor 75/90/100/120. Its frequency is the operating frequency of the Pentium processor 75/90/100/120 external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK. **NOTE:** **It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to ensure long-term reliability of the device.**
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the Pentium processor 75/90/100/120 is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC}. For the Future Pentium OverDrive processor, CPUTYP will be used to determine whether the bootup handshake protocol will be used (in a dual socket system) or not (in a single socket system).
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor 75/90/100/120 with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor 75/90/100/120 on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor 75/90/100/120. DP7 applies to D63-56, DP0 applies to D7-0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if Socket 5 is occupied. DPEN# shares a pin with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium processor 75/90/100/120 address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium processor 75/90/100/120 generates a write, and EWBE# is sampled inactive, the Pentium processor 75/90/100/120 will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
FERR#	O	The **floating point error** pin is driven active when an unmasked floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# is never driven active by the Dual processor.
FLUSH#	I	When asserted, the **cache flush** input forces the Pentium processor 75/90/100/120 to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium processor 75/90/100/120 indicating completion of the write back and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered. If two Pentium processors 75/90/100/120 are operating in dual processing mode in a system and FLUSH# is asserted, the Dual processor will perform a flush first (without a flush acknowledge cycle), then the Primary processor will perform a flush followed by a flush acknowledge cycle.
FRCMC#	I	The **functional redundancy checking master/checker** mode input is used to determine whether the Pentium processor 75/90/100/120 is configured in master mode or checker mode. When configured as a master, the Pentium processor 75/90/100/120 drives its output pins as required by the bus protocol. When configured as a checker, the Pentium processor 75/90/100/120 tristates all outputs (except IERR# and TDO) and samples the output pins. The configuration as a master/checker is set after RESET and may not be changed other than by a subsequent RESET.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor 75/90/100/120 data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium processor 75/90/100/120 cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor 75/90/100/120 has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor 75/90/100/120 will resume driving the bus. If the Pentium processor 75/90/100/120 has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
HOLD	I	In response to the **bus hold request,** the Pentium processor 75/90/100/120 will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor 75/90/100/120 will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium processor 75/90/100/120 will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. If a parity error occurs on a read from an internal array, the Pentium processor 75/90/100/120 will assert the IERR# pin for one clock and then shutdown. If the Pentium processor 75/90/100/120 is configured as a checker and a mismatch occurs between the value sampled on the pins and the corresponding value computed internally, the Pentium processor 75/90/100/120 will assert IERR# two clocks after the mismatched value is returned.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor 75/90/100/120 will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor 75/90/100/120 will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor 75/90/100/120 will stop execution and wait for an external interrupt. IGNNE# is internally masked when the Pentium processor 75/90/100/120 is configured as a Dual processor.
INIT	I	The Pentium processor 75/90/100/120 **initialization** input pin forces the Pentium processor 75/90/100/120 to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the Pentium processor 75/90/100/120 will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor 75/90/100/120 will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized. If the local APIC is enabled, this pin becomes **local interrupt 0.**

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium processor 75/90/100/120 generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LINT0/INTR	I	If the APIC is enabled, this pin is **local interrupt 0.** If the APIC is disabled, this pin is **interrupt.**
LINT1/NMI	I	If the APIC is enabled, this pin is **local interrupt 1.** If the APIC is disabled, this pin is **non-maskable interrupt.**
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor 75/90/100/120 will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one o f the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor 75/90/100/120 will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium processor 75/90/100/120 supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. If the local APIC is enabled, this pin becomes **local interrupt 1.**
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processors 75/90/100/120 are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor 75/90/100/120 exists in a system.
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processors 75/90/100/120 are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor 75/90/100/120 exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors 75/90/100/120 are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor 75/90/100/120 will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the Pentium processor 75/90/100/120 will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processors 75/90/100/120 are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected if only one Pentium processor 75/90/100/120 exists in a system.
PHITM#	I/O	**Private modified hit** is a hit indication used when two Pentium processors 75/90/100/120 are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one Pentium processor 75/90/100/120 exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor 75/90/100/120.
PICD0-1 [DPEN#] [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium processor 75/90/100/120 comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals share pins with DPEN# and APICEN.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
R/S#	I	The **run/stop** input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	**RESET** forces the Pentium processor 75/90/100/120 to begin execution at a known state. All the Pentium processor 75/90/100/120 internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH#, FRCMC# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor 75/90/100/120 thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium processor 75/90/100/120 will still respond to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the Pentium processor 75/90/100/120 boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium processor 75/90/100/120 during boundary scan.

Table 2. Quick Pin Reference (Contd.)

Symbol	Type*	Name and Function
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium processor 75/90/100/120 on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor 75/90/100/120 on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC}	I	The Pentium processor 75/90/100/120 has 53 3.3V **power** inputs.
V_{SS}	I	The Pentium processor 75/90/100/120 has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

* The pins are classified as Input or Output based on their function in Master Mode. See the Functional Redundancy Checking section in the "Error Detection" chapter of the *Pentium™ Family User's Manual,* Vol. 1, for further information.

2.4 Pin Reference Tables

Table 3. Output Pins

Name	Active Level	When Floated
ADS#*	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#*	Low	Bus Hold, BOFF#
D/P#**	n/a	
FERR#**	Low	
HIT#*	Low	
HITM#*	Low	
HLD A*	High	
IERR#	Low	
LOCK#*	Low	Bus Hold, BOFF#
M/IO#*, D/C#*, W/R#*	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC*	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:
All output and input/output pins are floated during tristate test mode and checker mode (except IERR#).
* These are I/O signals when two Pentium® processors 75/90/100/120 are operating in dual processing mode.
** These signals are undefined when the CPU is configured as a Dual Processor.

Table 4. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#*	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
CPUTYP	High	Synchronous/RESET		
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
FRCMC#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#*	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pullup	
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

* Undefined when the CPU is configured as a Dual processor.

Table 5. Input/Output Pins

Name	Active Level	When Floated	Qualified (when an input)	Internal Resistor
A31-A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#-BE0#	Low	Address Hold, Bus Hold, BOFF#	RESET	Pulldown*
D63-D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7-DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTES:
All output and input/output pins are floated during tristate test mode (except TDO) and checker mode (except IERR# and TDO).
* BE3#-BE0# have Pulldowns during RESET only.

Table 6. Inter-Processor I/O Pins

Name	Active Level	Internal Resistor
PHIT#	Low	Pullup
PHITM#	Low	Pullup
PBGNT#	Low	Pullup
PBREQ#	Low	Pullup

NOTE:
For proper inter-processor operation, the system cannot load these signals.

2.5 Pin Grouping According to Function

Table 7 organizes the pins with respect to their function.

Table 7. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT
Address Bus	A31-A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0-1
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
Functional Redundancy Checking	FRCMC# (IERR#)
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Probe Mode	R/S#, PRDY

3.0 ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium processor 60/66 and the Pentium processor 75/90/100/120 and the DC and AC specifications.

3.1 Electrical Differences Between Pentium® Processor 75/90/100/120 and Pentium Processor 60/66

Pentium® Processor 60/66 Electrical Characteristic	Difference in Pentium Processor 75/90/100/120
5V Power Supply	3.3V Power Supply*
5V TTL Inputs/Outputs	3.3V Inputs/Outputs
Pentium Processor 60/66 Buffer Models	Pentium Processor 75/90/100/120 Buffer Models

* The upgrade socket specifies two 5V inputs (section 6.0.).

The sections that follow will briefly point out some ways to design with these electrical differences.

3.1.1 3.3V POWER SUPPLY

The Pentium processor 75/90/100/120 has all V_{CC} 3.3V inputs. By connecting all Pentium processor 60/66 V_{CC} inputs to a common and dedicated power plane, that plane can be converted to 3.3V for the Pentium processor 75/90/100/120.

The CLK and PICCLK inputs can tolerate a 5V input signal. This allows the Pentium processor 75/90/100/120 to use 5V or 3.3V clock drivers.

3.1.2 3.3V INPUTS AND OUTPUTS

The inputs and outputs of the Pentium processor 75/90/100/120 are 3.3V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the 3.3V V_{IN} max.

For Pentium processor 75/90/100/120 outputs, if the Pentium processor 60/66 system support components use TTL-compatible inputs, they will interface to the Pentium processor 75/90/100/120 without extra logic. This is because the Pentium processor 75/90/100/120 drives according to the 5V TTL specification (but not beyond 3.3V).

For Pentium processor 75/90/100/120 inputs, the voltage must not exceed the 3.3V V_{IH3} maximum specification. System support components can consist of 3.3V devices or open-collector devices. 3.3V support components may interface to the Pentium processor 60/66 since they typically meet 5V TTL specifications. In an open-collector configuration, the external resistor may be biased with the CPU V_{CC}; as the CPU's V_{CC} changes from 5V to 3.3V, so does this signal's maximum drive.

The CLK and PICCLK inputs of the Pentium processor 75/90/100/120 are 5V tolerant, so they are electrically identical to the Pentium processor 60/66 clock input. This allows a Pentium processor 60/66 clock driver to drive the Pentium processor 75/90/100/120.

All pins, other than the CLK and PICCLK inputs, are 3.3V-only. If an 8259A interrupt controller is used, for example, the system must provide level converters between the 8259A and the Pentium processor 75/90/100/120.

3.1.3 3.3V PENTIUM® PROCESSOR 75/90/100/120 BUFFER MODELS

The structure of the buffer models of the Pentium processor 75/90/100/120 are the same as those of the Pentium processor 60/66, but the values of the components change since the Pentium processor 75/90/100/120 buffers are 3.3V buffers on a different process.

Despite this difference, the simulation results of Pentium processor 75/90/100/120 buffers and Pentium processor 60/66 buffers look nearly identical. Since the 0pF AC specifications of the Pentium processor 75/90/100/120 are derived from the Pentium processor 60/66 specifications, the system should see little difference between the AC behavior of the Pentium processor 75/90/100/120 and the Pentium processor 60/66.

To meet specifications, simulate the AC timings with Pentium processor 75/90/100/120 buffer models. Pay special attention to the new signal quality restrictions imposed by 3.3V buffers.

3.2 Absolute Maximum Ratings

The values listed below are stress ratings only. Functional operation at the maximums is not implied or guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor 75/90/100/120 contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Case temperature under bias ..... −65°C to 110°C

Storage temperature ..... −65°C to 150°C

3V Supply voltage with respect to V_{SS} ..... −0.5V to +4.6V

3V Only Buffer DC Input Voltage −0.5V to V_{CC} +0.5; not to exceed V_{CC3} max(2)

5V Safe Buffer DC Input Voltage ..... −0.5V to 6.5V(1,3)

NOTES:

1. Applies to CLK and PICCLK.
2. Applies to all Pentium processor 75/90/100/120 inputs except CLK and PICCLK.
3. See overshoot/undershoot transient spec.

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

3.3 DC Specifications

Tables 8, 9, and 10 list the DC specifications which apply to the Pentium processor 75/90/100/120. The Pentium processor 75/90/100/120 is a 3.3V part internally. The CLK and PICCLK inputs may be a 3.3V or 5V inputs. Since the 3.3V (5V-safe) input levels defined in Table 9 are the same as the 5V TTL levels, the CLK and PICCLK inputs are compatible with existing 5V clock drivers. The power dissipation specification in Table 11 is provided for design of thermal solutions during operation in a sustained maximum level. This is the worst case power the device would dissipate in a system. This number is used for design of a thermal solution for the device.

Table 8. 3.3V DC Preliminary Specifications

T_{CASE} = 0 to 70°C; V_{CC} = 3.3V +5%

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	−0.3	0.8	V	TTL Level(3)
V_{IH3}	Input High Voltage	2.0	V_{CC}+0.3	V	TTL Level(3)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level(1, 3)
V_{OH3}	Output High Voltage	2.4		V	TTL Level(2, 3)
I_{CC3}	Power Supply Current		3700 3250 2950 2650	mA mA mA mA	@120 MHz(4) @100 MHz(4) @90 MHz(4) @75 MHz(4)

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK and PICCLK.
4. This value should be used for power supply design. It was determined using a worst case instruction mix and V_{CC} + 5%. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to section 3.4.3.

Table 9. 3.3V (5V-Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	−0.3	0.8	V	TTL Level(1)
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level(1)

NOTES:
1. Applies to CLK and PICCLK only.

Table 10. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	4
C_O	Output Capacitance		20	pF	4
$C_{I/O}$	I/O Capacitance		25	pF	4
C_{CLK}	CLK Input Capacitance		15	pF	4
C_{TIN}	Test Input Capacitance		15	pF	4
C_{TOUT}	Test Output Capacitance		20	pF	4
C_{TCK}	Test Clock Capacitance		15	pF	4
I_{LI}	Input Leakage Current		±15	μA	$0 < V_{IN} < V_{CC3}$(1)
I_{LO}	Output Leakage Current		±15	μA	$0 < V_{IN} < V_{CC3}$(1)
I_{IH}	Input Leakage Current		200	μA	$V_{IN} = 2.4V$(3)
I_{IL}	Input Leakage Current		−400	μA	$V_{IN} = 0.4V$(2)

NOTES:
1. This parameter is for input without pullup or pulldown.
2. This parameter is for input with pullup.
3. This parameter is for input with pulldown.
4. Guaranteed by design.

Table 11. Preliminary Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical(1)	Max(2)	Unit	Notes
Active Power Dissipation	4.7	11.9	Watts	@120 MHz
	3.9	10.1	Watts	@100 MHz
	3.5	9.0	Watts	@90 MHz
	3.0	8.0	Watts	@75 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		1.47	Watts	@120 MHz
		1.55	Watts	@100 MHz(3)
		1.40	Watts	@90 MHz(3)
		1.20	Watts	@75 MHz
Stop Clock Power Dissipation	0.02	<0.05	Watts	4

NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at V_{CC} = 3.3V running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with V_{CC} = 3.3V and also takes into account the thermal time constants of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

3.4 AC Specifications

The AC specifications of the Pentium processor 75/90/100/120 consist of setup times, hold times, and valid delays at 0 pF.

3.4.1 PRIVATE BUS

When two Pentium processors 75/90/100/120 are operating in dual processor mode, a "private bus" exists to arbitrate for the CPU bus and maintain local cache coherency. The private bus consists of two pinout changes:

1. Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
2. Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC.

The new pins are given AC specifications of valid delays at 0 pF, setup times, and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must only be met when a dual processor is present in the system.

3.4.2 POWER AND GROUND

For clean on-chip power distribution, the Pentium processor 75/90/100/120 has 53 V_{CC} (power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium processor 75/90/100/120. On the circuit board all V_{CC} pins must be connected to a 3.3V V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

3.4.3 DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Pentium processor 75/90/100/120. The Pentium processor 75/90/100/120 driving its large address and data buses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Pentium processor 75/90/100/120 and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

For the Pentium processor 75/90/100/120, the power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the Pentium processor 75/90/100/120 to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the Pentium processor 75/90/100/120. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 μf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the Pentium processor 75/90/100/120 (on the 3.3V plane) to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

3.4.4 CONNECTION SPECIFICATIONS

All NC and INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to ground.

3.4.5 AC TIMING TABLES

3.4.5.1 AC Timing Table for a 50-MHz Bus

The AC specifications given in Tables 12 and 13 consist of output delays, input setup requirements and input hold requirements for a 50-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor 75/90/100/120 operation.

Table 12. Pentium® Processor 610\75, 815\100 AC Specifications for 50-MHz Bus Operation
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	25.0	50.0	MHz		Max Core Freq = 100 MHz @1/2
t_{1a}	CLK Period	20.0	40.0	nS	4	
t_{1b}	CLK Period Stability		±250	pS		1, 25
t_2	CLK High Time	4.0		nS	4	@2V,(1)
t_3	CLK Low Time	4.0		nS	4	@0.8V,(1)
t_4	CLK Fall Time	0.15	1.5	nS	4	(2.0V–0.8V),(1,5)
t_5	CLK Rise Time	0.15	1.5	nS	4	(0.8V–2.0V), (1,5)
t_{6a}	ADS#, ADSC#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	5	

Table 12. Pentium® Processor 610\75, 815\100 AC Specifications for 50-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{6b}	AP Valid Delay	1.0	8.5	nS	5	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	5	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	6	1
t_8	APCHK#, IERR#, FERR#, PCHK# Valid Delay	1.0	8.3	nS	5	4
t_{9a}	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	5	4
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	5	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	5	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	6	1
t_{14}	A5-A31 Setup Time	6.5		nS	7	26
t_{15}	A5-A31 Hold Time	1.0		nS	7	
t_{16a}	INV, AP Setup Time	5.0		nS	7	
t_{16b}	EADS# Setup Time	6.0		nS	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	7	
t_{18a}	KEN# Setup Time	5.0		nS	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	7	
t_{22}	BOFF# Setup Time	5.5		nS	7	
t_{22a}	AHOLD Setup Time	6.0		nS	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	7	

Table 12. Pentium® Processor 610\75, 815\100 AC Specifications for 50-MHz Bus Operation (Contd.)
3.135 < V_{CC} < 3.465V, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	7	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	7	
t_{25a}	HOLD Hold Time	1.5		nS	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	7	12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1 .0		nS	7	13
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	7	12, 16, 17
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	7	13
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	7	15, 17
t_{31}	R/S# Setup Time	5.0		nS	7	12, 16, 17
t_{32}	R/S# Hold Time	1.0		nS	7	13
t_{33}	R/S# Pulse Width, Async.	2. 0		CLKs	7	15, 17
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	7	
t_{36}	RESET Setup Time	5.0		nS	8	11, 12, 16
t_{37}	RESET Hold Time	1.0		nS	8	11, 13
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	8	11, 17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	8	12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	8	13

Table 12. Pentium® Processor 610\75, 815\100 AC Specifications for 50-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge(16)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge(27)
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge(1,27)
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	8	To RESET falling edge(22)
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	8	To RESET falling edge(22)
t_{43c}	APICEN Setup Time	2.0		CLKs	8	To RESET falling edge
t_{43d}	APICEN Hold Time	2.0		CLKs	8	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		nS	4	
t_{46}	TCK High Time	25.0		nS	4	@2V(1)
t_{47}	TCK Low Time	25.0		nS	4	@0.8V(1)
t_{48}	TCK Fall Time		5.0	nS	4	(2.0V–0.8V)(1,8,9)
t_{49}	TCK Rise Time		5.0	nS	4	(0.8V–2.0V)(1,8,9)
t_{50}	TRST# Pulse Width	40.0		nS	10	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	9	7
t_{52}	TDI, TMS Hold Time	13.0		nS	9	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	9	8
t_{54}	TDO Float Delay		25.0	nS	9	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	9	3, 8, 10

Table 12. Pentium® Processor 610\75, 815\100 AC Specifications for 50-MHz Bus Operation (Contd.)
3.135 < V_{CC} < 3.465V, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	9	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	9	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	9	3, 7, 10
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60.0	500.0	nS	4	
t_{60c}	PICCLK High Time	9.0		nS	4	
t_{60d}	PICCLK Low Time	9.0		nS	4	
t_{60e}	PICCLK Rise Time	1.0	5.0	nS	4	
t_{60f}	PICCLK Fall Time	1.0	5.0	nS	4	
t_{60g}	PICD0-1 Setup Time	3.0		nS	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	nS	5	From PICCLK(28,29)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	nS	5	From PICCLK(28,29)

Table 13. Pentium® Processor 610\75, 815\100 Dual Processor Mode AC Specifications for 50 MHz Bus Operation

$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT# Valid Delay	1.0	5.0	nS	5	18
t_{80b}	PHIT#, PHITM# Flight Time	0	2.0	nS	11	30
t_{81a}	PBREQ#, PBGNT# Setup Time	8.0		nS	7	18
t_{82}	PBREQ#, PBGNT# Hold Time	1.0		nS	7	18, 24
t_{83a}	A5-A31 Setup Time	6 .5		nS	7	18, 21, 26
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	6.0		nS	7	18, 21
t_{83c}	ADS#, M/IO# Setup Time	8.0		nS	7	18, 21
t_{83d}	HIT#, HITM# Setup Time	8.0		nS	7	18, 21
t_{83e}	HLDA Setup Time	6.0		nS	7	18, 21
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A5-A31, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		nS	7	18, 21
t_{85}	DPEN# Valid Time		10.0	CLKs		18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLKs		18, 20, 23
t_{87}	APIC ID (BE0#-BE3#) Setup Time	2.0		CLKs	8	To RESET falling edge(23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLKs	8	From RESET falling edge(23)
t_{89}	D/P# Valid Delay	1.0	8.0	nS	5	Primary Processor Only

3.4.5.2 AC Timing Tables for a 60-MHz Bus

The AC specifications given in Tables 14 and 15 consist of output delays, input setup requirements and input hold requirements for a 60-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor 75/90/100/120 operation.

Table 14. Pentium® Processor 735\90 AC Specifications for 60-MHz Bus Operation
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz	4	
t_{1a}	CLK Period	16.67	33.33	nS	4	
t_{1b}	CLK Period Stability		±250	pS	4	Adjacent Clocks,(1,25)
t_2	CLK High Time	4.0		nS	4	@2V(1)
t_3	CLK Low Time	4.0		nS	4	@0.8V(1)
t_4	CLK Fall Time	0.15	1.5	nS	4	(2.0V–0.8V)(1,5)
t_5	CLK Rise Time	0.15	1.5	nS	4	(0.8V–2.0V)(1,5)
t_{6a}	ADS#, ADSC#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	5	
t_{6b}	AP Valid Delay	1.0	8.5	nS	5	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	5	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	5	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	5	4
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	5	4
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	5	
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	5	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	5	

Table 14. Pentium® Processor 735\90 AC Specifications for 60-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	6	1
t_{14}	A5-A31 Setup Time	6.0		nS	7	26
t_{15}	A5-A31 Hold Time	1.0		nS	7	
t_{16a}	INV, AP Setup Time	5.0		nS	7	
t_{16b}	EADS# Setup Time	5.5		nS	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	7	
t_{18a}	KEN# Setup Time	5.0		nS	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	7	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	7	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	7	
t_{25a}	HOLD Hold Time	1.5		nS	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	7	12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	7	13
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	7	12, 16, 17
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	7	13
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		15, 17
t_{31}	R/S# Setup Time	5.0		nS	7	12, 16, 17
t_{32}	R/S# Hold Time	1.0		nS	7	13
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs	7	15, 17

Table 14. Pentium® Processor 735\90 AC Specifications for 60-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.0		nS	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	8	
t_{36}	RESET Setup Time	5.0		nS	8	11, 12, 16
t_{37}	RESET Hold Time	1.0		nS	8	11, 13
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	8	11, 17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	8	12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	8	13
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge(16)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge (27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge(27)
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge(1,27)
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	8	To RESET falling edge(22)
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	8	To RESET falling edge(22)
t_{43c}	APICEN Setup Time	2.0		CLKs	8	To RESET falling edge
t_{43d}	APICEN Hold Time	2.0		CLKs	8	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz	8	
t_{45}	TCK Period	62.5		nS	4	
t_{46}	TCK High Time	25.0		nS	4	@2V(1)
t_{47}	TCK Low Time	25.0		nS	4	@0.8V(1)

Table 14. Pentium® Processor 735\90 AC Specifications for 60-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{48}	TCK Fall Time		5.0	nS	4	(2.0V–0.8V)(1,8,9)
t_{49}	TCK Rise Time		5.0	nS	4	(0.8V–2.0V)(1,8,9)
t_{50}	TRST# Pulse Width	40.0		nS	10	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	9	7
t_{52}	TDI, TMS Hold Time	13.0		nS	9	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	9	8
t_{54}	TDO Float Delay		25.0	nS	9	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	9	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	9	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	9	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	9	3, 7, 10
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz	4	
t_{60b}	PICCLK Period	60.0	500.0	nS	4	
t_{60c}	PICCLK High Time	9.0		nS	4	
t_{60d}	PICCLK Low Time	9.0		nS	4	
t_{60e}	PICCLK Rise Time	1.0	5.0	nS	4	
t_{60f}	PICCLK Fall Time	1.0	5.0	nS	4	
t_{60g}	PICD0-1 Setup Time	3.0		nS	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	nS	5	From PICCLK(28,29)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	nS	5	From PICCLK(28,29)

Table 15. Pentium® Processor 735\90 Dual Processor Mode AC Specifications for 60-MHz Bus Operation

$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT# Valid Delay	1.0	5.0	nS	5	18
t_{80b}	PHIT#, PHITM# Flight Time	0	2.0	nS	11	30
t_{81a}	PBREQ#, PBGNT# Setup Time	8.0		nS	7	18
t_{82}	PBREQ#, PBGNT# Hold Time	1.0		nS	7	18, 24
t_{83a}	A5-A31 Setup Time	3.0		nS	7	18, 21, 26
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	4.0		nS	7	18, 21
t_{83c}	ADS#, M/IO# Setup Time	6.0		nS	7	18, 21
t_{83d}	HIT#, HITM# Setup Time	6.0		nS	7	18, 21
t_{83e}	HLDA Setup Time	6.0		nS	7	18, 21
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A5-A31, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		nS	7	18, 21
t_{85}	DPEN# Valid Time		10.0	CLKs		18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLKs		18, 20, 23
t_{87}	APIC ID (BE0#–BE3#) Setup Time	2.0		CLKs	8	To RESET falling edge(23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLKs	8	From RESET falling edge(23)
t_{89}	D/P# Valid Delay	1.0	8.0	nS	5	Primary Processor Only

3.4.5.3 AC Timing Tables for a 66-MHz Bus

The AC specifications given in Tables 16 and 17 consist of output delays, input setup requirements and input hold requirements for a 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and AP IC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor 75/90/100/120 operation.

Table 16. Pentium® Processor 815\100 AC Specifications for 66-MHz Bus Operation
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	nS	4	
t_{1b}	CLK Period Stability		±250	pS		Adjacent Clocks(1,25)
t_2	CLK High Time	4.0		nS	4	@2V(1)
t_3	CLK Low Time	4.0		nS	4	@0.8V(1)
t_4	CLK Fall Time	0.15	1.5	nS	5	(2.0V–0.8V)(1)
t_5	CLK Rise Time	0.15	1.5	nS	4	(0.8V–2.0V)(1)
t_{6a}	ADSC#, PWT, PCD, BE0-7#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	nS	5	
t_{6b}	AP Valid Delay	1.0	8.5	nS	5	
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	5	
t_{6d}	ADS#, M/IO# Valid Delay	1.0	6.0	nS	5	
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	6	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	5	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	5	4
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	5	4
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	5	4
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	5	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	5	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	6	1
t_{14}	A5-A31 Setup Time	6.0		nS	7	26
t_{15}	A5-A31 Hold Time	1.0		nS	7	

Table 16. Pentium® Processor 815\100 AC Specifications for 66-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{16a}	INV, AP Setup Time	5.0		nS	7	
t_{16b}	EADS# Setup Time	5.5		nS	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	7	
t_{18a}	KEN# Setup Time	5.0		nS	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		nS	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		nS	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	7	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	7	
t_{25b}	HOLD Hold Time	1.5		nS	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	7	12, 16
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	7	13
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	7	12, 16, 17
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	7	13
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		15, 17
t_{31}	R/S# Setup Time	5.0		nS	7	12, 16, 17
t_{32}	R/S# Hold Time	1.0		nS	7	13
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		15, 17
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.0		nS	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	2.0		nS	7	
t_{36}	RESET Setup Time	5.0		nS	8	11, 12, 16

Table 16. Pentium® Processor 815\100 AC Specifications for 66-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{37}	RESET Hold Time	1.0		nS	8	11, 13
t_{38}	RESET Pulse Width, V_{CC} & CL K Stable	15.0		CLKs	8	11, 17
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time	5.0		nS	8	12, 16, 17
t_{41}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Hold Time	1.0		nS	8	13
t_{42a}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#) Setup Time, Async.	2.0		CLKs	8	To RESET falling edge(16)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, FRCMC#, BRDYC#, BUSCHK#) Hold Time, Async.	2.0		CLKs	8	To RESET falling edge(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLKs	8	To RESET falling edge(27)
t_{42d}	Reset Configuration Signal BRDYC# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge(1,27)
t_{43a}	BF, CPUTYP Setup Time	1.0		mS	8	To RESET falling edge(22)
t_{43b}	BF, CPUTYP Hold Time	2.0		CLKs	8	To RESET falling edge(22)
t_{43c}	APICEN Setup Time	2.0		CLKs	8	To RESET falling edge
t_{43d}	APICEN Hold Time	2.0		CLKs	8	To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		nS	4	
t_{46}	TCK High Time	25.0		nS	4	@2V(1)
t_{47}	TCK Low Time	25.0		nS	4	@0.8V(1)
t_{48}	TCK Fall Time		5.0	nS	4	(2.0V–0.8V)(1,8,9)
t_{49}	TCK Rise Time		5.0	nS	4	(0.8V–2.0V)(1,8,9)
t_{50}	TRST# Pulse Width	40.0		nS	10	Asynchronous(1)
t_{51}	TDI, TMS Setup Time	5.0		nS	9	7

Table 16. Pentium® Processor 815\100 AC Specifications for 66-MHz Bus Operation (Contd.)
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{52}	TDI, TMS Hold Time	13.0		nS	9	7
t_{53}	TDO Valid Delay	3.0	20.0	nS	9	8
t_{54}	TDO Float Delay		25.0	nS	9	1, 8
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	9	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	9	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	9	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	9	3, 7, 10
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz		
t_{60b}	PICCLK Period	60.0	500.0	nS	4	
t_{60c}	PICCLK High Time	9.0		nS	4	
t_{60d}	PICCLK Low Time	9.0		nS	4	
t_{60e}	PICCLK Rise Time	1.0	5.0	nS	4	
t_{60f}	PICCLK Fall Time	1.0	5.0	nS	4	
t_{60g}	PICD0-1 Setup Time	3.0		nS	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		nS	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	nS	5	From PICCLK(28,29)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	nS	5	From PICCLK(28,29)

Table 17. Pentium® Processor 815\100 Dual Processor Mode AC Specifications for 66-MHz Bus Operation

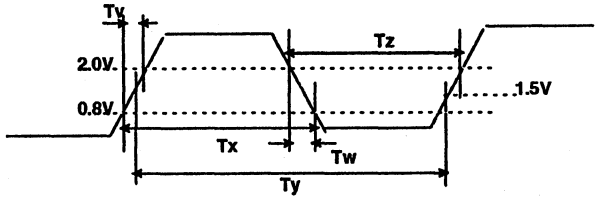
$3.135 < V_{CC} < 3.465V$, T_{CASE} = 0 to 70°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT# Valid Delay	1.0	5.0	nS	5	18
t_{80b}	PHIT#, PHITM# Flight Time	0	2.0	nS	11	30
t_{81a}	PBREQ#, PBGNT# Setup Time	8.0		nS	7	18
t_{82}	PBREQ#, PBGNT# Hold Time	1.0		nS	7	18, 24
t_{83a}	A5-A31 Setup Time	3.0		nS	7	18, 21, 26
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	4.0		nS	7	18, 21
t_{83c}	ADS#, M/IO# Setup Time	5.8		nS	7	18, 21
t_{83d}	HIT#, HITM# Setup Time	6.0		nS	7	18, 21
t_{83e}	HLDA Setup Time	6.0		nS	7	18, 21
t_{84}	ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, A5-A31, HLDA, HIT#, HITM#, SCYC Hold Time	1.0		nS	7	18, 21
t_{85}	DPEN# Valid Time		10.0	CLKs		18, 19, 23
t_{86}	DPEN# Hold Time	2.0		CLKs		18, 20, 23
t_{87}	APIC ID (BE0#-BE3#) Setup Time	2.0		CLKs	8	To RESET falling edge(23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLKs	8	From RESET falling edge(23)
t_{89}	D/P# Valid Delay	1.0	8.0	nS	5	Primary Processor Only

NOTES:
Notes 2, 6, and 14 are general and apply to all standard TTL signals used with the Pentium® Processor family.
1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1V/nS rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns ≤ CLK input rise/fall time ≤ 8V/ns.
6. 0.3V/ns ≤ input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55\text{-}58}$).
11. FRCMC# should be tied to V_{CC} (high) to ensure proper operation of the Pentium processor 75/90/100/120 as a primary processor.
12. Setup time is required to guarantee recognition on a specific clock. Pentium processor 75/90/100/120 must meet this specification for dual processor operation for the FLUSH# and RESET signals.

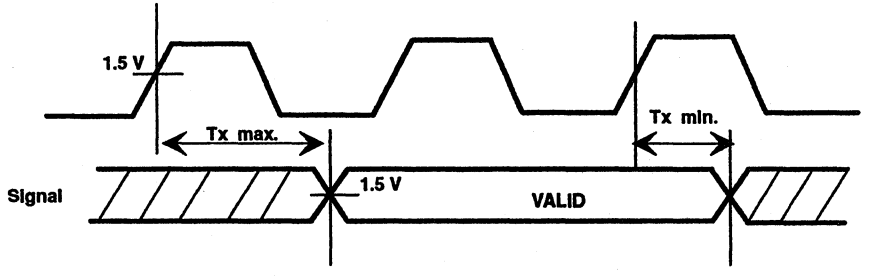
13. Hold time is required to guarantee recognition on a specific clock. Pentium processor 75/90/100/120 must meet this specification for dual processor operation for the FLUSH# and RESET signals.
14. All TTL timings are referenced from 1.5V.
15. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of 2 clocks before being returned active and must meet the minimum pulse width.
16. This input may be driven asynchronously. However, when operating two processors in dual processing mode, FLUSH# and RESET must be asserted synchronously to both processors.
17. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of 2 clocks before being returned active.
18. Timings are valid only when dual processor is present.
19. Maximum time DPEN# is valid from rising edge of RESET.
20. Minimum time DPEN# is valid after falling edge of RESET.
21. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
22. BF and CPUTYP should be strapped to V_{CC} or V_{SS}.
23. RESET is synchronous in dual processing mode and functional redundancy checking mode. All signals which have a setup or hold time with respect to a falling or rising edge of RESET in UP mode, should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing and functional redundancy checking modes.
24. The PHIT# and PHITM# signals operate at the core frequency (75, 90 or 100 MHz).
25. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
26. In dual processing mode, timing t_{14} is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
27. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
28. This assumes an external pullup resistor to V_{CC} and a lumped capacitive load such that the maximum RC product does not exceed $R = 150\Omega$, $C = 240$ pF.
29. This assumes an external pullup resistor to V_{CC} and a lumped capacitive load such that the minimum RC product does not fall below $R = 150\Omega$, $C = 20$ pF.
30. This is a flight time specification, that includes both flight time and clock skew. The flight time is the time from where the unloaded driver crosses 1.5V (50% of min V_{CC}), to where the receiver crosses the 1.5V level (50% of min V_{CC}). See Figure 11.

** Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.



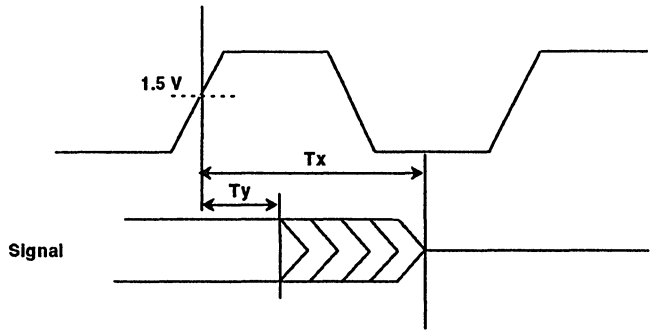
Tv = t5, t49, t60e; Tw = t4, t48, t60f; Tx = t3, t47, t60d
Ty = t1, t45, t60b; Tz = t2, t46, t60c

Figure 4. Clock Waveform



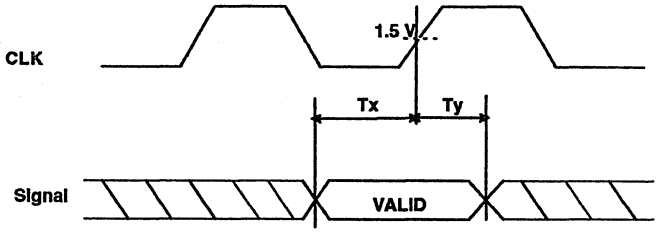
Tx = t6, t8, t9, t10, t11, t12, t60i, t80, t89

Figure 5. Valid Delay Timings



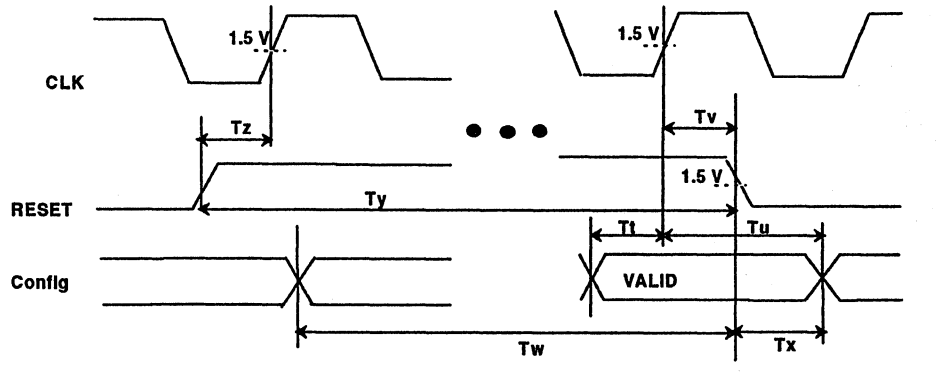
Tx = t7, t13; Ty = t6min, t12min

Figure 6. Float Delay Timings



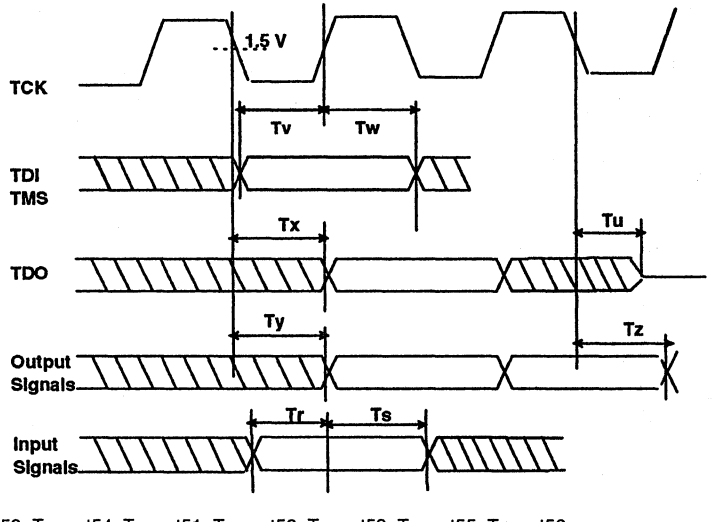
Tx = t14, t16, t18, t20, t22, t24, t26, t28, t31, t34, t60g (to PICCLK),t81, t83
Ty = t15, t17, t19, t21, t23, t25, t27, t29, t32, t35, t60h (to PICCLK), t82, t84

Figure 7. Setup and Hold Timings



Tt = t40, Tu = t41, Tv = t37, T w =t42, t43a, t43c, t87, Tx = t43b, t43d, t88, Ty = t38, t39, Tz = t36

Figure 8. Reset and Configuration Timings



Tr = t57, Ts = t58, Tu = t54, Tv = t51, Tw = t52, Tx = t53, Ty = t55, Tz = t56

Figure 9. Test Timings

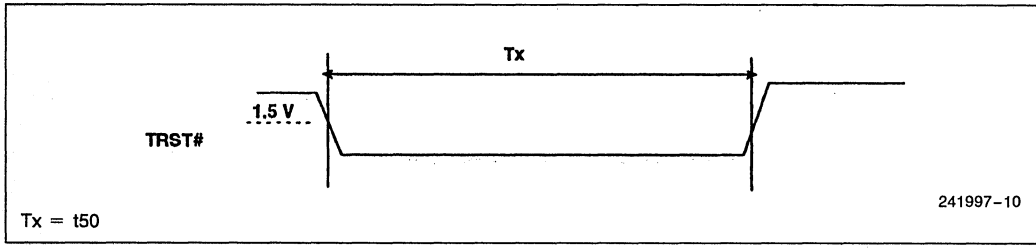


Figure 10. Test Reset Timings

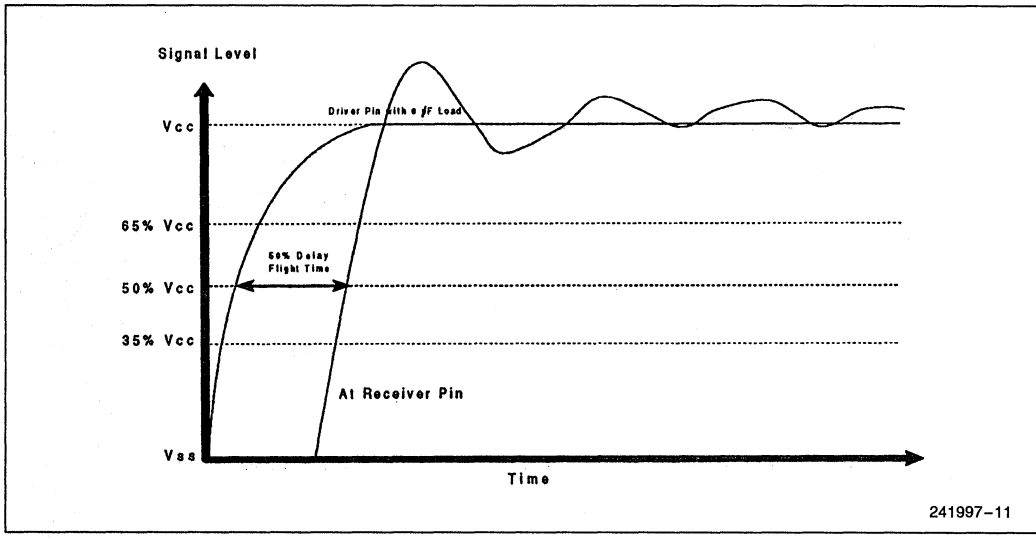


Figure 11. 50% V_{CC} Measurement of Flight Time

4.0 MECHANICAL SPECIFICATIONS

The Pentium processor 75/90/100/120 is packaged in a 296-pin staggered pin grid array package. The pins are arranged in a 37 x 37 matrix and the package dimensions are 1.95″ x 1.95″ (Table 18). A 1.25″ x 1.25″ copper tungsten heat spreader may be attached to the top of the ceramic. This package design with spreader is being phased out in favor of a package which has no attached spreader. In this section, both spreader and non-spreader packages are shown.

The mechanical specifications for the Pentium processor 75/90/100/120 are provided in Table 19. Figure 12 shows the package dimensions.

Table 18. Package Information Summary

	Package Type	Total Pins	Pin Array	Package Size
Pentium® Processor 75/90/100/120	SPGA	296	37 x 37	1.95″ x 1.95″ 4.95 cm x 4.95 cm

Table 19. Package Dimensions with Spreader

Family: Ceramic Staggered Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.91	4.70	Solid Lid	0.154	0.185	Solid Lid
A1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.91		1.940	1.965	
D1	45.47	45.97		1.790	1.810	
D2	31.50	32.00	Square	1.240	1.260	Square
D3	33.99	34.59		1.338	1.362	
D4	8.00	9.91		0.315	0.390	
E1	2.41	2.67		0.095	0.105	
E2	1.14	1.40		0.045	0.055	
F		0.127	Diagonal		0.005	Diagonal
L	3.05	3.30		0.120	0.130	
N	296			296		
S1	1.52	2.54		0.060	0.100	

Table 20. Package Dimensions without Spreader

Family: 296-Pin Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.27	3.83	Ceramic Lid	0.129	0.151	Ceramic Lid
A1	0.66	0.86	Ceramic Lid	0.026	0.034	Ceramic Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
F		0.127	Flatness of the top of the package, measured diagonally		0.005	Flatness of the top of the package, measured diagonally
L	3.05	3.30		0.120	1.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	

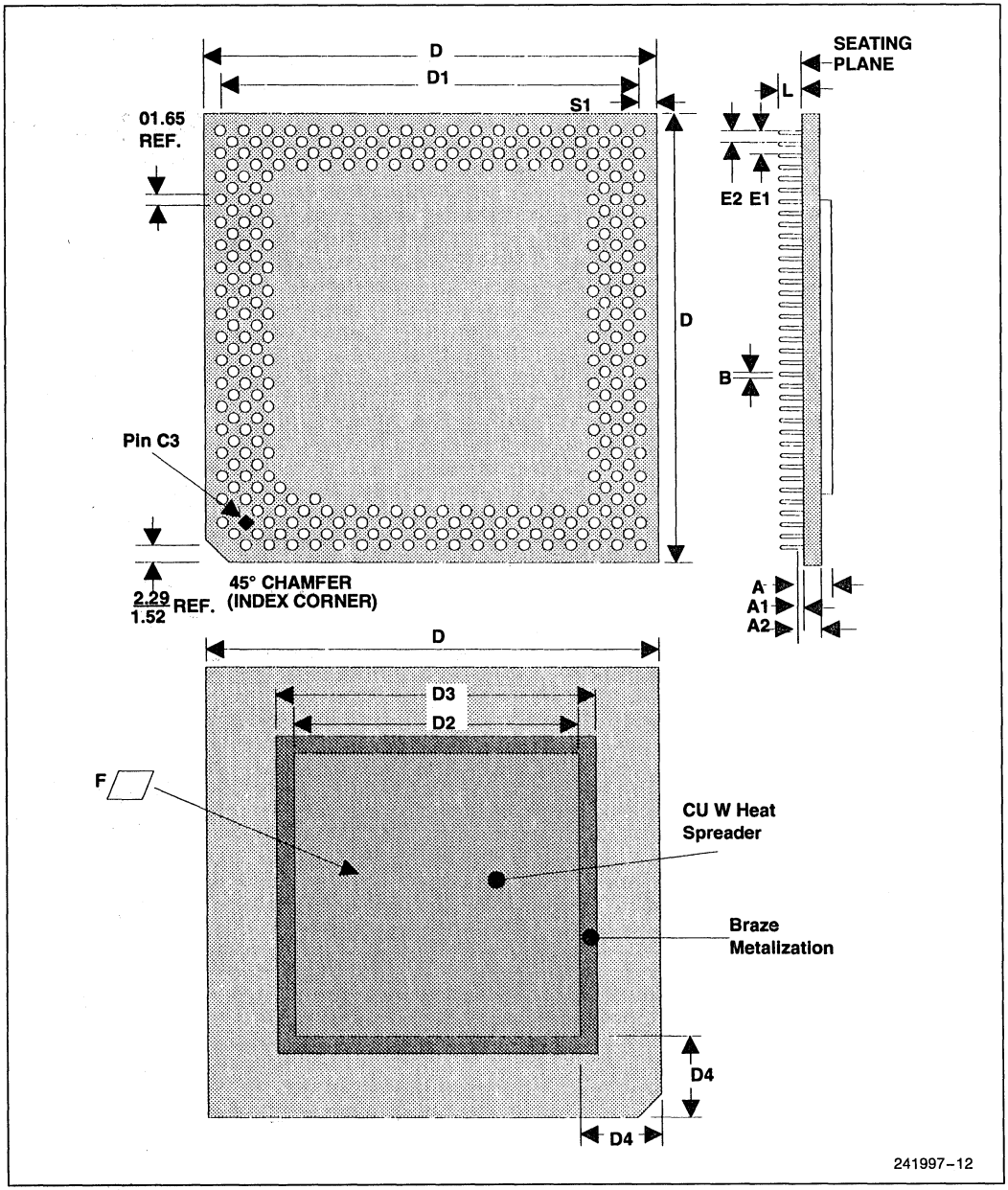


Figure 12. Pentium® Processor 75/90/100/120 Package Dimensions (with Spreader)

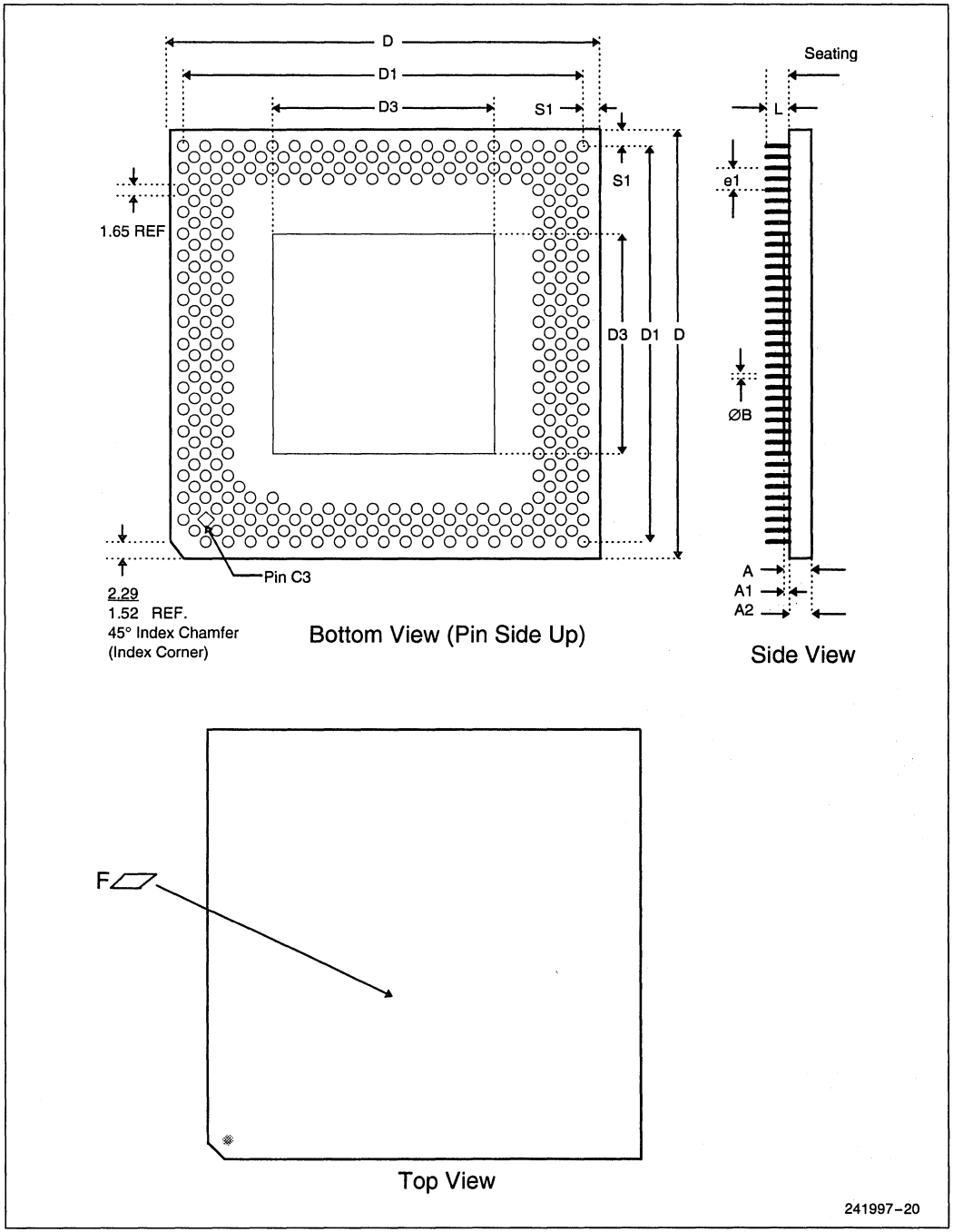


Figure 13. Pentium® Processor 75/90/100/120 Package Dimensions (without Spreader)

5.0 THERMAL SPECIFICATIONS

Due to the advanced 3.3V BiCMOS process that it is produced on, the Pentium processor 75/90/100/120 dissipates less power than the Pentium processor 60/66.

The Pentium processor 75/90/100/120 is specified for proper operation when case temperature, T_{CASE}, (T_C) is within the specified range of 0°C to 70°C.

5.1 Measuring Thermal Values

The Pentium processor 75/90/100/120 package will include a heat spreader. To verify that the proper T_C (case temperature) is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heat sink attached. When a heat sink is attached a hole (smaller than 0.150" diameter) should be drilled through the heat sink to allow probing the center of the package. See Figure 13 for an illustration of how to measure T_C.

To minimize the measurement errors, it is recommended to use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number: OB-100).
- The thermocouple should be attached at a 90-degree angle as shown in Figure 14.
- The hole size should be smaller than 0.150" in diameter.

5.1.1 THERMAL EQUATIONS AND DATA

For the Pentium processor 75/90/100/120, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that T_C is met. To calculate T_A values, the following equations may be used:

$$T_A = T_C - (P * \theta_{CA})$$

$$\theta_{CA} = \theta_{JA} - \theta_{JC}$$

where:

T_A and T_C = ambient and case temperature. (°C)

θ_{CA} = case-to-ambient thermal resistance. (°C/Watt)

θ_{JA} = junction-to-ambient thermal resistance. (°C/Watt)

θ_{JC} = junction-to-case thermal resistance. (°C/Watt)

P = maximum power consumption (Watt)

Table 21 lists the θ_{CA}values for the Pentium processor 75/90/100/120 with passive heat sinks. Figure 15 shows Table 21 in graphic format.

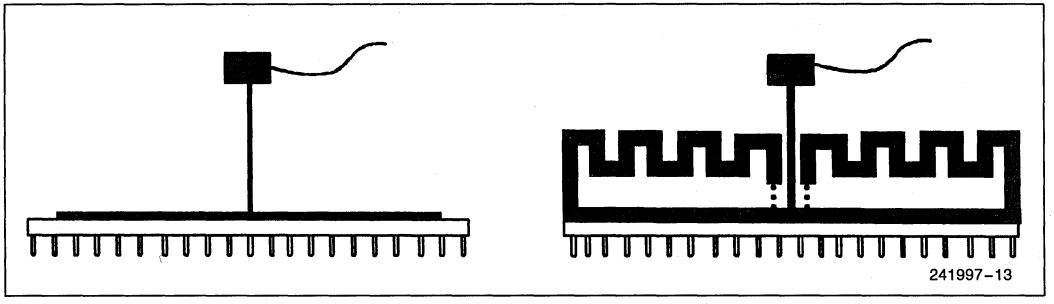


Figure 14. Technique for Measuring TC

Table 21. Thermal Resistances for Packages with Spreader

Heat Sink in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
1.95x1.95x0.25	0.9	8.7	7.6	6.2	4.0	3.2	2.6
1.95x1.95x0.35	0.9	8.4	7.1	5.6	3.6	2.9	2.4
1.95x1.95x0.45	0.9	8.0	6.6	4.9	3.2	2.5	2.1
1.95x1.95x0.55	0.9	7.7	6.1	4.3	2.8	2.2	1.9
1.95x1.95x0.65	0.9	7.3	5.6	3.9	2.6	2.0	1.7
1.95x1.95x0.80	0.9	6.6	4.9	3.5	2.2	1.8	1.6
1.95x1.95 x1.00	0.9	5.9	4.2	3.2	2.2	1.7	1.4
1.95x1.95x1.20	0.9	5.5	3.9	2.9	2.0	1.6	1.4
1.95x1.95x1.40	0.9	5.0	3.5	2.6	1.8	1.5	1.3
Without Heat Sink	1.4	11.4	10.5	8.7	5.7	4.5	3.8

Table 22. Thermal Resistances for Packages without Spreader

Heat Sink in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.8	9.1	8.0	6.6	4.4	3.6	3.0
0.35	0.8	8.8	7.5	6.0	4.0	3.3	2.8
0.45	0.8	8.4	7.0	5.3	3.6	2.9	2.5
0.55	0.8	8.1	6.5	4.7	3.2	2.6	2.3
0.65	0.8	7.7	6.0	4.3	3.0	2.4	2.1
0.80	0.8	7.0	5.3	3.9	2.8	2.2	2.0
1.00	0.8	6.3	4.6	3.6	2.6	2.1	1.8
1.20	0.8	5.9	4.3	3.3	2.4	2.0	1.8
1.40	0.8	5.4	3.9	3.0	2.2	1.9	1.7
Without Heat Sink	1.3	14.4	13.1	11.7	8.8	7.4	6.5

NOTES:
Heat sinks are omni directional pin aluminum alloy.
Features were based on standard extrusion practices for a given height
Pin size ranged from 50 to 129 mils
Pin spacing ranged from 93 to 175 mils
Based thickness ranged from 79 to 200 mils
Heat sink attach was 0.005″ of thermal grease.
Attach thickness of 0.002″ will improve performance approximately 0.3°C/Watt

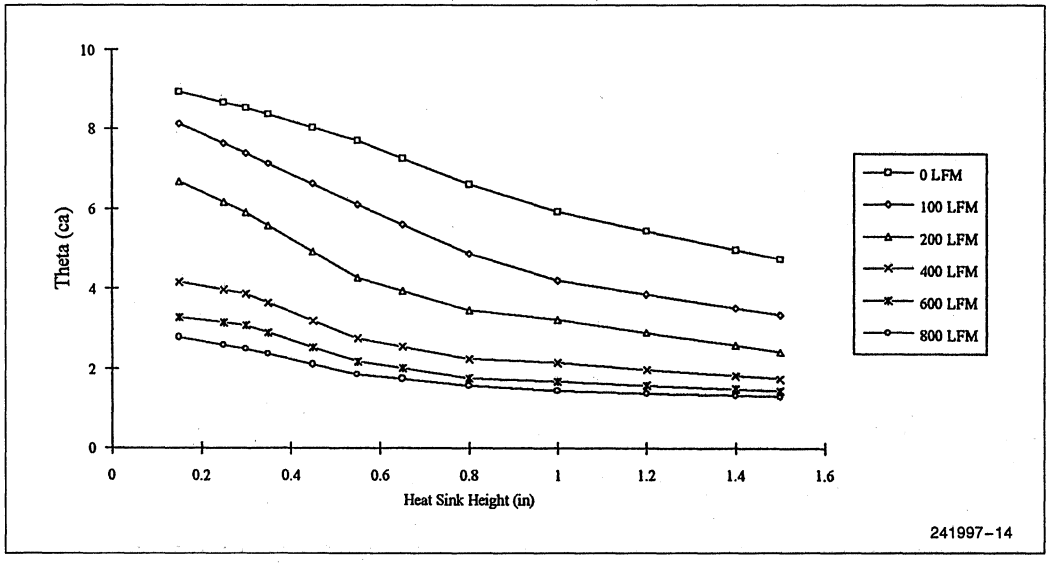


Figure 15. Thermal Resistance vs. Heatsink Height (Spreader Package)

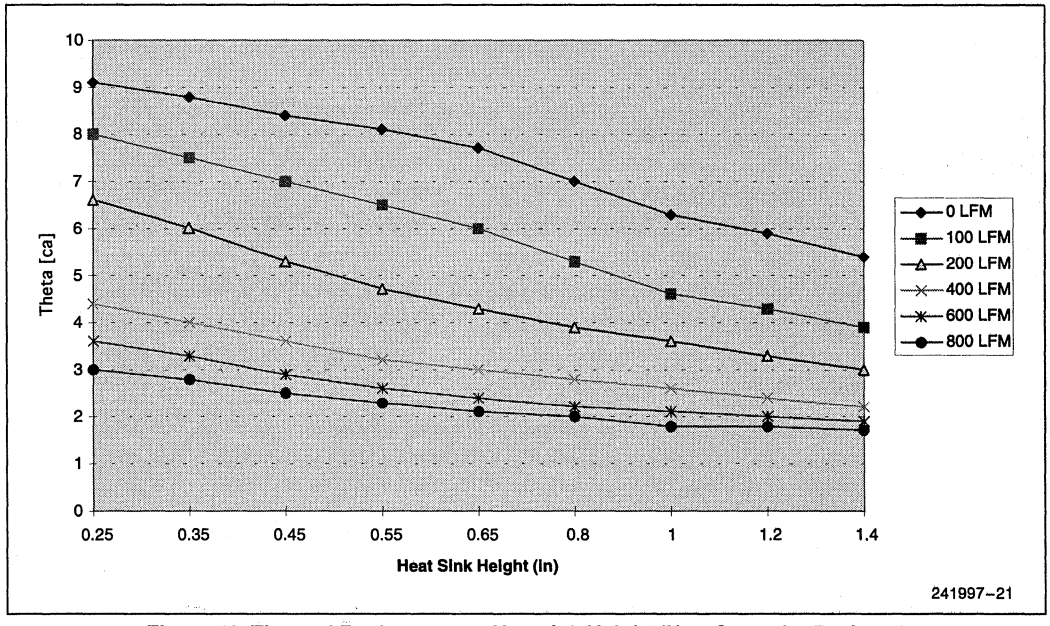


Figure 16. Thermal Resistance vs. Heatsink Height (Non-Spreader Package)

6.0 FUTURE PENTIUM® OverDrive™ PROCESSOR SOCKET SPECIFICATION

6.1 Introduction

The Future Pentium OverDrive processor is an end-user single-chip CPU upgrade product for Pentium processor 75/90/100/120-based systems. The Future Pentium OverDrive processor will speed up most software applications by 40% to 70%. It is binary compatible with the Pentium processor 75/90/100/120.

An upgrade socket (Socket 5) has been defined along with the Pentium processor 75/90/100/120 as part of the processor architecture. Upgradability can be supported by implementing either a single socket or a dual socket strategy for Pentium processor 75/90/100/120-based systems. A single socket system will include a 320-pin SPGA Socket 5. When this system configuration is upgraded, the Pentium processor 75/90/100/120 is simply replaced by the Future Pentium OverDrive processor. A dual socket system will include a 296-pin SPGA socket for the Pentium processor 75/90/100/120 and a 320-pin SPGA Socket 5 for the second processor. In dual socket systems, Socket 5 can be filled with either the Dual processor or the Future Pentium OverDrive processor.

6.1.1 UPGRADE OBJECTIVES

Systems using the Pentium processor 75/90/100/120, and equipped with only one processor socket, must use socket 5 to also accept the Future Pentium OverDrive processor. Systems equipped with two processor sockets must use Socket 5 as the second socket to contain either the Pentium processor 75/90/100/120 Dual processor or the Future Pentium OverDrive processor.

Inclusion of Socket 5 in Pentium processor 75/90/100/120 systems provides the end-user with an easy and cost-effective way to increase system performance. The paradigm of simply installing an additional component into an easy to use Zero Insertion Force (ZIF) Socket to achieve enhanced system performance is familiar to the millions of end-users and dealers who have purchased Intel math coprocessor upgrades to boost system floating point performance.

The majority of upgrade installations which take advantage of Socket 5 will be performed by end users and resellers. Therefore, it is important that the design be "end-user easy," and that the amount of training and technical expertise required to install the upgrade processors be minimized. Upgrade installation instructions should be clearly described in the system user's manual. In addition, by making installation simple and foolproof, PC manufacturers can reduce the risk of system damage, warranty claims and service calls. Feedback from Intel's math coprocessor upgrade customers highlights three main characteristics of end user easy designs:

- accessible socket location
- clear indication of upgrade component orientation
- minimization of insertion force

The Future Pentium OverDrive processor will support the 82430NX PCIset. Unlike the Pentium processor 75/90/100/120, the Future Pentium OverDrive processor will not support the 82497 Cache Controller and 82492 Cache SRAM chip set.

6.1.2 INTEL VERIFICATION PROGRAM

The Intel Verification Program ensures that a Pentium processor 75/90/100/120-based personal computer meets a minimum set of design criteria for reliable and straight-forward CPU upgradability with a Future Pentium OverDrive processor. Testing performed at the Intel Verification Labs confirms that Future Pentium OverDrive processor specifications for mechanical, thermal, electrical, functional, and end-user installation attributes have been met. While system designs may exceed these minimum design criteria, the intent is to provide end-users with confidence that computer systems based on verified designs can be upgraded with Future Pentium OverDrive processors.

The OEM submits production-ready designs to one of Intel's worldwide Verification Labs for testing. The OEM benefits from advance testing of the design prior to availablitiy of the Future Pentium OverDrive processor. By identifying and resolving upgradability problems before a system is introduced, the OEM increases system quality and reduces future support costs associated with end-user calls and complications when the CPU upgrade is ultimately installed.

Contact your local Intel representative for more information on the Intel Verification Program for Pentium processor 75/90/100/120-based systems.

6.2 Future Pentium® OverDrive® Processor (Socket 5) Pinout

This section contains pinouts of the Future Pentium OverDrive Socket (Socket 5) when used as a single-socket turbo upgrade.

6.2.1 PIN DIAGRAMS

6.2.1.1 Socket 5 Pinout

For systems with a single socket for the Pentium processor 75/90/100/120 and Future Pentium OverDrive processor, the following pinout *must* be followed for the single socket location. Note that to be Intel Verified for a Future Pentium OverDrive processor, this must be a ZIF socket. The socket footprint contains V_{CC}, V_{CC5}, and V_{SS} pins that are internal no connects on the Pentium processor 75/90/100/120. These pins *must* be connected to the appropriate PCB power and ground layers to ensure Future Pentium OverDrive processor compatibility.

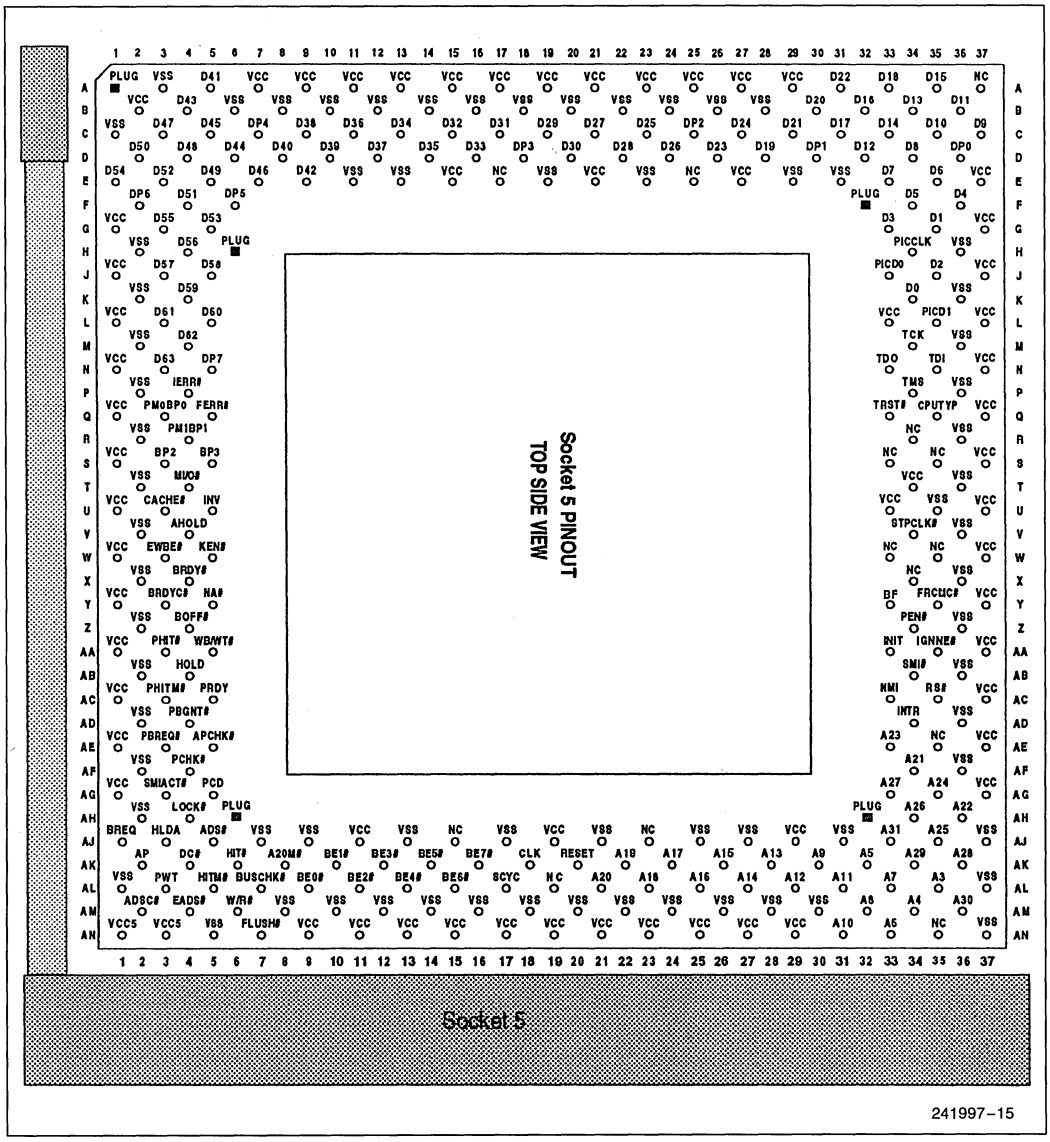


Figure 17. Socket 5 Pinout Top Side View

NOTE:

The "Socket 5 PINOUT TOP SIDE VIEW" text orientation on the top side view drawing in this section represents the orientation of the ink mark on the actual packages. (Note that the text shown in this section is not the actual text which will be marked on the packages).

Table 23. Pentium® Processor 75/90/100/120 vs. Socket 5 Pins

Pentium® Processor 75/90/100/120 Signal	Socket 5 Signal	Pin Number
INC	V_{SS}	A03
D/P#	NC	AE35
NO PIN	V_{SS}	AJ07
NO PIN	V_{SS}	AJ09
NO PIN	V_{CC}	AJ11
NO PIN	V_{SS}	AJ13
NO PIN	NC	AJ15
NO PIN	V_{SS}	AJ17
NO PIN	V_{CC}	AJ19
NO PIN	V_{SS}	AJ21
NO PIN	NC	AJ23
NO PIN	V_{SS}	AJ25
NO PIN	V_{SS}	AJ27
NO PIN	V_{CC}	AJ29
NO PIN	V_{SS}	AJ31
INC	V_{CC5}	AN01
INC	V_{CC5}	AN03
INC	V_{CC}	B02
NO PIN	V_{SS}	E11
NO PIN	V_{SS}	E13
NO PIN	V_{CC}	E15
NO PIN	NC	E17
NO PIN	V_{SS}	E19
NO PIN	V_{CC}	E21
NO PIN	V_{SS}	E23
NO PIN	NC	E25
NO PIN	V_{CC}	E27
NO PIN	V_{SS}	E29
NO PIN	V_{SS}	E31

NOTE:
All INCs are internal no connects. These signals are guaranteed to remain internally not connected in the Pentium processor 75/90/100/120.

6.3 Electrical Specifications

The Future Pentium OverDrive processor will have the same AC specifications, power and ground specifications and decoupling recommendations as the Pentium processor 75/90/100/120.

6.3.1 V_{CC5} PIN DEFINITION

The Future Pentium OverDrive processor pinout contains two 5V V_{CC} pins (V_{CC5}) used to provide power to the fan/heatsink. These pins should be connected to +5V ±5% regardless of the system design. Failure to connect V_{CC5} to 5V may cause the component to shut down.

6.4 Absolute Maximum Ratings of Upgrade

The on-chip Voltage Regulation and fan/heatsink devices included with the Future Pentium OverDrive processor require different stress ratings than the Pentium processor 75/90/100/120. The voltage regulator is surface mounted on the Future Pentium OverDrive processor and is, therefore, an integral part of the assembly. The Future Pentium OverDrive processor storage temperature ratings are tightened as a result. The fan is a detachable unit, and the storage temperature is stated separately in the table below. Functional operation of the Future Pentium OverDrive processor remains 0°C to 70°C.

Future Pentium® OverDrive® Processor and Voltage Regulator Assembly

Storage Temperature ..... −30°C to 100°C

Case Temperature Under Bias ..... −30°C to 100°C

Fan

Storage Temperature ..... −30°C to 75°C

Case Temperature Under Bias ..... −30°C to 75°C

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.4.1 DC SPECIFICATIONS

The Future Pentium OverDrive processor will have compatible DC specifications to the Pentium processor 75/90/100/120, except that I_{CC3} (Power Supply Current), I_{CC5} (Fan/Heatsink Current), and V_{CC} are the following:

Table 24. Future Pentium® OverDrive® Processor I_{CC} Specification

V_{CC5} = 5V ±5%, T_{CASE} = 0 to 70°C

Symbol	Parameter	Min	Max	Unit
I_{CC3}(1)	Power Supply Current		4330	mA
I_{CC5}	Fan/Heatsink Current		200	mA

NOTE:
1. V_{CC} = 3.135V to 3.6V

6.5 Mechanical Specifications

The Future Pentium OverDrive processor will be packaged in a 320-pin ceramic staggered pin grid array (SPGA). The pins will be arranged in a 37 x 37 matrix and the package dimensions will be 1.95" x 1.95" (4.95 cm x 4.95 cm).

Table 25. Processor Package Information Summary

	Package Type	Total Pins	Pin Array	Package Size
Future Pentium® OverDrive® Processor	SPGA	320	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

Table 26. Future Pentium® OverDrive® Processor Package Dimensions

Family: Ceramic Staggered Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A*		33.88	Solid Lid		1.334	Solid Lid
A1	0.33	0.43	Solid Lid	0.013	0.017	Solid Lid
A2	2.62	2.97		0.103	0.117	
A4		20.32			0.800	
A5	10.16		Air Space	0.400		Air Space
B	0.43	0.51		0.017	0.020	
D	49.28	49.91		1.940	1.965	
D1	45.47	45.97		1.790	1.810	
E1	2.41	2.67		0.095	0.105	
E2	1.14	1.40		0.045	0.055	
L	3.05	3.30		0.120	0.130	
N	320		SPGA pins	320		SPGA pins
S1	1.52	2.54		0.060	0.100	

NOTES:
* Assumes the minimum air space above the fan/heatsink
A 0.2" clearance around three of four sides of the package is also required to allow free airflow through the fan/heatsink.

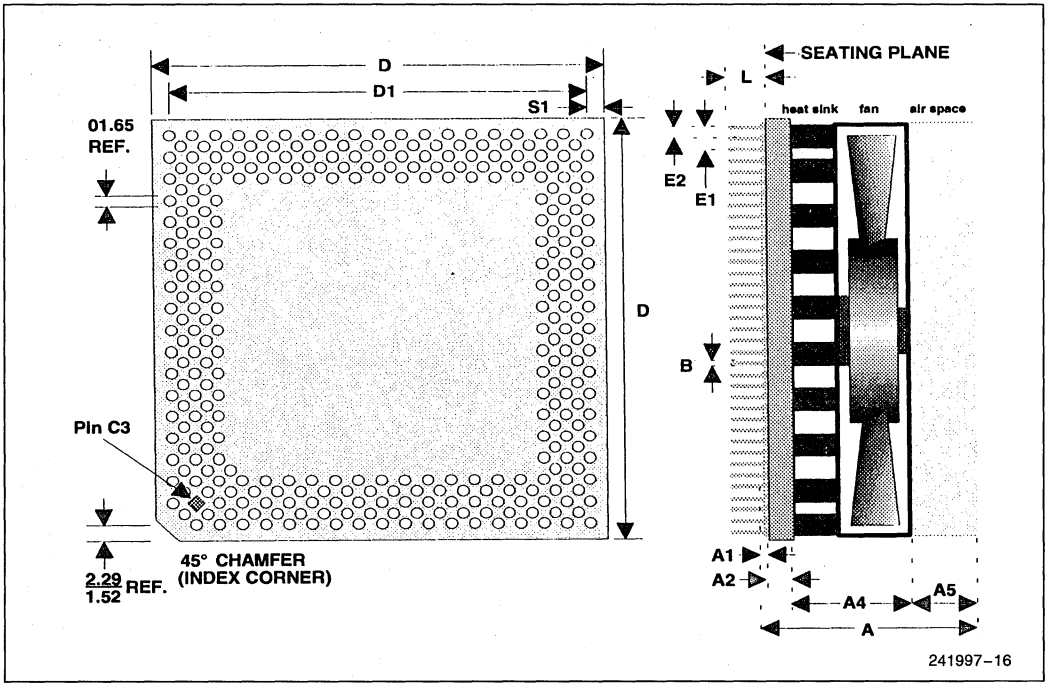


Figure 18. Future Pentium® OverDrive® Processor Package Dimensions

6.6 Thermal Specifications

The Future Pentium OverDrive processor will be cooled with a fan/heatsink cooling solution. The Future Pentium OverDrive processor with a fan/heatsink is specified for proper operation when T_A (air temperature entering the fan/heatsink) is a maximum of 45°C. When the $T_A(max) \leq 45°C$ specification is met, the fan/heatsink will keep T_C (case temperature) within the specified range of 0°C to 70°C provided airflow through the fan/heatsink is unimpeded.

6.7 Upgradability with Socket 5

6.7.1 INTRODUCTION

- Built-in upgradability for Pentium processor 75/90/100/120 based systems
  - — Supports the Future Pentium OverDrive processor 320-pin socket (Socket 5)

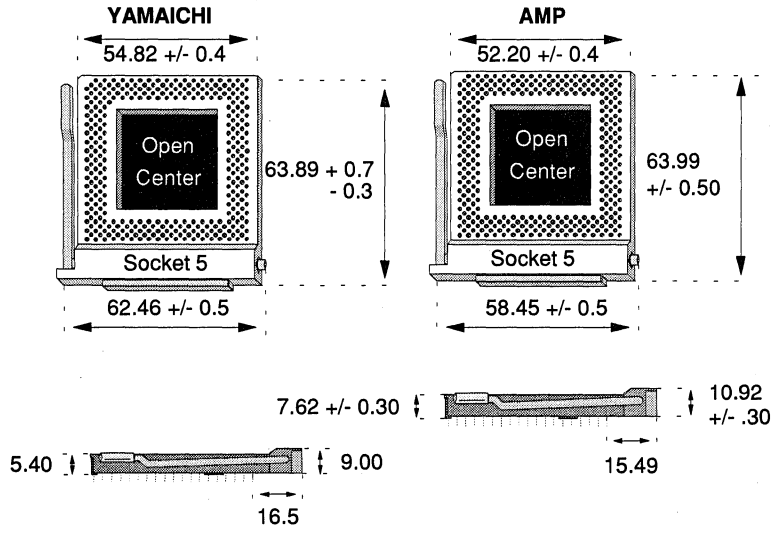
6.7.2 SOCKET 5 VENDORS

OEMs should contact Intel for the most current list of Intel-qualified socket vendors. For a complete list of Qualified Sockets and Vendor Order Numbers, call the Intel Faxback number for your geographical area and have document #7209 automatically faxed to you. Figure 19 shows preliminary dimensions for AMP and Yamaichi sockets. OEMs should directly contact the socket vendors for the most current socket information. Figure 20 shows the upgrade processor's orientation in Socket 5.

To order Socket 5 from AMP and Yamaichi, the phone numbers and part numbers are as follows:

AMP: 1-800-522-6752
part#: 916513-1

Yamaichi: 1-800-769-0797
part#: NP210-320K13625



NOTE:
All dimensions are in mm.

Figure 19. Socket 5 Footprint Dimensions

WARNING:
See socket manufacturer for the most current information.

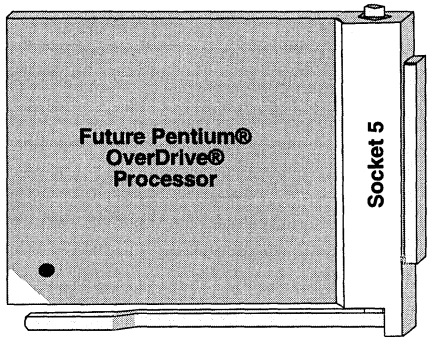


Figure 20. Socket 5 Chip Orientation

6.8 Testability

6.8.1 BOUNDARY SCAN

The Future Pentium OverDrive processor supports the IEEE Standard 1149.1 boundary scan using the Test Access Port (TAP) and TAP Controller. The boundary scan register for the Future Pentium OverDrive processor contains a cell for each pin. The turbo upgrade component will have a different bit order than the Pentium processor 75/90/100/120. If the TAP port on your system will be used by an end user following installation of the Future Pentium OverDrive processor, please contact Intel for the bit order of the upgrade processor boundary scan register.

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