Semiconductor Corporation

CS4248

Parallel Interface, Multimedia Audio Codec

Features

- Integrated parallel interface to ISA and EISA buses
- Stereo Digital Audio at sample rates from 4 kHz to 50 kHz with 16-bit resolution.
- DMA Transfers with on-chip FIFOs
- Free Window™ Software Drivers
- Linear, μ-law, and A-law coding
- Pin compatible with the AD1848 (PLCC)

General Description

The CS4248 is an Mwave™ audio codec.

The CS4248 is a mixed signal integrated circuit that provides 16-bit audio for computer multimedia systems. The CS4248 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data. The CS4248 combines conversion, analog mixing, and programmable gain and attenuation to provide a complete audio subsystem in a single 68-pin PLCC or 100-pin TQFP package. The CS4248 includes an 8-bit parallel interface to the industry standard ISA bus.

ORDERING INFORMATION:

Model	Temp. Range	Package Type
CS4248-KL	0 to 70° C	68 pin PLCC
CS4248-KQ	0 to 70° C	100 pin TQFP

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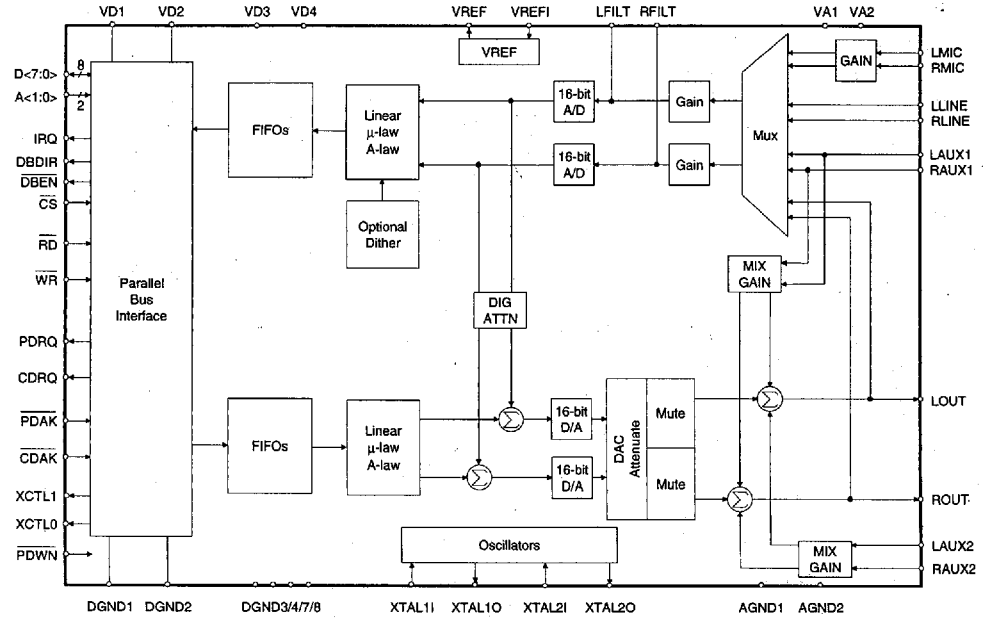

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine wave; Conversion Rate = 48 kHz; Measurement Bandwidth is 10 Hz to 20 kHz, 16-bit linear coding.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution	(Note 1)		16	-	-	Bits
ADC Differential Nonlinearity	(Note 1)		-	-	±0.5	LSB
Instantaneous Dynamic Range	Line Inputs (Note 2) Mic Inputs	IDR	80 72	85 77	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	0.02 0.025	0.003 0.01	- -	% %
Signal-to-Intermodulation Distortion			-	90	-	dB
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs Line-to-AUX1 Line-to-AUX2		- - - -	80 80 90 90	- - - -	dB dB dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Programmable Input Gain Span	Line Inputs		21.5	22.5	-	dB
Gain Step Size			1.3	1.5	1.7	dB
ADC Offset Error	0 dB gain		-	10	100	LSB
Gain Error			-	-	5	%
Full Scale Input Voltage:	(MGE=1) MIC Inputs (MGE=0) MIC Inputs LINE, AUX1, AUX2 Inputs		0.266 2.66 2.66	0.29 2.9 2.9	0.31 3.1 3.1	V_{pp} V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 1)		20	-	-	kΩ
Input Capacitance	(Note 1)		-	-	15	pF

Notes: 1. This specification is guaranteed by characterization, not production testing.
2. MGE = 1 and a 10µF capacitor on the VREF pin.

* Parameter definitions are given at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation (0 dB); Unless Otherwise Specified.							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity		(Note 1)		-	-	±0.5	LSB
Dynamic Range	- Total	All Outputs	TDR	-	95	-	dB
	- Instantaneous		IDR	80	85	-	dB
Total Harmonic Distortion		(Note 4)	THD	0.02	0.01	-	%
Signal-to-Intermodulation Distortion				-	85	-	dB
Interchannel Isolation	Line Out	(Note 4)		-	95	-	dB
Interchannel Gain Mismatch		Line Out		-	0.1	0.5	dB
Voltage Reference Output				2.0	2.15	2.3	V
Voltage Reference Output Current		(Note 3)		-	100	-	µA
DAC Programmable Attenuation Span				93	94.5	-	dB
DAC Attenuation Step Size		0 dB to -81 dB		1.3	1.5	1.7	dB
		-82.5 dB to -94.5 dB		1.0	1.5	2	dB
DAC Offset Voltage				-	1	10	mV
Full Scale Output Voltage		(Notes 4, 5)		1.85	2.0	2.25	V_{pp}
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase		(Note 1)		-	-	1	Degree
External Load Impedance				10	-	-	kΩ
Mute Attenuation (0 dB)				80	-	-	dB
Total Out-of-Band Energy	(Note 1)	0.6×Fs to 3 MHz		-	-	-45	dB
Audible Out-of-Band Energy	(Fs = 8kHz)	0.6×Fs to 22 kHz		-	-	-60	dB
Power Supply							
Power Supply Current		Digital, Operating		-	55	65	mA
		Analog, Operating		-	43	60	mA
		Total		-	98	120	mA
		Digital, Power Down		-	-	1	mA
		Analog, Power Down		-	-	1	mA
Power Supply Rejection	1kHz	(Note 1)		40	-	-	dB

Notes: 3. DC current only. If dynamic loading exists, then the voltage reference output must be buffered or the performance of ADCs and DACs will be degraded.
4. 10 kΩ, 100 pF load.
5. The output level full-scale value is 3 dB below the input full-scale value. This attenuation is not taken into account in the mixer gain tables which show gain internal to the mixer.

AUXILIARY INPUT MIXERS (T_A = 25°C; VA1, VA2, VD1-VD4 = +5V; Input Levels: Logic 0 = 0V, Logic 1 = VD1-VD4; 1 kHz Input Sine Wave)

Parameter			Symbol	Min	Typ	Max	Units
Mixer Gain Range Span	AUX1, AUX2	(Note 6)		45	46.5	-	dB
Step Size	AUX1, AUX2			1.3	1.5	1.7	dB

Note: 6. An addition 3 dB attenuation must be included when comparing the output value to the input value since the analog output full-scale value is 3 dB lower than the analog input full-scale value.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital	VD1-VD4	-0.3	6.0	V
	Analog	VA1,VA2	-0.3	6.0	V
Input Current Per Pin	(Except Supply Pins)		-10	10	mA
Output Current Per Pin	(Except Supply Pins)		-50	50	mA
Analog Input Voltage			-0.3	VA+0.3	V
Digital Input Voltage			-0.3	VD+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital	VD1-VD4	4.75	5.0	5.25	V
	Analog	VA1,VA2	4.75	5.0	5.25	V
Operating Ambient Temperature		T_A	0	25	70	°C

DIGITAL FILTER CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Passband			0	-	0.40xFs	Hz
Frequency Response			-0.5	-	+ 0.2	dB
Passband Ripple	(0-0.4xFs)		-	-	±0.1	dB
Transition Band			0.40xFs	-	0.60xFs	Hz
Stop Band			0.60xFs	-	-	Hz
Stop Band Rejection			74	-	-	dB
Group Delay			-	-	30/Fs	s
Group Delay Variation vs. Frequency	ADCs DACs		- -	- -	0.0 0.1/Fs	µs µs

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DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1-VD4 = 5V; AGND1, AGND2, DGND1-DGND4, DGND7, DGND8 = 0V.)

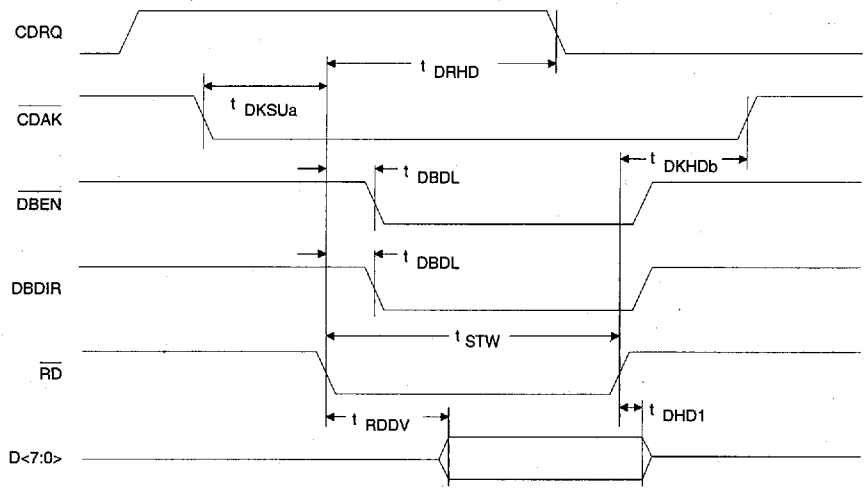
Parameter			Symbol	Min	Max	Units
High-level Input Voltage		Digital Inputs XTAL1I/XTAL2I, $\overline{PDWN}$	V_{IH}	2.0 VD-1.0	VD+ 0.3 VD+ 0.3	V V
Low-level Input Voltage			V_{IL}	-0.3	0.8	V
High-level Output Voltage:	D<7:0> All Others	I_O = -16.0 mA I_O = -1.0 mA	V_{OH}	2.4 2.4	VD VD	V V
Low-level Output Voltage:	D<7:0> All Others	I_O = 16.0 mA I_O = 4.0 mA	V_{OL}	- -	0.4 0.4	V V
Input Leakage Current		(Digital Inputs)	-	-10	10	µA
Output Leakage Current		(High-Z Digital Outputs)	-	-10	10	µA

TIMING PARAMETERS

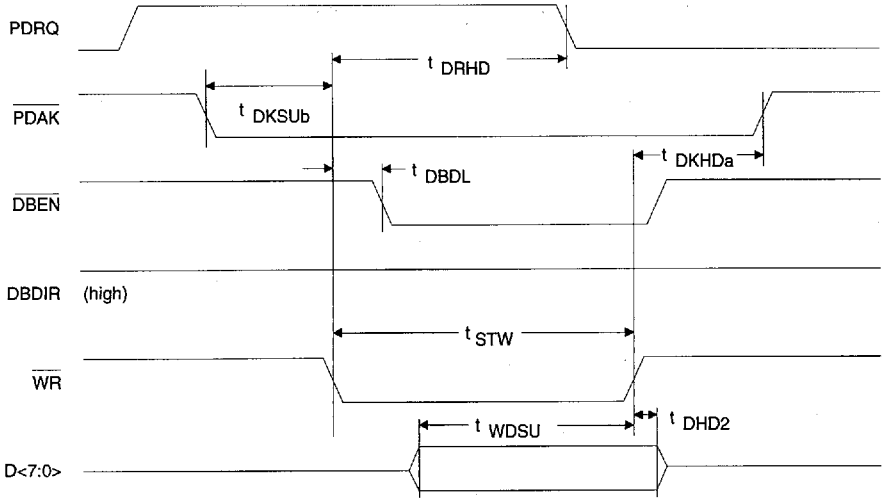
Parameter	Description		Min	Max	Units
t_{STW}	$\overline{WR}$ or $\overline{RD}$ strobe width		90	-	ns
t_{WDSU}	Data valid to $\overline{WR}$ rising edge	(write cycle)	22	-	ns
t_{RDDV}	$\overline{RD}$ falling edge to data valid	(read cycle)	-	60	ns
t_{CSSU}	$\overline{CS}$ setup to $\overline{WR}$ or $\overline{RD}$ falling edge		10	-	ns
t_{CSHD}	$\overline{CS}$ hold from $\overline{WR}$ or $\overline{RD}$ rising edge		0	-	ns
t_{ADSU}	ADDR <> setup to $\overline{RD}$ or $\overline{WR}$ falling edge		22	-	ns
t_{ADHD}	ADDR <> hold from $\overline{WR}$ or $\overline{RD}$ rising edge		10	-	ns

TIMING PARAMETERS (continued)

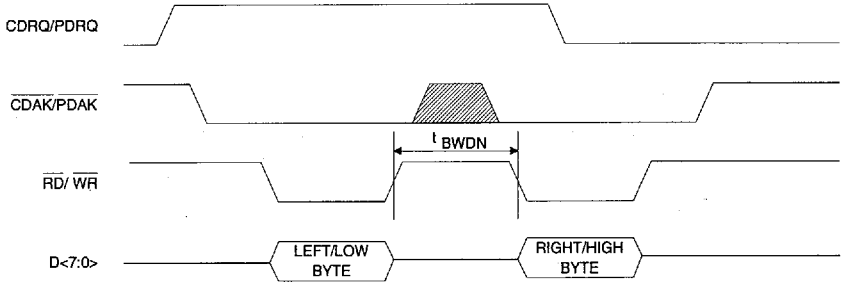
Parameter	Description	Min	Max	Units
t_{SUDK1}	$\overline{DAK}$ inactive to $\overline{WR}$ or $\overline{RD}$ falling edge (DMA cycle completion immediately followed by a PIO cycle)	60	-	ns
t_{SUDK2}	$\overline{DAK}$ active from $\overline{WR}$ or $\overline{RD}$ rising edge (PIO cycle completion immediately followed by DMA cycle)	0	-	ns
t_{DKSUa} t_{DKSUb}	$\overline{DAK}$ setup to $\overline{RD}$ falling edge (DMA cycles) $\overline{DAK}$ setup to $\overline{WR}$ falling edge	25 25	- -	ns ns
t_{DHD2}	Data hold from $\overline{WR}$ rising edge	15	-	ns
t_{DRHD}	DRQ hold from $\overline{WR}$ or $\overline{RD}$ falling edge (assumes no more DMA cycles needed)	0	25	ns
t_{BWDN}	Time between rising edge of $\overline{WR}$ or $\overline{RD}$ to next falling edge of $\overline{WR}$ or $\overline{RD}$	80	-	ns
t_{DHD1}	Data hold from $\overline{RD}$ rising edge	0	20	ns
t_{DKHDa} t_{DKHDb}	$\overline{DAK}$ hold from $\overline{WR}$ rising edge $\overline{DAK}$ hold from $\overline{RD}$ rising edge	25 25	- -	ns ns
t_{DBDL}	$\overline{DBEN}$ or $\overline{DBDIR}$ active from $\overline{WR}$ or $\overline{RD}$ falling edge		40	ns
t_{PDWN}	$\overline{PDWN}$ pulse width low	200	-	ns



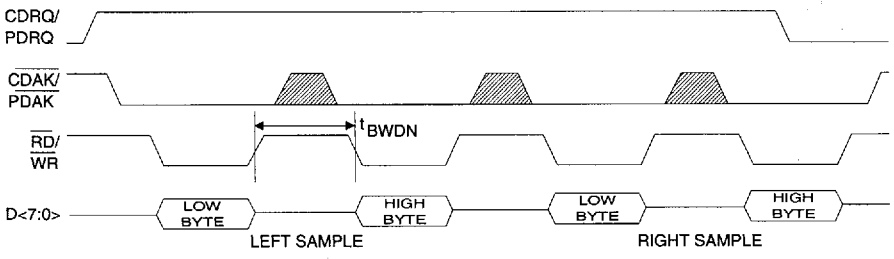
8-Bit Mono DMA Read/Capture Cycle



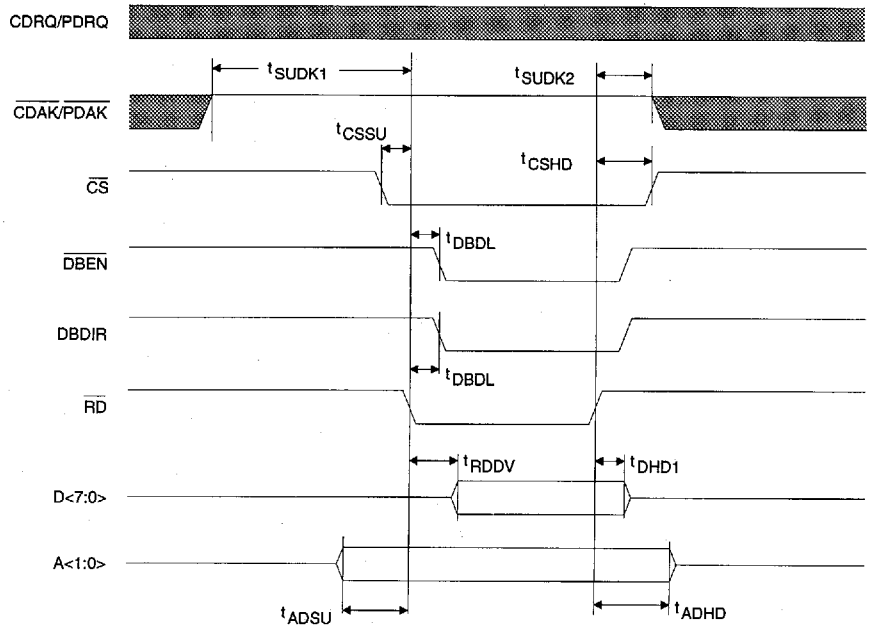
8-Bit Mono DMA Write/Playback Cycle



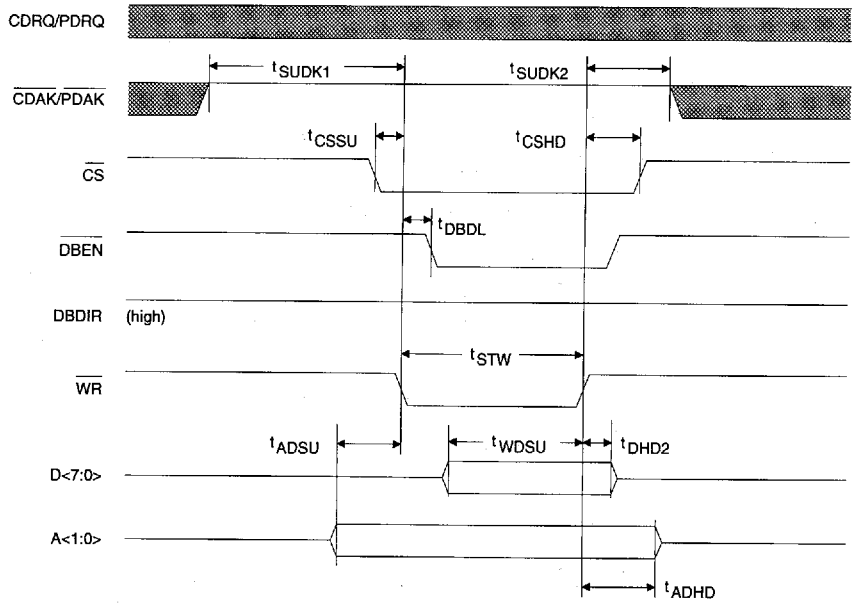
8-Bit Stereo or 16-Bit Mono DMA Cycle



16-Bit Stereo DMA Cycle



I/O Read Cycle



I/O Write Cycle

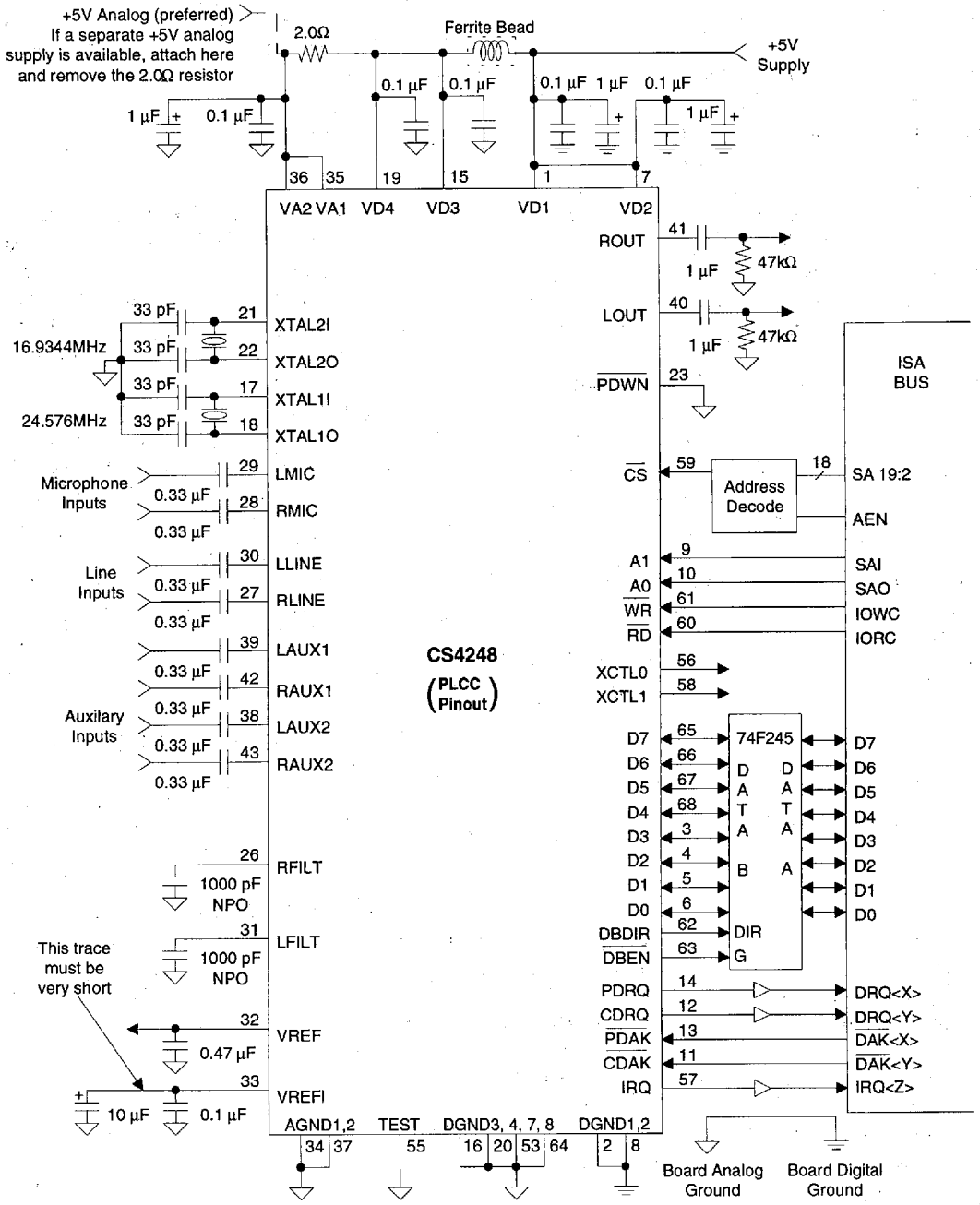


Figure 1. Recommended Connection Diagram
(See also Figures 9 & 10 for Layout Recommendations)

GENERAL DESCRIPTION

The CS4248 is a monolithic integrated circuit that provides audio in personal computers or other parallel interface environments. The functions include stereo Analog-to-Digital and Digital-to-Analog Converters (ADC and DAC), analog mixing, anti-aliasing and reconstruction filters, line and microphone level inputs, selectable A-law / μ-law coding, and a parallel bus interface. Three stereo analog inputs, LINE, MIC, and AUX1, are provided and can be multiplexed to the ADC. AUX1 can be mixed with the output of the DAC along with an additional auxiliary input (AUX2). The only external filtering required is two capacitors. Several data modes are supported including 8- and 16-bit linear as well as 8-bit companded. The CS4248 is packaged in a 68-pin PLCC or a 100-pin TQFP.

A number of innovative design techniques are used to minimize audible noise from external sources, data handling errors and during normal operating changes such as volume control. In the event that a data error does occur, the CS4248 provides smooth error masking and eliminates pops and clicks.

FUNCTIONAL DESCRIPTION

Parallel Data Interface

The 8-bit parallel port of the CS4248 provides an interface which is compatible with most computer peripheral busses. The model for this interface is the Industry Standard Architecture (ISA) bus, but the CS4248 will easily interface to other buses such as EISA and micro channel. Two types of accesses can occur via the parallel interface; Programmed I/O (PIO) access, and DMA access.

There is no provision for the CS4248 to "hold off" or extend a cycle occurring on the parallel interface. Therefore, the internal architecture of the CS4248 accepts asynchronous parallel bus cycles without interfering with the flow of data to or from the ADC and DAC sections.

Control Registers Interface

The first I/O cycle access is to the control registers of the CS4248. Timing diagrams are given to show the timing of control register cycles. The $\overline{RD}$ and $\overline{WR}$ signals are used to define the read and write cycles respectively. The control register cycle is defined by the assertion of the CS4248 $\overline{CS}$ signal while the DMA acknowledge signals, $\overline{CDAK}$ and $\overline{PDAK}$, are inactive. For read cycles, the CS4248 will drive data on the DATA lines while the host asserts the $\overline{RD}$ strobe. Write cycles require the host to assert data on the DATA lines and strobe the $\overline{WR}$ signal. The CS4248 will latch data into the control register on the rising edge of the $\overline{WR}$ strobe. The CS4248 $\overline{CS}$ signal should remain active until after completion of the read or write cycle. PIO cycles (non-DMA) are the only type which access the Control Registers.

The data interface typically uses DMA request/grant pins to transfer the digital audio data between the CS4248 and the bus. The CS4248 is responsible for asserting a request signal whenever the CS4248's internal buffers need updating. The logic interfaced with the CS4248 responds with an acknowledge signal and strobes data to and from the CS4248, 8 bits at a time. The CS4248 keeps the request pin active until the appropriate number of 8-bit cycles have occurred to transfer one audio sample. Notice that different audio data types will require a different number of 8-bit transfers.

DMA Interfaces

The second type of parallel bus cycle on the CS4248 is a DMA transfer. DMA cycles are distinguished from control register cycles by the assertion by the CS4248 of a CDRQ (or PDRQ)

followed by an acknowledgment by the host by the assertion of $\overline{CDAK}$ (or $\overline{PDAK}$). While the acknowledgment is received from the host, the CS4248 assumes that any cycles occurring are DMA cycles and ignores the addresses on the address lines and the $\overline{CS}$ line.

The CS4248 may assert the DMA request signal at any time. Once asserted, the DMA request will remain asserted until a DMA cycle occurs to the CS4248. Once the falling edge of the final $\overline{WR}$ or $\overline{RD}$ strobe of a full sample of a DMA cycle occurs, the DMA request signal is deasserted immediately. DMA transfers may be terminated by resetting the PEN and/or CEN bits in the Interface Configuration Register, depending on the DMA that is in progress (Playback, Capture, or Both). Termination of DMA transfers may only happen between sample transfers on the bus. If PDRQ and/or CDRQ goes active while resetting PEN and/or CEN, the request must be acknowledged ($\overline{PDAK}$ and/or $\overline{CDAK}$) and a final sample transfer completed. The CS4248 supports one or two DMA channels.

Dual Channel DMA Mode

In dual-channel mode, playback and capture DMA requests and acknowledges occur on independent DMA channels. In this mode, capture and playback are enabled and set for DMA transfers. In addition, the SDC bit must be set to zero. The playback and capture enables can be changed without a mode change enable. This allows proper control where applications are independently using playback and capture. Simultaneous capture and playback is not plausible.

Single Channel DMA (SDC) Mode

SDC mode is designed to allow the CS4248 to be used in a computer where two dedicated DMA channels for audio are not available. SDC forces all DMA transfers (capture or playback) to occur on a single DMA channel (the playback channel).

To enable the SDC mode, set the SDC bit (Index 9) to one in the Interface Configuration register. With the SDC bit asserted, the internal workings of the CS4248 remain exactly the same as dual mode, except for the manner in which DMA request and acknowledges are handled.

The playback of audio data will occur on the playback channel exactly as dual channel operation. However, the capture audio channel is now diverted to the playback channel. This means that the capture DMA request occurs on the PDRQ pin and the $\overline{PDAK}$ pin is used to acknowledge the capture request. Simultaneous DMA capture and playback is not plausible. If both playback and capture are enabled, the default will be playback.

In SDC mode, the CDRQ pin is logic low (inactive). The $\overline{CDAK}$ pin is ignored by the CS4248. SDC does not have any affect when using Programmed I/O mode.

Interrupt

Interrupts are generated under control of the Current Count register. The Current Count register is not accessible by the host, but is loaded when a write occurs to the upper byte of the Base Count Register. Note that the Base Count registers should be loaded with the buffer size minus one. The Current Count Register decrements on every sample period. Once the Current Count register reaches zero, an interrupt is generated on the next sample.

The INT bit of this Status Register always reflects the status of the CS4248 internal interrupt state. A roll-over from Current Count register sets the INT bit. This bit remains set until cleared by a write of ANY value to Status register.

The Interrupt Enable (IEN) bit in the Pin Control register determines whether the interrupt pin responds to the interrupt event in the CS4248. When the IEN bit has the interrupt disabled, the IRQ pin of the CS4248 is forced low and does not change. However, the INT bit of the status register always responds to the counter.

Error Conditions

Data overrun or underrun could occur if data is not supplied to or read from the CS4248 in an appropriate amount of time. The amount of time for such data transfers depends on the frequency selected within the CS4248.

Should an overrun condition occur during data capture, the last whole sample (before the overrun condition) will be read by the DMA interface. A sample will not be overwritten while the DMA interface is in the process of transferring the sample.

Should an underrun condition occur in a playback case the last valid sample will be output to the digital mixer. This will mask short duration error conditions. When the next complete sample arrives from the host computer the data stream will resume on the next sample clock.

Noise Management

The CS4248 includes circuitry for noise management resulting from power up and down transients. No audible clicks and pops occur due to power up and down transients or when entering power down mode.

Analog Input Interface

The analog input interface is designed to accommodate four stereo input sources. Three of these sources are multiplexed to the ADC. These inputs are: the stereo line level input, the microphone input, and an auxiliary line level input (AUX1). AUX1 and AUX2 can be analog mixed with the DAC outputs. All audio inputs should be capacitively coupled to the CS4248.

Microphone Level Inputs

The CS4248 includes an selectable +20 dB gain stage for interfacing to an external microphone. Figure 2 shows an example microphone input buffer circuit.

Analog Output Interface

The analog output section of the CS4248 provides a stereo line level output. The other output types (headphone and speaker) are implemented with external circuitry. Left and Right outputs should be capacitively coupled to external circuitry.

Miscellaneous Signals

Four pins have been allocated to allow the interfacing of two crystal oscillator circuits to the CS4248. These pins are XTAL1I, XTAL1O, XTAL2I, AND XTAL2O.

A $\overline{\text{PDWN}}$ signal places the CS4248 into maximum power conservation mode. A 2.1 V reference pin is provided to maintain an audio reference level for single supply input and output audio signals; however, this reference is not maintained in power-down mode.

The $\overline{\text{DBEN}}$ and DBDIR pins are used to control an external data buffer to the CS4248. The CS4248 is capable of driving a 16 mA bus load. Data bus loading requirements greater than 16 mA will require an external buffer. $\overline{\text{DBEN}}$ enables the external drivers and DBDIR controls the direction of the data flow.

CONTROL REGISTER DEFINITION

The two address pins of the CS4248 allow access to four 8-bit registers. Two of these registers allow indirect accessing to more CS4248 registers via an index and data register. The other two registers provide status information and allow direct access to the CS4248's digital audio data without the need to perform DMA cycles.

Changing Transfer Modes

The CS4248 must be in Mode Change Enable Mode (MCE=1) before any changes to the Interface Configuration register or the Data Format register are allowed. The exceptions are CEN and PEN which can be changed "on-the-fly" via programmed I/O writes to these bits. All outstanding DMA transfers must be completed before new values of CEN or PEN are recognized.

Digital Loopback

Digital Loopback is enabled via the LBE bit in the Loopback Control register and can be used to monitor the record path during a capture sequence. This loopback routes the digital data from the ADCs to the DACs. This loopback can be digitally attenuated via additional bits in the Loopback Control register. Loopback is then summed with DAC data supplied at the digital bus interface. When loopback is enabled, it will "freerun" synchronous with the sample rate. The digital loopback is shown in the CS4248 block diagram on the front page of this data sheet.

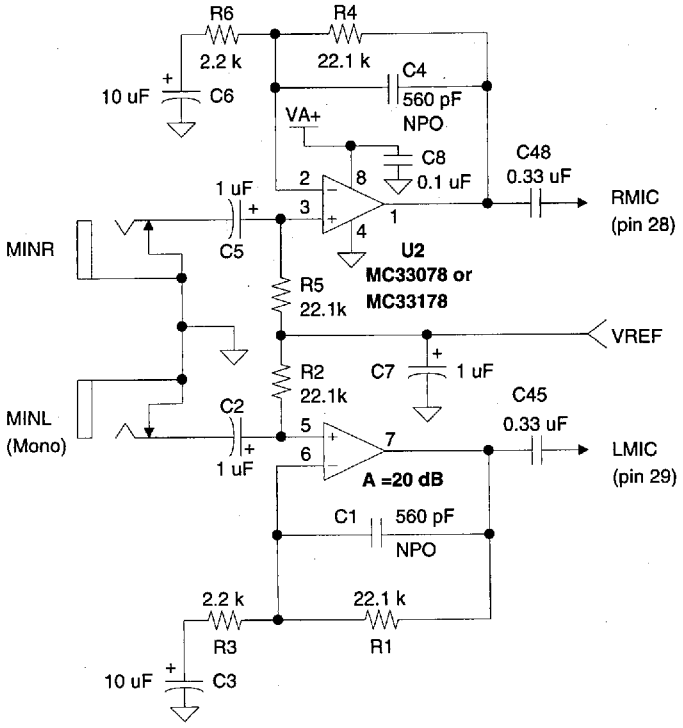


Figure 2. Optional Microphone Input Buffer.

If the sum of the loopback and bus data are greater than full scale, CS4248 will send a + or - full scale value to the DACs whichever is appropriate. (Clipping)

INITIALIZATION AND PROCEDURES

Reset and Power down

Reset and power down modes are controlled by the $\overline{\text{PDWN}}$ pin. To put the CS4248 into a power down mode, the $\overline{\text{PDWN}}$ pin is pulled low. In this state the host interface is inactive and all digital and analog circuits are turned off.

To let the CS4248 go through its reset initialization the $\overline{\text{PDWN}}$ pin should be set high. This rising edge starts the initialization process. While the CS4248 is initializing, all reads by the host computer will receive a 80 hex. All writes during initialization of the CS4248 will be ignored. At the end of the initialization, all registers are set to known values as documented in the register definition section.

Auto Calibration

The CS4248 has the ability to calibrate the ADCs and DACs. Auto-calibration is initiated when MCE goes from 1 to 0 with the ACAL bit in the Interface Configuration register set.

The completion of calibration can be determined by polling the Auto-calibrate In-Progress (ACI) bit in the Test and Initialization register. This bit will be high while the calibration is in progress and low once completed. The calibration sequence will take at least 128 sample periods. Transfers enabled during calibration will not begin until calibration has completed.

The calibration procedure is as follows:

1) Place the CS4248 in Mode Change Enable using the MCE bit of the Index register.

2) Set the ACAL bit in the Interface Configuration register.

3) Return from Mode Change Enable by resetting the MCE bit of the Index register.

4) Poll the ACI bit in the Test and Initialization register for a one (active) then poll for a zero (complete).

Changing Sampling Rate

The internal states of the CS4248 are synchronized by the selected sampling frequency defined in the Data Format register. If only one crystal is provided in hardware, it must be XTAL1. The changing of the clock source requires a special sequence for proper CS4248 operation.

1) Mute the outputs of the CS4248 and place it in Mode Change Enable using the MCE bit of the Index register.

2) During a single write cycle, change the Clock Frequency Divide Select (CFS) and/or Clock Source Select (CSL) bits of the Data Format register to the desired values.

3) The CS4248 resynchronizes its internal states to the new clock. During this time the CS4248 will be unable to respond at its parallel interface. Writes to the CS4248 will not be recognized and reads will always return the value 80 hex.

4) The host now polls the CS4248's Index register until the value 80 hex is no longer returned.

5) Once the CS4248 is no longer responding to reads with a value of 80 hex, normal operation can resume and the CS4248 can be removed from MCE.

6) If ACAL is set, proceed with Auto Calibration steps previously mentioned.

The CSL and CFS[2..0] bits cannot be changed unless the MCE bit has been set. Attempts to change the Data Format register or Interface Configuration register without MCE set, will not be recognized.

DATA STREAM DEFINITION

The CS4248 is designed for data formats which are in "little endian" format. This format defines the byte ordering of a multibyte word as having the least significant byte occupying the lowest memory address. Likewise, the most significant byte of a little endian word occupies the highest memory address.

The CS4248 always orders the left channel data before the right channel. Note that these definitions apply regardless of the specific format of the data. For example, 8-bit linear data streams look exactly like 8-bit companded data streams. Also, the left sample always comes first in the data stream regardless of whether the sample is 16-bit or 8-bit in size. See Figures 3 through 6.

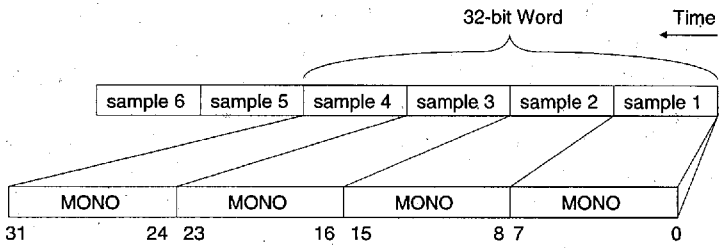


Figure 3. 8-bit Mono, Data Stream Definition.

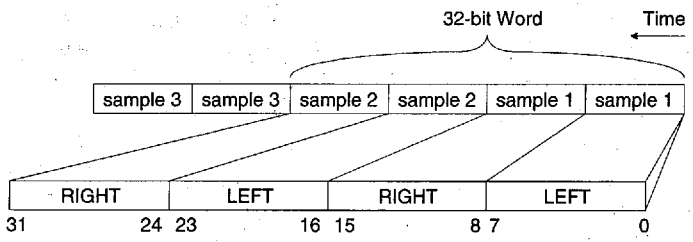


Figure 4. 8-bit Stereo, Data Stream Definition.

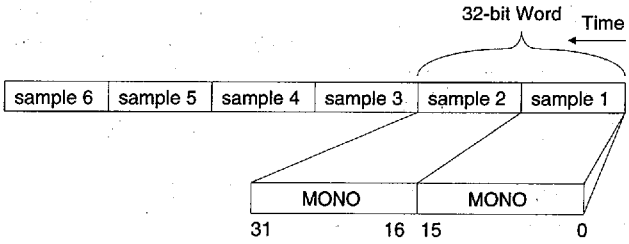


Figure 5. 16-bit Mono, Data Stream Definition.

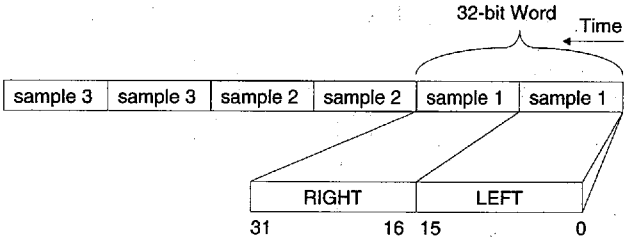


Figure 6. 16-bit Stereo, Data Stream Definition.

Data Format Definition

There are four data formats supported by the CS4248: 16-bit signed, 8-bit unsigned, 8-bit companded μ-Law, and 8-bit companded A-Law.

16-bit Signed

The 16-bit signed format (also called 16-bit two's-complement) is the standard method of representing 16-bit digital audio. This format gives 96 dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent minimum analog amplitude while 32767 (7FFFh) represents maximum analog amplitude.

8-bit Unsigned

The 8-bit unsigned format is commonly used in the personal computer industry. This format delivers a theoretical dynamic range of 48 dB. This format uses the value 0 (00h) to represent minimum analog amplitude while 255 (FFh) represents maximum analog amplitude. 16-bit signed and 8-bit unsigned formats are shown in Figure 7. When using A/D converters of higher resolution (16-bits) to generate 8-bit values, truncating can produce correlated noise artifacts which can be disturbing to the listener. Once the data is truncated to 8 bits, it is impossible to remove these artifacts. The CS4248 contains an optional dither bit in indirect register 10. When the dither bit is set, a triangular pdf dither is added to the internal 16-bit ADC before truncating to the 8-bit value. Dither is only used for the ADCs when the 8-bit unsigned data format is selected. This dither removes the correlation between the noise and the signal with a slight increase in the noise floor.

8-bit Companded

The 8-bit companded formats (A-law and μ-law) come from the telephone industry. μ-law is the standard for the United States/Japan while A-law is used in Europe. Companded audio allows either 64 dB or 72 dB of dynamic range using only 8 bits per sample. This is accomplished using a non-linear companding which assigns more digital codes to lower amplitude analog signals with the sacrifice of precision on higher amplitude signals. The μ-law and A-law formats of the CS4248 conform to the CCITT G.711 specifications. Figure 8 is a diagram of approximately how both A- and μ-law behave. Please refer to the standard mentioned above for an exact definition.

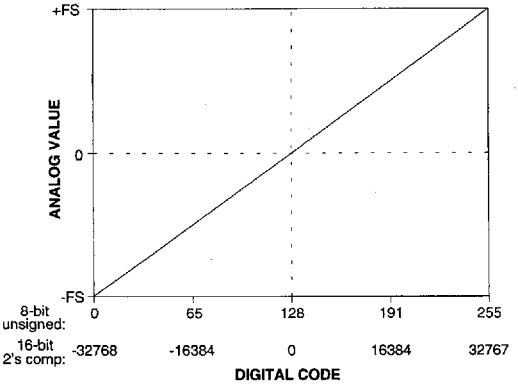


Figure 7. 16-bit Signed, 8-bit Unsigned Formats.

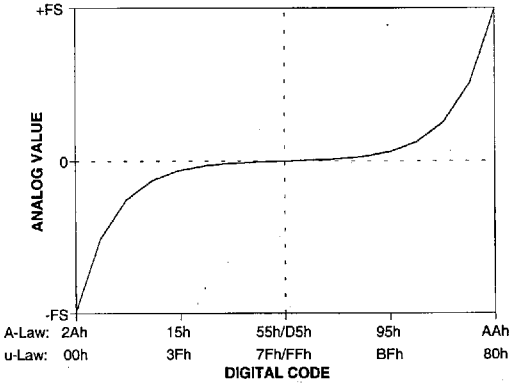


Figure 8. 8-bit A-Law, μ-Law Formats.

CS4248 REGISTER MAPPING

Addr.	Register Name
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Register

Table 1. Direct Registers

Index	Register Name
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left Output Control
7	Right Output Control
8	Data Format
9	Interface Configuration
10	Pin Control
11	Test and Initialization
12	Misc. Information
13	Loopback Control
14	Upper Base Count
15	Lower Base Count

Table 2. Indirect Registers

Physical Mapping

The control registers are mapped via partial indirect mapping. Two address bits are defined to access all of the CS4248's registers. The four direct registers are shown in Table 1. The first two direct registers are used to access 16 indirect registers as shown in Table 2. Table 3 details a summary of each bit in each register. The detailed register descriptions are described in this section. Tables 4 through 6 illustrate all the programmable gain block decodes and is included here for reference. These gain tables will be referred to under the description for the particular register.

Index Register

D7	D6	D5	D4	D3	D2	D1	D0
INIT	MCE	TRD	res	IA3	IA2	IA1	IA0

IA3-IA0 — Index Address: These bits define the address of the CS4248 register accessed by the Indexed Data Register. These bits are read/write.

res — Reserved for future expansion. Always write zero to this bit.

MCE — Mode Change Enable: This bit must be set whenever the current mode of the CS4248 is changed. The Data Format and Interface Configuration registers CANNOT be changed unless this bit is set. The exceptions are CEN and PEN which can be changed "on-the-fly". No audio activity will occur when this bit is set.

TRD — Transfer Request Disable: This bit, when set, causes DMA transfers to cease when the INT bit of the status register is set.

0 - Transfers Enabled (PDRQ and CDRQ occur uninhibited)
1 - Transfers Disabled (PDRQ and CDRQ only occur if INT bit is 0)

INIT — CS4248 Initialization: This bit is read as 1 when the CS4248 is in a state which it cannot respond to parallel interface cycles. This bit is read-only.

Immediately after RESET (and once the CS4248 has left the INIT state), the state of this register is: 010X0000 (40h)

During CS4248 initialization, this register CANNOT be written and is always read 10000000 (80h)

Indexed Data Register

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7-ID0 Indexed Register Data: These bits are the data the CS4248 register referenced by the Indexed Data register.

During CS4248 initialization, this register can NOT be written and is always read 10000000 (80h)

I/O Data Register

The PIO Data register is two registers mapped to the same address. Writes to this register sends data to the Playback Data register. Reads from this register will receive data from the Capture Data register.

During CS4248 initialization, this register CANNOT be written and is always read 10000000 (80h)

Capture Data Register (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0

CD7-CD0 Capture Data Port. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status register. Once all relevant bytes have been read, the state machine will point to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, and a read of the status has occurred, the state machine and status register will point to the first byte of the new sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

During CS4248 initialization, this register can NOT be written and is always read 10000000 (80h)

Playback Data Register (Write Only)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

PD7-PD0 Playback Data Port. This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Status Register

D7	D6	D5	D4	D3	D2	D1	D0
CU/L	CL/R	CRDY	SER	PU/L	PL/R	PRDY	INT

INT — Interrupt Status: This indicates the status of the internal interrupt logic of the CS4248. This bit is cleared by any write of any value to this register. The IEN bit of the Pin Control register determines whether the state of this bit is reflected on the IRQ pin of the CS4248. Read States

0 - Interrupt pin inactive
1 - Interrupt pin active

PRDY — Playback Data Register Ready. The Playback Data register is ready for more data. This bit would be used when direct programmed I/O data transfers are desired. (This bit is Read-Only)

0 - Data still valid. Do not overwrite.
1 - Data stale. Ready for next host data write value.

PL/$\overline{R}$ — Playback Right/Left Sample: This bit indicates whether data needed is for the Right channel or Left channel. (This bit is Read-Only)

0 - Right Channel Data
1 - Left Channel Data or Mono selected

PU/$\overline{L}$ — Playback Upper/Lower Byte: This bit indicates whether the playback data needed is for the upper or lower byte of the channel. (This bit is Read-Only)

0 - Lower Byte Needed
1 - Upper Byte Needed or any 8-bit mode

SER — Sample Error: This bit indicates that a sample was not serviced in time and therefore an error has occurred. The bit indicates an overrun for capture and underrun for playback. If both the capture and playback are enabled, the source which set this bit can not be determined. (This bit is Read-Only)

CRDY — Capture Data Ready. The Capture Data register contains data ready for reading by the host. This bit would be used for direct programmed I/O data transfers. (This bit is a Read-Only)

0 - Data is stale. Do not reread the information.
1 - Data is fresh. Ready for next host data read.

CL/$\overline{R}$ — Capture Left/Right Sample: This bit indicates whether the capture data waiting is for the Right channel or Left channel. (This bit is Read-Only)

0 - Right Channel Data
1 - Left Channel Data or mono

CU/$\overline{L}$ — Capture Upper/Lower Byte: This bit indicates whether the capture data ready is for the upper or lower byte of the channel. (This bit is Read-Only)

0 - Lower byte ready
1 - Upper byte ready or any 8-bit mode

The PRDY and CRDY bits are designed to be read as one when action is required by the host. For example, when PRDY is set to one the device is ready for more data, or when the CRDY is set to one data is available to the host. The definition of the CRDY and PRDY bits are therefore consistent in this regard.

Indirect Mapped Registers

These registers are accessed by placing the appropriate index in the Index register and then accessing the Index Data register. A detailed description of each of the registers is given below. All reserved bits should be written zero and may be 0 or 1 when read back

Input Control Registers

Left Input Control (Index 0)

D7	D6	D5	D4	D3	D2	D1	D0
LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0

LIG3-LIG0 Left input gain select. The least significant bit of this gain select represents 1.5 dB. See Table 4.

LMGE Left Input Mic Gain Enable: This bit will enable the 20 dB gain of the left mic input signal.

LSS1-LSS0 Left input source select. These bits select the input source for the left gain stage going to the left ADC.

0 - Left Line
1 - Left Auxiliary 1
2 - Left Microphone
3 - Left Line Output Loopback

This register's initial state after reset is: 000x0000

Right Input Control (Index 1)

D7	D6	D5	D4	D3	D2	D1	D0
RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0

RIG3-RIG0 Right input gain select. The least significant bit of this gain select represents 1.5 dB. See Table 4.

RMGE Right Input Mic Gain Enable: This bit will enable the 20 dB gain of the right mic input signal.

RSS1-RSS0 Right input source select. These bits select the input source for the right channel gain stage going to the right ADC.

0 - Right Line
1 - Right Auxiliary 1
2 - Right Microphone
3 - Right Line Out Loopback

This register's initial state after reset is: 000x0000

Left Auxiliary #1 Input Control (Index 2)

D7	D6	D5	D4	D3	D2	D1	D0
LX1M	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4-LX1G0 Left Auxiliary #1 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

LX1M Left Auxiliary #1 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #1 input source.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #1 Input Control (Index 3)

D7	D6	D5	D4	D3	D2	D1	D0
RX1M	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4-RX1G0 Right Auxiliary #1 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

RX1M Right Auxiliary #1 Mute. This bit, when set to 1, will mute the right channel of the Auxiliary #1 input source.

This register's initial state after reset is: 1xx01000.

Left Auxiliary #2 Input Control (Index 4)

D7	D6	D5	D4	D3	D2	D1	D0
LX2M	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4-LX2G0 Left Auxiliary #2 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

LX2M Left Auxiliary #2 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #2 input source.

This register's initial state after reset is: 1xx01000.

Right Auxiliary #2 Input Control (Index 5)

D7	D6	D5	D4	D3	D2	D1	D0
RX2M	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4-RX2G0 Right Auxiliary #2 Mix Gain Select. The least significant bit of this gain select represents 1.5 dB. See Table 5.

RX2M Right Auxiliary #2 Mute. This bit, when set to 1, will mute the right channel of the Auxiliary #2 input source.

This register's initial state after reset is: 1xx01000.

Output Control Registers

Left Output Control (Index 6)

D7	D6	D5	D4	D3	D2	D1	D0
LOM	res	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0

LOA5-LOA0 Left Output Attenuate Select. The least significant bit of this attenuate select represents -1.5 dB. Full attenuation is at least -94.5 dB. See Table 6.

LOM Left Output Mute. This bit, when set to 1, will mute the left DAC channel output.

This register's initial state after reset is: 1x000000.

Right Output Control (Index 7)

D7	D6	D5	D4	D3	D2	D1	D0
ROM	res	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0

ROA5-ROA0 Right Output Attenuate Select. The least significant bit of this attenuate select represents -1.5 dB. Full attenuation must be at least -94.5 dB. See Table 6.

ROM Right Output Mute. This bit, when set to 1, will mute the right DAC output.

This register's initial state after reset is: 1x000000.

Data Format Register (Index 8)

D7	D6	D5	D4	D3	D2	D1	D0
res	FMT	C/$\overline{L}$	S/$\overline{M}$	CSF2	CFS1	CFS0	CSL

CSL Clock Source Select: These bits select the clock source used for the audio sample rates.
CAUTION: See note at end of this section about changing these bits

0 - XTAL1/ 24.576 MHz
1 - XTAL2/ 16.9344 MHz
Note: When only one crystal or clock source is provided in hardware,it must be XTAL1.

CFS2-CFS0 Clock Frequency Divide Select: These bits select the audio sample rate frequency. The actual audio sample rate depends on which Clock Source is selected and it's frequency.
CAUTION: See note below about changing bits

Divide	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0 - 3072	8.0 kHz	5.51 kHz
1 - 1536	16.0 kHz	11.025 kHz
2 - 896	27.42 kHz	18.9 kHz
3 - 768	32.0 kHz	22.05 kHz
4 - 448	N/A	37.8 kHz
5 - 384	N/A	44.1 kHz
6 - 512	48.0 kHz	33.075 kHz
7 - 2560	9.6 kHz	6.62 kHz

S/$\overline{M}$ Stereo/Mono Select: This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

0 - Mono
1 - Stereo

C/$\overline{L}$ Companded /Linear Select: This bit selects between a linear digital representation of the audio signal or a non-linear, companded format. The type of companded format is defined by the FMT bit.

0 - Linear 1 - Companded

FMT Format Select: This bit defines the exact format of the digital audio based on the state of the C/L bit.

C/$\overline{L}$=0	C/$\overline{L}$=1
Linear	Companded
0 - 8 bit, unsigned	0 - μ-Law
1 - 16-bit, signed	1 - A-law

This register's initial state after reset is: x0000000.

Note: The Contents of this register CANNOT be changed except when the CS4248 is in Mode Change Enable (MCE) is 1. If MCE is not one, writes to this register will be ignored.

Interface Configuration Register (Index 9)

D7	D6	D5	D4	D3	D2	D1	D0
CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

PEN Playback Enable. This bit enables playback. The CS4248 will generate PDRQ and respond to PDAK signals when this bit is enabled and PPIO=0. If PPIO=1, this bit enables PIO playback mode. PEN may be set and reset without setting the MCE bit.

0 - Playback Disabled (PDRQ and PIO inactive)
1 - Playback Enabled

CEN Capture Enabled. This bit enables the capture of data. The CS4248 will generate CDRQ and respond to CDAK signals when this bit is enabled and CPIO=0. If CPIO=1, this bit enables PIO capture mode. CEN may be changed without setting the MCE bit.

0 - Capture Disabled (CDRQ and PIO inactive)
1 - Capture Enabled

SDC Single DMA Channel: This bit will force BOTH capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be zero. This bit will allow the CS4248 to be used with only one DMA channel. Should both capture and playback be enabled in this mode, only the playback will occur. See the DMA section for further explanation.

0 - Dual DMA channel mode
1 - Single DMA channel mode

ACAL Auto calibrate Enable: This bit determines whether the CS4248 performs an auto calibrate whenever returning from the Mode Change Enable (MCE) bit being asserted. If the ACAL bit is not set, previous calibration values are used, and no calibration cycle takes place. Therefore, ACAL is normally set.

0 - No auto calibration
1 - Auto calibration allowed

PPIO Playback PIO Enable: This bit determines whether the playback data is transferred via DMA or PIO.

0 - DMA transfers only
1 - PIO transfers only

CPIO Capture PIO Enable: This bit determines whether the capture data is transferred via DMA or PIO.

0 - DMA transfers only
1 - PIO transfers only

Note: This register, except bits CEN and PEN, can only be written while in Mode Change Enable. See section on MCE for more details.

This register's initial state after reset is: 00xx1000

Pin Control Register (Index 10)

D7	D6	D5	D4	D3	D2	D1	D0
XCTL1	XCTL0	res	res	DEN	res	IEN	res

IEN — Interrupt Enable: This bit enables interrupts to occur on the interrupt pin. The Interrupt pin will reflect the value of the INT bit in the status register. The interrupt pin is active high.

0 - Interrupt Disabled
1 - Interrupt Enabled

DEN — Dither Enable: When this bit is set, triangular pdf dither is added before truncating the ADC 16-bit data to 8-bit unsigned data. Dither is only active in the 8-bit unsigned data format.

0 - Dither Disabled
1 - Dither Enabled

XCTL1, XCTL0 — XCTL Control: These bits are reflected on the XCTL1,0 pins of the CS4248

0 - TTL Logic Low on XCTL1,0 pins
1 - TTL Logic High on XCTL1,0 pins

This registers initial state after reset is: 00xx0x0x

Test and Initialization Register (Index 11)

D7	D6	D5	D4	D3	D2	D1	D0
COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1-ORL0 — Overrange Left Detect: These bits determine the overrange on the left input channel. (Read Only) These bits hold the peak value and are reset to "0" by a read of this register

0 - Greater than -1.5 dB underrange
1 - Between -1.5 dB and 0 dB underrange
2 - Between 0 dB and 1.5 dB overrange
3 - Greater 1.5 dB overrange

ORR1-ORR0 — Overrange Right Detect: These bits determine the overrange on the right input channel. (Read Only) These bits hold the peak value and are reset to "0" by a read of this register

0 - Greater than -1.5 dB underrange
1 - Between -1.5 dB and 0 dB underrange
2 - Between 0 dB and 1.5 dB overrange
3 - Greater than 1.5 dB overrange

DRS — DRQ Status: This bit indicates the current status of the PDRQ and CDRQ pins of the CS4248.

0 - CDRQ AND PDRQ are presently inactive
1 - CDRQ OR PDRQ are presently active

ACI — Auto calibrate In-Progress: This bit indicates the state of auto calibration (Read-Only)

0 - Auto calibration not in progress
1 - Auto calibration is in progress

PUR — Playback underrun: This bit is set when playback data has not arrived from the host in time to be played. As a result the last valid sample will be sent to the DAC. This bit is sticky and will set in in an error condition. This bit is cleared by a Status register read.

COR — Capture overrun: This bit is set when the capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample will be ignored. This bit is sticky and will stay set in an error condition. This bit is cleared by a Status register read.

The SER bit in the Status register is simply a logical OR of the COR and PUR bits. This enables a polling host CPU to detect an error condition while checking other status bits.

This register's initial state after reset is: 00000000

Misc. Information Register (Index 12)

D7	D6	D5	D4	D3	D2	D1	D0
1	res	res	res	ID3	ID2	ID1	ID0

ID3-ID0 — CS4248 ID: These four bits define the version of the CS4248. These bits are Read-Only

ID3-ID0 = 0001 Chip version "B"
ID3-ID0 = 1010 Chip version "C" and later.

This register's initial state after reset is: 1xxx0001 or 1xxx1010 based on chip version.

Loopback Control Register (Index 13)

D7	D6	D5	D4	D3	D2	D1	D0
LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	res	LBE

LBE — Loopback Enable: This bit will enable the loopback mode of the CS4248 from the ADC's output to the DACs. When enabled, the data from the ADC's are digitally mixed with other data being delivered to the DACs.

0 - Loopback disabled
1 - Loopback enabled

LBA5-LBA0 — Loopback Attenuation: These bits determine the attenuation of the loopback from ADC to DAC. Each attenuation step is -1.5 dB. See Table 7.

This register's initial state after reset is: 000000x0

DMA Count Registers

The DMA Count registers allow easier integration of the CS4248 in ISA systems. Peculiarities of the ISA DMA controller require an external count mechanism to notify the host CPU of a full DMA buffer via interrupt. The programmable DMA Count registers provides this service. This register should be loaded with the buffer size minus one.

The Base Count register contains the number of samples which occur before an interrupt is generated on the INT pin. The act of writing a value to the Upper Base register cause both Base registers to load the current count register. Once transfers are enabled, each sample will decrement the current count registers until zero is reached. The next sample after zero generates an interrupt and reloads the count registers with the values in the Base registers. The interrupt is cleared by a write to the Status register.

The count register is only decremented when either the PEN or CEN bit is enabled AND a sample occurs.

Upper Base Register (Index 14)

D7	D6	D5	D4	D3	D2	D1	D0
UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

UB7-UB0 — Upper Base Bits: This byte is the upper byte of the base count register. It represents the 8 most significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count registers cannot be read. The base register should be loaded with the buffer size minus 1.

This register's initial state after reset is: 0000000

Lower Base Register (Index 15)

D7	D6	D5	D4	D3	D2	D1	D0
LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

LB7-LB0 — Lower Base Bits: This byte is the lower byte of the base count register. It represents the 8 least significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count registers cannot be read. The Base register should be loaded with the buffer size minus one.

This register's initial state after reset is: 00000000

Direct Registers:

	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	INIT	MCE	TRD	-	IA3	IA2	IA1	IA0
1	0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
2	1	0	CU/$\overline{L}$	CL/$\overline{R}$	CRDY	SER	PU/$\overline{L}$	PL/$\overline{R}$	PRDY	INT
3	1	1	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	1	1	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers:

IA3-IA0	D7	D6	D5	D4	D3	D2	D1	D0
0	LSS1	LSS0	LMGE	-	LIG3	LIG2	LIG1	LIG0
1	RSS1	RSS0	RMGE	-	RIG3	RIG2	RIG1	RIG0
2	LX1M	-	-	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0
3	RX1M	-	-	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0
4	LX2M	-	-	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0
5	RX2M	-	-	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0
6	LOM	-	LOA5	LOA4	LOA3	LOA2	LOA1	LOA0
7	ROM	-	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0
8	-	FMT	C/$\overline{L}$	S/$\overline{M}$	CSF2	CSF1	CSF0	CSL
9	CPIO	PPIO	-	-	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	-	-	DEN	-	IEN	-
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	1	-	-	-	ID3	ID2	ID1	ID0
13	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	-	LBE
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

Table 3. Register Bit Summary

	IG3	IG2	IG1	IG0	Level
0	0	0	0	0	0.0 dB
1	0	0	0	1	1.5 dB
2	0	0	1	0	3.0 dB
3	0	0	1	1	4.5 dB
.					.
.					.
.					.
12	1	1	0	0	18.0 dB
13	1	1	0	1	19.5 dB
14	1	1	1	0	21.0 dB
15	1	1	1	1	22.5 dB

Table 4. ADC Input Gain

	OA5	OA4	OA3	OA2	OA1	OA0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.							.
.							.
.							.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 6. DAC Output Attenuation

	XxG4	XxG3	XxG2	XxG1	XxG0	Level
0	0	0	0	0	0	12.0 dB
1	0	0	0	0	1	10.5 dB
2	0	0	0	1	0	9.0 dB
3	0	0	0	1	1	7.5 dB
4	0	0	1	0	0	6.0 dB
5	0	0	1	0	1	4.5 dB
6	0	0	1	1	0	3.0 dB
7	0	0	1	1	1	1.5 dB
8	0	1	0	0	0	0.0 dB
9	0	1	0	0	1	-1.5 dB
10	0	1	0	1	0	-3.0 dB
11	0	1	0	1	1	-4.5 dB
12	0	1	1	0	0	-6.0 dB
.			.			.
.			.			.
.			.			.
24	1	1	0	0	0	-24.0 dB
25	1	1	0	0	1	-25.5 dB
26	1	1	0	1	0	-27.0 dB
27	1	1	0	1	1	-28.5 dB
28	1	1	1	0	0	-30.0 dB
29	1	1	1	0	1	-31.5 dB
30	1	1	1	1	0	-33.0 dB
31	1	1	1	1	1	-34.5 dB

Table 5. AUX1, AUX2 Output Mix Gain

	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0	Level
0	0	0	0	0	0	0	0.0 dB
1	0	0	0	0	0	1	-1.5 dB
2	0	0	0	0	1	0	-3.0 dB
3	0	0	0	0	1	1	-4.5 dB
.							.
.							.
.							.
60	1	1	1	1	0	0	-90.0 dB
61	1	1	1	1	0	1	-91.5 dB
62	1	1	1	1	1	0	-93.0 dB
63	1	1	1	1	1	1	-94.5 dB

Table 7. Loopback Attenuation

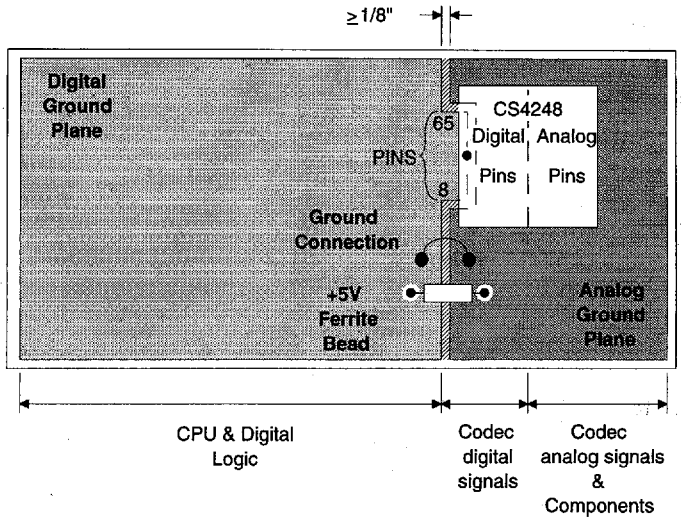


Figure 9. Suggested Layout Guideline

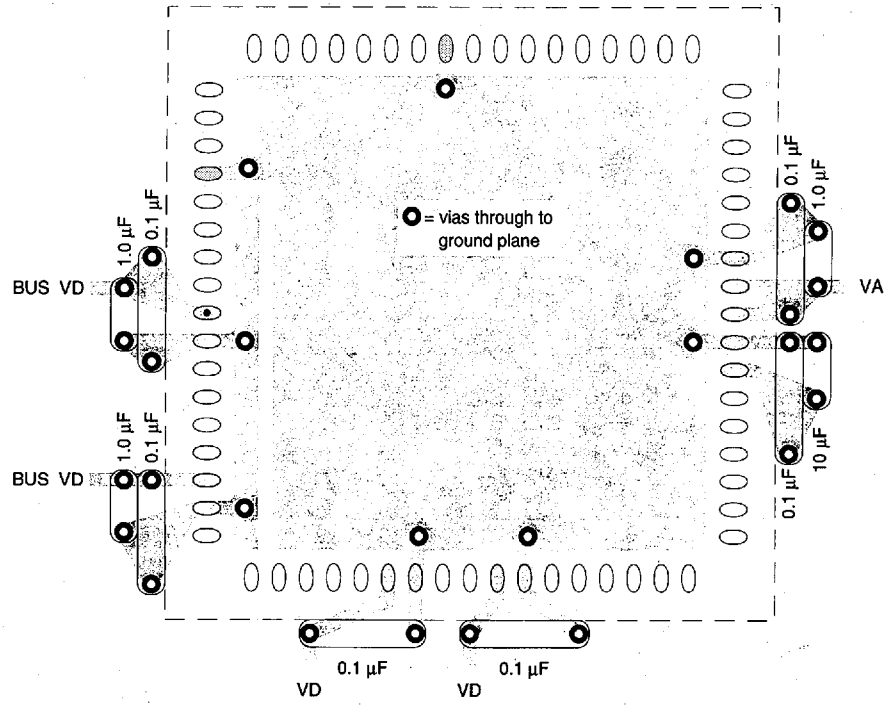


Figure 10. Recommended Decoupling Capacitor Positions

POWER SUPPLY AND GROUNDING

Figure 9 is the suggested layout for the CS4248. Similar to other Crystal codecs, it is recommended that the device be located on a separate analog ground plane. With the CS4248's parallel data interface, however, optimum performance is achieved by extending the digital ground plane across pins 65 through 68 and pins 1 through 8. Pins 2 and 8 are grounds for the data bus and are electrically connected to the digital ground plane. This minimizes the effect of the bus interface due to transient currents during bus switching. Figure 10 shows the recommended positioning of the decoupling capacitors. The capacitors must be on the same layer as, and close to, the CS4248. The vias shown go through to the ground plane layer. See Crystal's layout application note for more information.

COMPATIBILITY WITH AD1848

The CS4248 is compatible with the AD1848 rev. J silicon in terms of the applications circuit. The AD1848 rev. K requires 1.0 µF capacitors (not 1000pF) on pins 26 and 31. The CS4248 requires 1000 pF NPO-type capacitors on filter pins 26 and 31 (not 1.0 µF). To achieve compatibility with the CS4248:

1. Correct spacing of pads will ensure that either 1.0 µF capacitors (for the AD1848 rev. K) or 1000 pF NPO capacitors (for the CS4248) may be installed.

2. The CS4248 does not require the input anti-aliasing filters included as an input R/C for the AD1848 (5.1kΩ and 560 pF). The additional R/C's can be used with the CS4248 if desired, with no degradation in performance.

3. Crystal recommends the ground plane as shown in Figure 9. Any ground plane scheme that achieves acceptable performance with the AD1848 should work with the CS4248.

4. The AD1848 needs extra power and ground pins. The power pins (VDD) are pins 24, 45, and 54. The ground pins (GNDD) are pins 25 and 44. The CS4248 PLCC package does not use these pins ard the appropriate power/ground connections can be made.

5. The AD1848 does not contain the selectable dither (DEN, I10).

6. The AD1848 is not avai;able in a 100-pin TQFP package.

As far as software is concerned, the CS4248 is compatible with the AD1848 rev. K in terms of the mix gain on the AUX1 and AUX2 inputs, and the position of the output mute block. The CS4248 is also software compatible with the MCE and auto-calibration functionality of the AD1848 rev. K.

ADC and DAC Filter Response Plots

Figures 11 through 16 show the overall frequency response, pass-band ripple and transition band for the CS4248 ADCs and DACs. Figure 17 shows the DACs' deviation from linear phase.

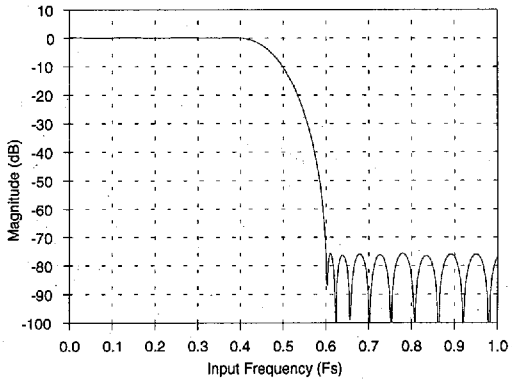


Figure 11. 16-bit ADC Filter Response.

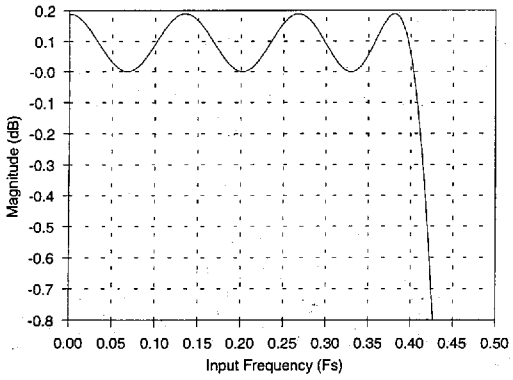


Figure 12. 16-bit ADC Passband Ripple.

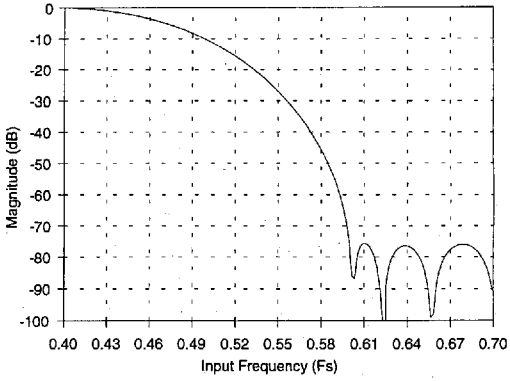


Figure 13. 16-bit ADC Transition Band.

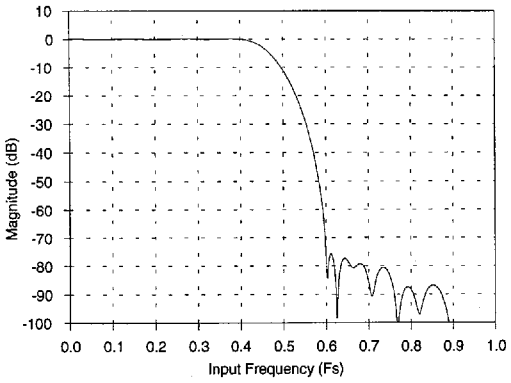


Figure 14. DAC Frequency Response

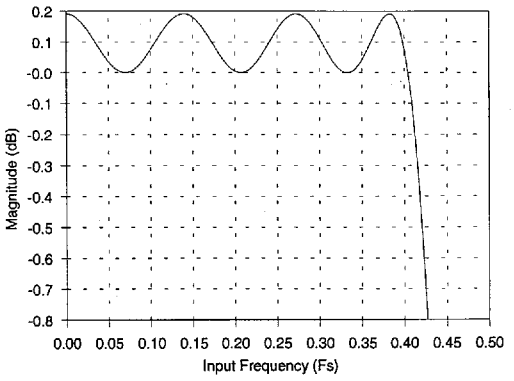


Figure 15. DAC Passband Ripple.

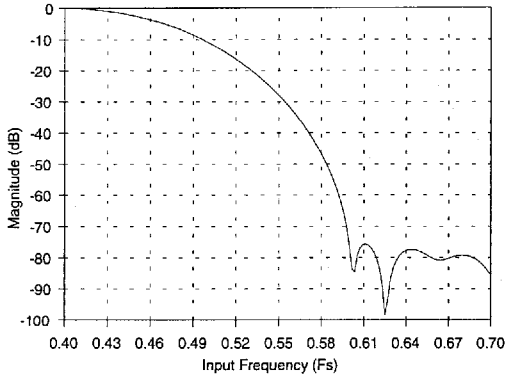


Figure 16. DAC Transition Band.

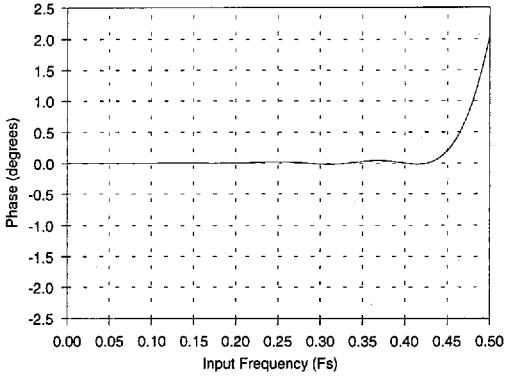
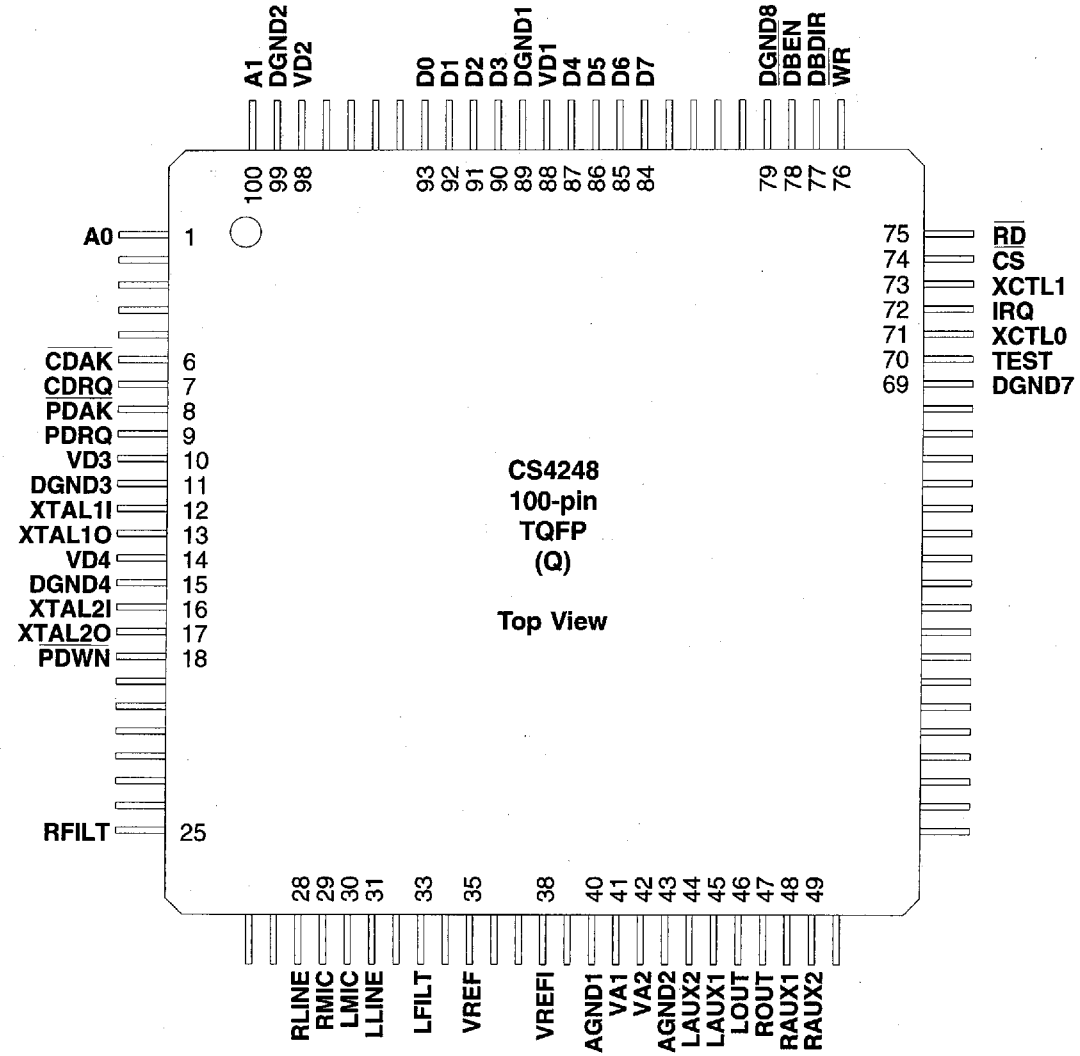
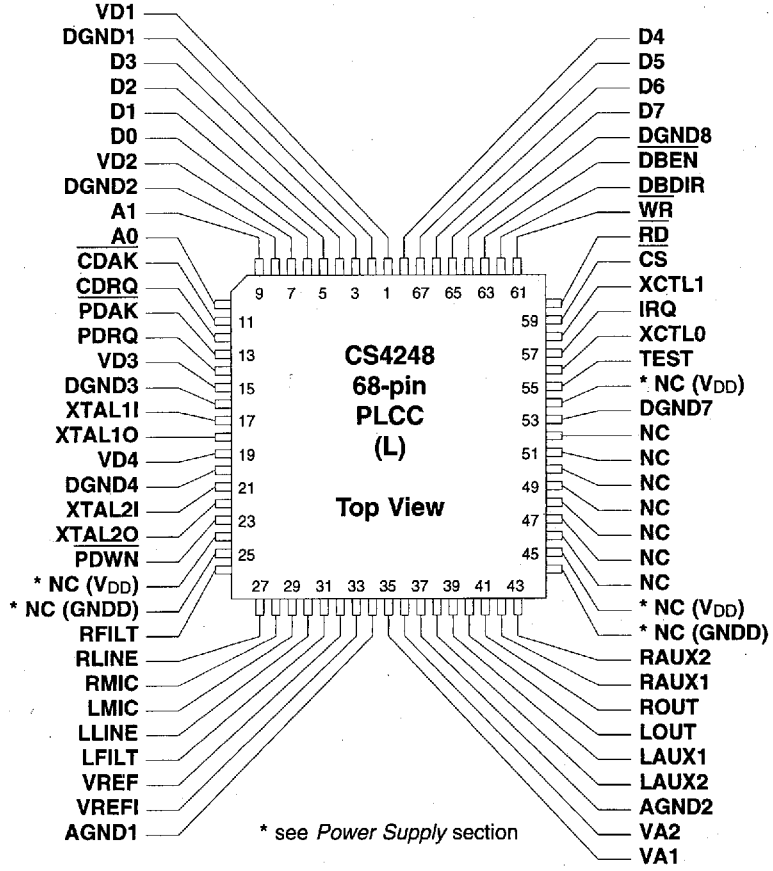


Figure 17. DAC Phase Response.

PIN DESCRIPTION





Parallel Bus Interface Pins

CDRQ - Capture Data Request, Output, Pin 12 (L), Pin 7 (Q).

The assertion of this signal indicates that the codec has a captured audio sample ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.

$\overline{\text{CDAK}}$ - Capture Data Acknowledge, Input, Pin 11 (L), Pin 6 (Q).

The assertion of this active low signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.

PDRQ - Playback Data Request, Output, Pin 14 (L), Pin 9 (Q).

The assertion of this signal indicates that the codec is ready for more playback data. The signal will remain asserted until the bytes needed for a playback sample have been transferred.

$\overline{\text{PDAK}}$ - Playback Data Acknowledge, Input, Pin 13 (L), Pin 8 (Q).
The assertion of this active low signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.

A< 1:0> - Address Bus, Input, Pin 9, 10 (L), Pin 100, 1 (Q).
These address pins are read by the codec interface logic during an I/O cycle access. The state of these address lines determines which register is accessed.

$\overline{\text{RD}}$ - Read Strobe, Input, Pin 60 (L), Pin 75 (Q).
This signal defines a read cycle to the codec. The cycle may be an I/O cycle read, or the cycle could be a read from the codec's DMA sample registers.

$\overline{\text{WR}}$ - Write Strobe, Input, Pin 61 (L), Pin 76 (Q).
This signal indicates a write cycle to the codec. The cycle may be an I/O cycle write, or the cycle could be a write to the codec's DMA sample registers.

$\overline{\text{CS}}$ - Chip Select, Input, Pin 59 (L), Pin 74 (Q).
The codec will not respond to any I/O cycle accesses unless this signal is active. This signal is ignored during DMA transfers.

D< 7:0> - Data Bus, Input/Output, Pin 65-68, 3-6 (L), Pin 84-87, 90-93 (Q).
These signals are used to transfer data to and from the CS4248.

$\overline{\text{DBEN}}$ - Data Bus Enable, Output, Pin 63 (L), Pin 78 (Q).
This pin indicates that the bus drivers attached to the CS4248 should be enabled. This signal is normally high.

DBDIR - Data Bus Direction, Output, Pin 62 (L), Pin 77 (Q).
This pin indicates the direction of the data bus transceiver. High points to the CS4248, low points to the host bus. This signal is normally high.

IRQ - Host Interrupt Pin, Output, Pin 57 (L), Pin 72 (Q).
This signal is used to notify the host of events which need servicing.

Analog Inputs

LLINE - Left Line Input, Pin 30 (L), Pin 31 (Q).
Nominally 1 V_{RMS} max analog input for the Left LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I0).

RLINE - Right Line Input, Pin 27 (L), Pin 28 (Q).
Nominally 1 V_{RMS} max analog input for the Right LINE channel, centered around VREF. The LINE inputs may be selected for A/D conversion via the input multiplexer (I1).

LMIC - Left Mic Input, Pin 29 (L), Pin 30 (Q).
Microphone input for the Left MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (LMGE = 0) or 0.1 V_{RMS} (LMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I0).

RMIC - Right Mic Input, Pin 28 (L), Pin 29 (Q).
Microphone input for the Right MIC channel, centered around VREF. This signal can be either 1 V_{RMS} (RMGE = 0) or 0.1 V_{RMS} (RMGE = 1). The MIC inputs may be selected for A/D conversion via the input multiplexer (I1).

LAUX1 - Left Auxiliary #1 Input, Pin 39 (L), Pin 45 (Q).
Nominally 1 V_{RMS} max analog input for the Left AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I0). A programmable gain block (I2) also allows routing to the output mixer.

RAUX1 - Right Auxiliary #1 Input, Pin 42 (L), Pin 48 (Q).
Nominally 1 V_{RMS} max analog input for the Right AUX1 channel, centered around VREF. The AUX1 inputs may be selected for A/D conversion via the input multiplexer (I1). A programmable gain block (I3) also allows routing to the output mixer.

LAUX2 - Left Auxiliary #2 Input, Pin 38 (L), Pin 44 (Q).
Nominally 1 V_{RMS} max analog input for the Left AUX2 channel, centered around VREF. A programmable gain block (I4) allows routing of the AUX2 channels into the output mixer.

RAUX2 - Right Auxiliary #2 Input, Pin 43 (L), Pin 49 (Q).
Nominally 1 V_{RMS} max analog input for the Right AUX2 channel, centered around VREF. A programmable gain block (I5) allows routing of the AUX2 channels into the output mixer.

Analog Outputs

LOUT - Left Line Level Output, Pin 40 (L), Pin 46 (Q).
Analog output from the mixer for the left channel. Nominally 0.707 V_{RMS} max centered around VREF.

ROUT - Right Line Level Output, Pin 41 (L), Pin 47 (Q).
Analog output from the mixer for the right channel. Nominally 0.707 V_{RMS} max centered around VREF.

Miscellaneous

XTAL1I - Crystal #1 Input, Pin 17 (L), Pin 12 (Q).
This pin will accept either a crystal with the other pin attached to XTAL1O or an external CMOS clock. XTAL1 must have a crystal or clock source attached for proper operation. The standard crystal frequency is 24.576 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL1O - Crystal #1 Output, Pin 18 (L), Pin 13 (Q).
This pin is used for a crystal placed between this pin and XTAL1I.

XTAL2I - Crystal #2 Input, Pin 21 (L), Pin 16 (Q).
If a second crystal is used, is should be placed between this pin and XTAL2O. The standard crystal frequency is 16.9344 MHz although other frequencies can be used. The crystal should be designed for fundamental mode, parallel resonance operation.

XTAL2O - Crystal #2 Output, Pin 22 (L), Pin 17 (Q).
This pin is used for a crystal placed between this pin and XTAL2I.

$\overline{\text{PDWN}}$ - Power Down Signal, Input, Pin 23 (L), Pin 18 (Q).
Places CS4248 in lowest power consumption mode. All sections of the CS4248, except the bus interface logic which reads 80h, are shut down and consuming minimal power. The CS4248 is in power down mode when this pin is logic low.

XCTL0, XCTL1 - External Control, Output, Pin 56, 58 (L), Pin 71, 73 (Q).
These signals are controlled by register bits inside the CS4248. They can be used to control external logic via TTL levels.

VREF - Voltage Reference, Output, Pin 32 (L), Pin 35 (Q).
All analog inputs and outputs are centered around VREF which is nominally 2.1 Volts. This pin may be used to level shift external circuitry, although any AC loads should be buffered. High internal-gain microphone inputs can be slightly improved by placing a 10µF capacitor on VREF.

VREFI - Voltage Reference Internal, Input, Pin 33 (L), Pin 38 (Q).
Voltage reference used internal to the CS4248 must have a 0.1 µF + 10 µF capacitor with short fat traces to attach to this pin. No other connections should be made to this pin.

LFILT - Left Channel Antialias Filter Input, Pin 31 (L), Pin 33 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

RFILT - Right Channel Antialias Filter Input, Pin 26 (L), Pin 25 (Q).
This pin needs 1000 pF NPO capacitor attached and tied to analog ground.

TEST - Test, Pin 55 (L), Pin 70 (Q).
This pin must be tied to ground for proper operation.

Power Supplies

VA1, VA2 - Analog Supply Voltage, Pin 35, 36 (L), Pin 41, 42 (Q).
Supply to the analog section of the codec.

AGND1, AGND2 - Analog Ground, Pin 34, 37 (L), Pin 40, 43 (Q).

Ground reference to the analog section of the codec. Internally, these pins are connected to the substrate as are DGND3/4/7/8; therefore, optimum layout is achieved with the AGND pins on the same ground plane as DGND3/4/7/8 (see Figure 10). However, other ground arrangements should yield adequate results.

VD1, VD2 - Digital Supply Voltage, Pin 1, 7 (L), Pin 88, 98 (Q).

Digital supply for the parallel data bus section of the codec.

VD3, VD4 - Digital Supply Voltage, Pin 15, 19 (L), Pin 10, 14 (Q).

Digital supply for the internal digital section of the codec (except for the parallel data bus).

DGND1, DGND2 - Digital Ground, Pin 2, 8 (L), Pin 89, 99 (Q).

Digital ground reference for the parallel data bus section of the codec. These pins are isolated from the other digital grounds and should be connected to the digital ground section of the board (see Figure 10).

DGND3, DGND4, DGND7, DGND8 - Digital Ground, Pin 16, 20, 53, 64(L), Pin 11, 15, 69, 79(Q)

Digital ground reference for the internal digital section of the codec (except the parallel data bus). These pins are connected to the substrate of the die as are the AGND pins; therefore, optimum layout is achieved by placing DGND3/4/7/8 on the analog ground plane with the AGND pins as shown in Figure 10. However, other ground arrangements should yield adequate results.

*** NC (V_{DD}) - No Connect, Pins 24, 45, 54 (L)**

These pins are no connects for the CS4248. When compatibility with the AD1848 is desired, these pins should be connected to the digital power supply. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

*** NC (GNDD) - No Connect, Pins 25, 44 (L)**

These pins are no connects for the CS4248. When compatibility with the AD1848 is desired, these pins should be connected to digital ground. For other compatibility issues, see the *Compatibility with AD1848* section of the data sheet.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal code width. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

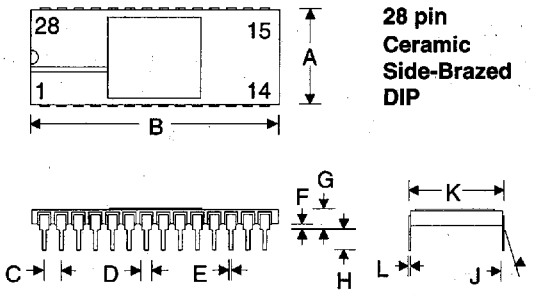
Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Offset Error

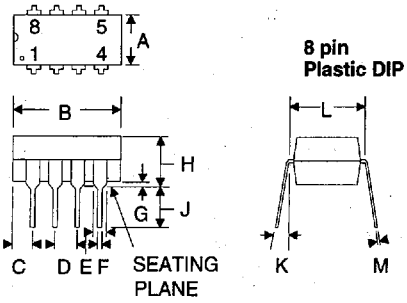
For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation in volts of the output from VREF with mid-scale input code.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

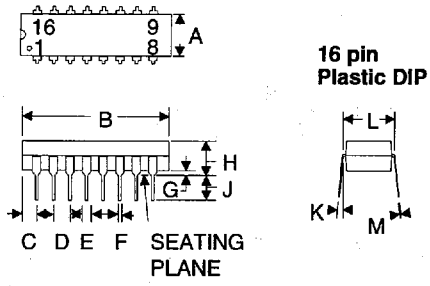
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

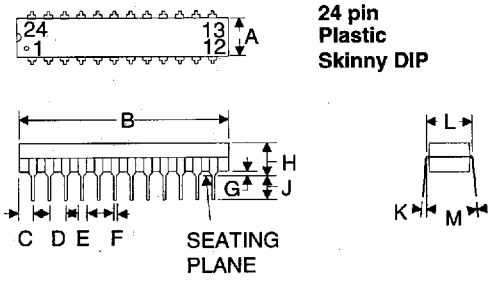
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

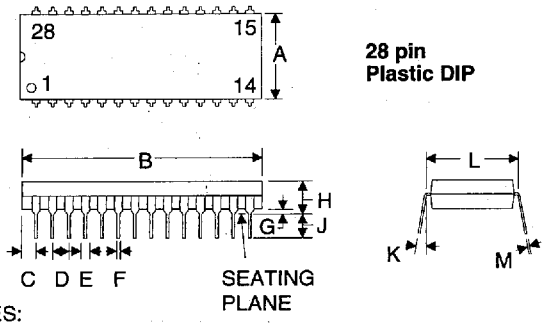
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

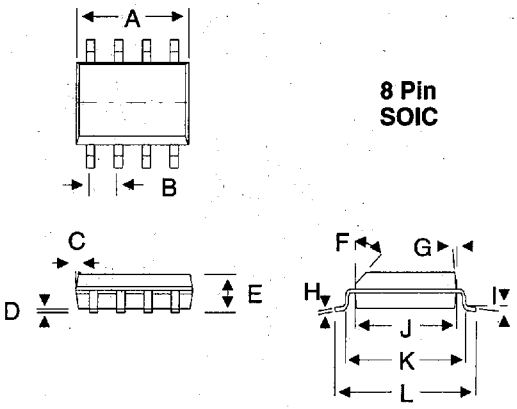
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

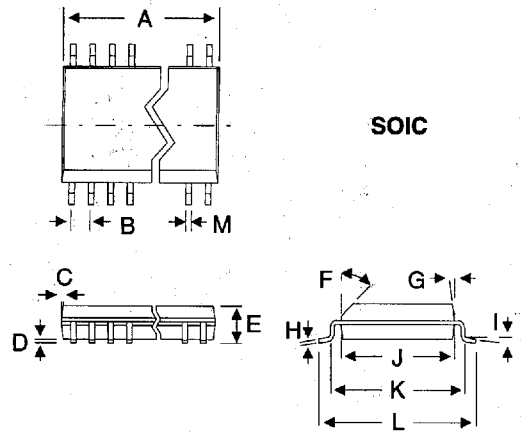
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

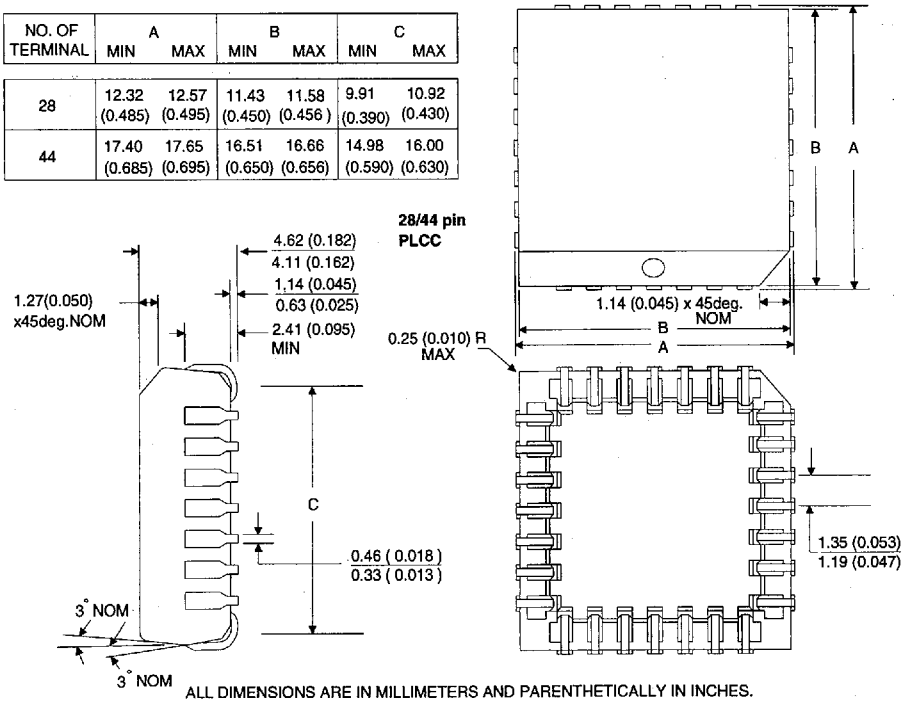


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

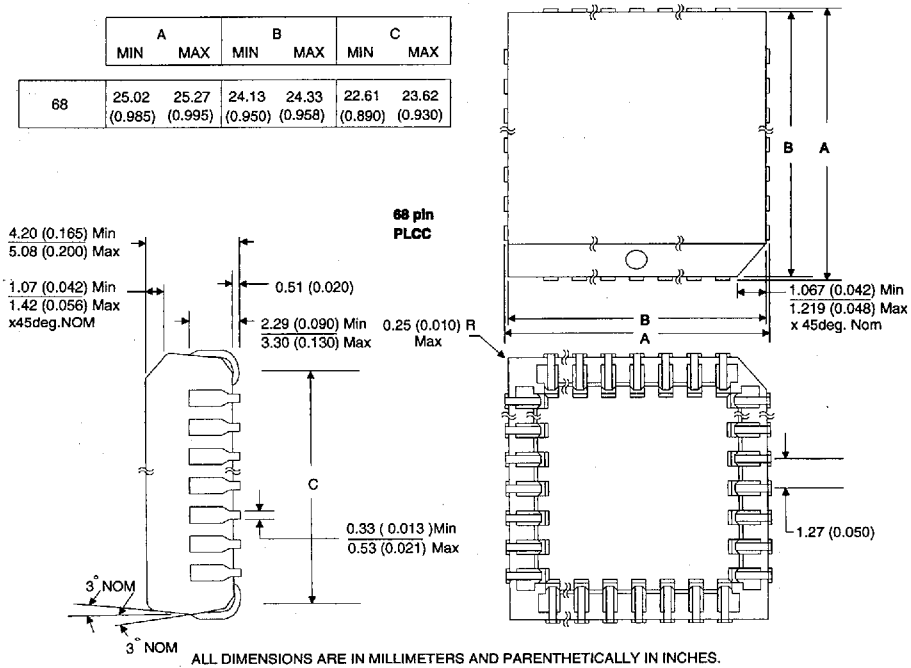
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

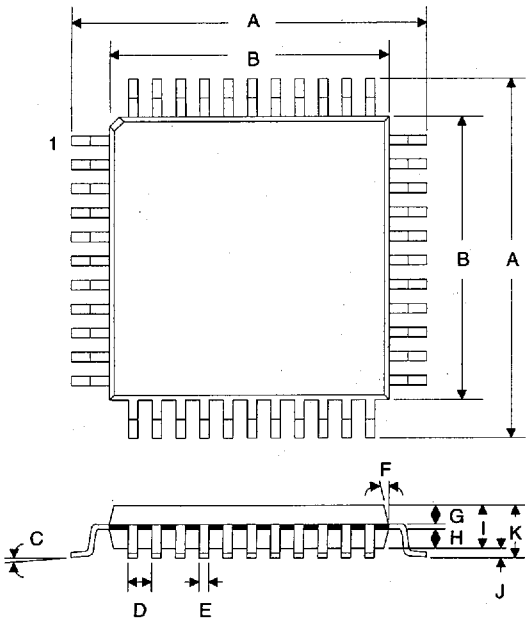
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

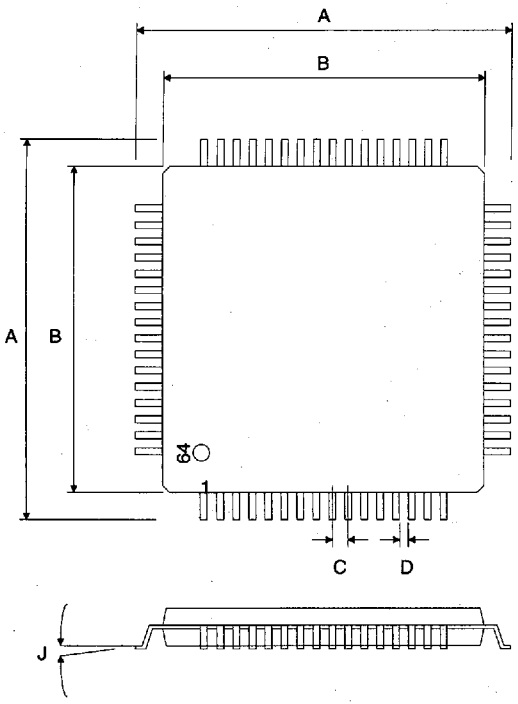
11

44 PIN QUAD FLATPACK



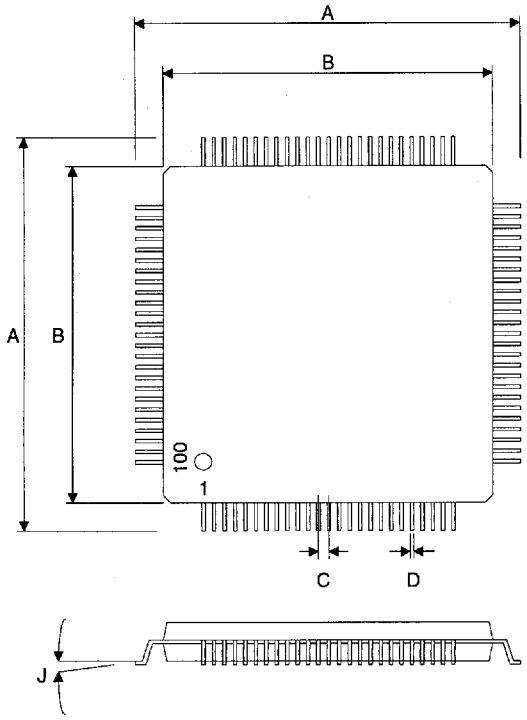
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026

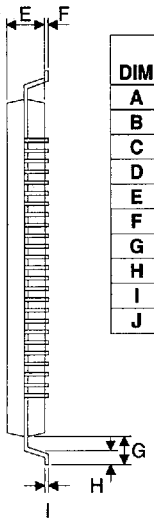
0.102 MAX
Lead Coplanarity



64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

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