Preliminary

Am81C176

CMOS Color Palette

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Plug-in Replacement for Inmos G171 and G176
- VGA hardware and software compatible
- Clock rates up to 80 MHz
- Available in 28-pin DIP and 32-pin PLCC package
- 256 x 18 Color Look-Up Table (LUT)
- Triple 6-bit Digital-to-Analog Converters (DACs)
- RS-170A compatible RGB outputs
- External current reference
- Asynchronous MPU interface
- Single monolithic, high-performance CMOS
- Single +5 V power supply

GENERAL DESCRIPTION

The Am81C176 is a monolithic CMOS Color Palette and is hardware and software compatible with the VGA standard. Applications include high-resolution color graphics, CAD/CAM/CAE, and desktop publishing. The Am81C176 operates at speeds up to 80 MHz and can support monitors with resolutions up to 1024 x 768.

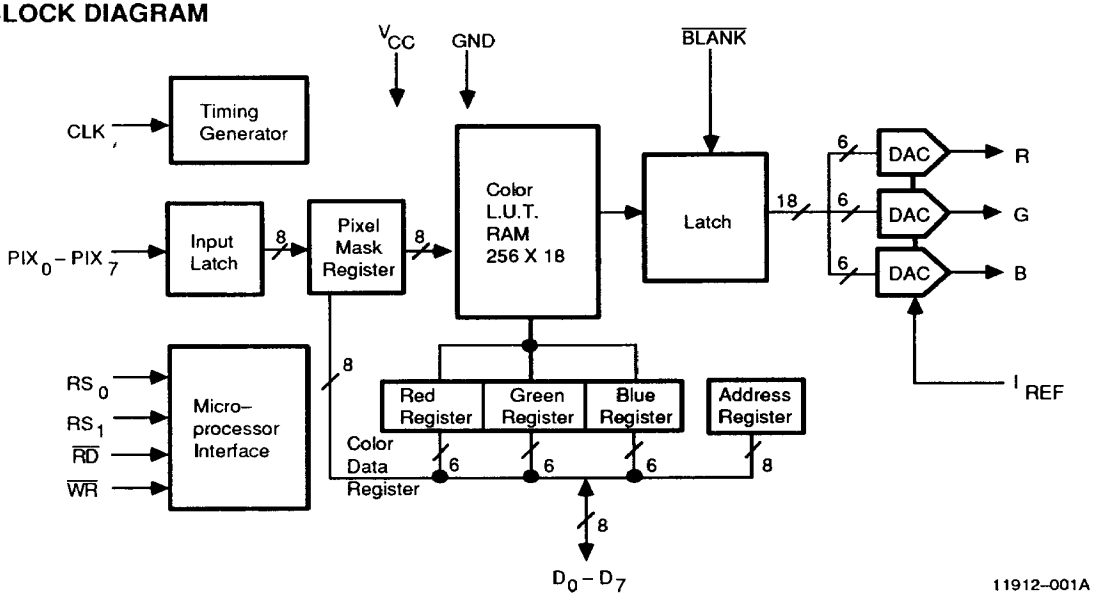
The Am81C176 has a 256 x 18 Look-Up Table and triple 6-bit DACs. It can simultaneously display 256 colors out of an available set of 256K colors.

Because of a proprietary technique, read and write operations to the Color look-up table may occur during active video.

The Am81C176 generates RS-170A compatible outputs into doubly-terminated 75Ω loads, without external buffers.

The Am81C176 is fabricated using AMD's state-of-the-art 1.2µ CMOS process. The device is available in a 28-lead DIP and 32-lead PLCC package. It is pin- and functionally-compatible with the Inmos IMS G171 and IMS G176.

BLOCK DIAGRAM

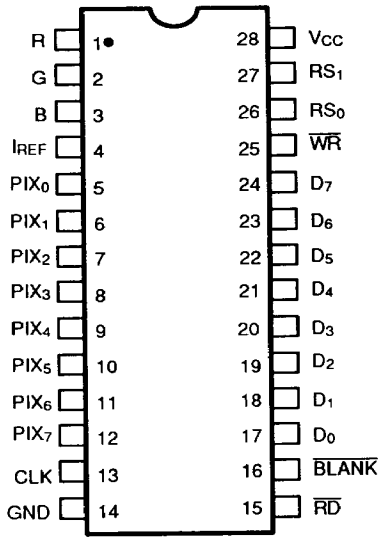


11912–001A

Publication # 11912 Rev. A Amendment /0
Issue Date: April 1989

CONNECTION DIAGRAMS
Top View

28-PIN DIP



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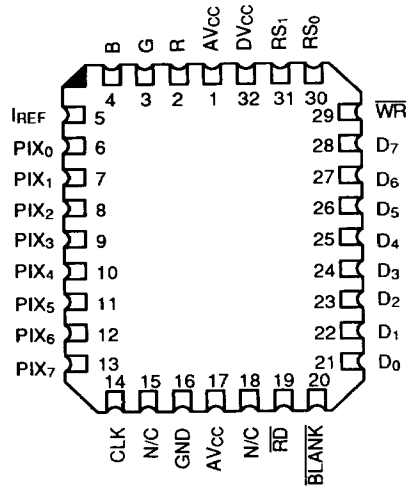
32-PIN PLCC



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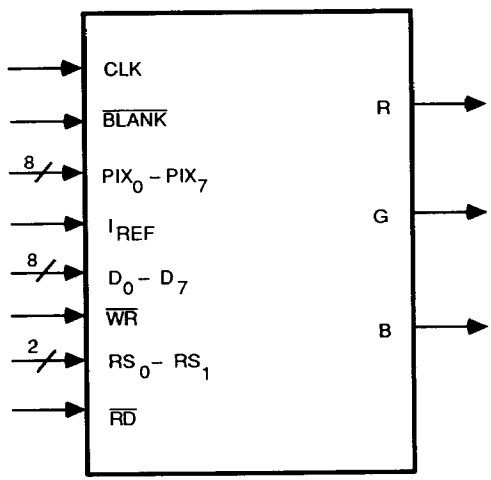
LOGIC SYMBOL



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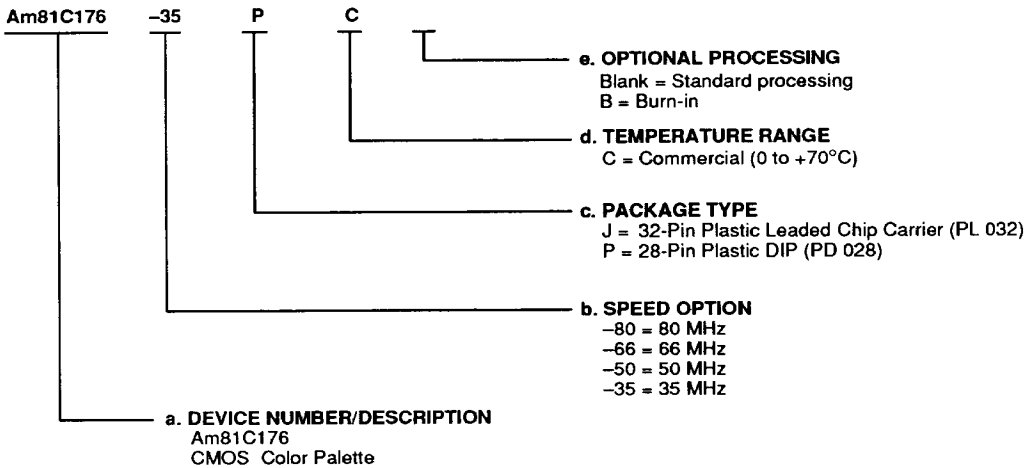
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Am81C176-80 Am81C176-66 Am81C176-50 Am81C176-35	JC, PCB, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Timing Section

CLK

Clock source pin (TTL compatible Input)

This input is the pixel clock of the video system and is to be driven by a dedicated TTL buffer. The rising edge of CLK latches the $\overline{BLANK}$ and $PIX_0 - PIX_7$ inputs and also controls the flow of these signals through the pipeline stages of the Color Palette and DACs to the R, G, and B outputs.

$\overline{BLANK}$

Blank (TTL compatible input)

The $\overline{BLANK}$ input, when active, overrides the pixel data to force the R, G, and B outputs to their blank levels. This blank level is required during the monitor vertical and horizontal retrace times. It is latched on the rising edge of CLK. Typically, blank time is used to update the Color-Look-up Table through $D_0 - D_7$.

Bit Map Interface Section

$PIX_0 - PIX_7$

Color Pixel Data addresses (TTL compatible inputs)

These 8 inputs select which of the 256 entries in the Color Look-Up Table is to be used to provide pixel color information. These inputs run at the pixel rate of the system and are latched on the rising edge of CLK. PIX_0 is the least significant bit.

MPU Interface Section

$D_0 - D_7$

Data and address bus (TTL compatible bi-directional)

These 8 pins are used by the host microprocessor to write to (with $\overline{WR}$ low) and read from (with $\overline{RD}$ low) the internal registers (Pixel Mask Register, Pixel Address Register, and Color Data Register). D_0 is the least significant bit.

During write cycles, the rising edge of $\overline{WR}$ latches data from the $D_0 - D_7$ inputs into the register selected by the $RS_0 - RS_1$ inputs. During read cycles, $\overline{RD}$ drives the $D_0 - D_7$ lines from the register selected by $RS_0 - RS_1$. The end of a read cycle is determined by the rising edge of $\overline{RD}$.

When both $\overline{WR}$ and $\overline{RD}$ are a logical one, the $D_0 - D_7$ pins go into three-state.

$\overline{WR}$

Write Control Input (TTL compatible Input)

$\overline{WR}$ is the control signal used for writing data into internal registers. $\overline{WR}$ must be a logical zero to write data to the internal registers. During Write operations, $RS_0 - RS_1$ are latched on the falling edge of $\overline{WR}$ and $D_0 - D_7$ are latched on the rising edge of $\overline{WR}$. When active, information on the external data bus is available to the $D_0 - D_7$ inputs.

$\overline{RD}$

Read Control Input (TTL compatible Input)

$\overline{RD}$ must be a logical zero to read data from the internal registers. During Read operations, $RS_0 - RS_1$ are latched on the falling edge of $\overline{RD}$. When active, information on the internal data bus is available to the $D_0 - D_7$ pins.

$RS_0 - RS_1$

Register Select Inputs (TTL compatible Inputs)

$RS_0 - RS_1$ allow the MPU to select any of the internal registers. These inputs determine the type of read or write operation being performed. See Table 1.

Analog Output Section

R

Red video output (Analog output)

Analog output of the red DAC. This output is capable of driving an RS-170A compatible doubly-terminated 75Ω cable.

G

Green video output (Analog output)

Analog output of the green DAC. This output is capable of driving an RS-170A compatible doubly-terminated 75Ω cable.

B

Blue video output (Analog output)

Analog output of the blue DAC. This output is capable of driving an RS-170A compatible doubly-terminated 75Ω cable.

I_{REF}

Current reference (Analog input).

I_{REF} is the reference current input. Through this pin the user provides the reference current for the DAC which, in turn, control the full-scale output currents.

$$I_{REF} = \frac{1}{2.1} * \frac{V_{white}}{R_{load} (= 37.5\Omega)}$$

Power Supply Section

V_{CC}

+5 volt supply.

DVcc

+5 volt digital power supply.

AVcc

+5 volt analog power supply.

GND

Ground

FUNCTIONAL DESCRIPTION

The Am81C176 CMOS color palette integrates all major functions required in the video section of a graphics system and supports pixel rates sufficient to drive monitors with resolutions up to 1024 x 768.

A programmable 256 x 18 Color Look-Up Table (LUT) maps pixel data from a bit-map memory into physical color, and three 6-bit Digital-to-Analog-Converters (DACs) convert the outputs of the Color Look-Up-Table (LUT) into RS170 compatible RGB analog format. Up to 8 bits per pixel are supported for a maximum of 256 simultaneous colors out of 256K available color combinations.

MPU Interface

The Am81C176 is designed to support a standard MPU bus interface with direct access to 256 Color Look-Up Table (LUT) locations and two control registers. The MPU interface is completely asynchronous with respect to pixel clock. However, data transfers between the LUT and Red Register, Green Register, and Blue Register (see block diagram) are internally synchronized to pixel clock. Double sampling techniques have been utilized in order to minimize metastability problems occurring when synchronizing an asynchronous event (such as $\overline{RD}$ or $\overline{WR}$) with a free running clock (such as CLK).

The Read and Write accesses to the LUT take one and two pixel clock cycles, respectively.

The nature of the MPU access is determined by the Register Select (RS_1, RS_0) inputs. RS_1 and RS_0 select among Address Register (LUT write), Address Register (LUT read), Color Data Register and Pixel Mask Register, as shown in Table 1.

Table 1. RS_0, RS_1 Decoding

RS_1	RS_0	Function
0	0	Address Register (LUT write)
0	1	Color Data Register
1	0	Pixel Mask Register
1	1	Address Register (LUT read)

A typical ***color data write cycle*** is initiated by setting the 8-bit Address Register (LUT write) with the address of the LUT into which data is to be written. Next the MPU performs three write cycles to the Color Data Register: one for red, one for green, one for blue intensity. At the end of the blue cycle the data is concatenated into an 18-bit word and written to the LUT location pointed to by the Address Register. The Address Register is then auto-incremented to point to the next location in LUT. This process may be repeated again as required. If the user needs to access consecutive LUT locations, the Address Register needs to be written to only at the beginning of the sequence. See Table 2.

A typical ***color data read cycle*** is initiated by setting the 8-bit Address Register (LUT read) with the address of the LUT to be read. At this point, 18 bits of color data are transferred from the LUT to the Red, Green and Blue portion of the Color Data Register (see block diagram) and the Address Register is auto-incremented to point to the next location in LUT. Next the MPU performs three read cycles to the Color Data Register: one for red, one for green, one for blue intensity. At the end of the blue cycle a new set of 18 bits is tranferred to the Red, Green and Blue portions of the Color Data Register, and the Address Register is again auto-incremented. This process may be repeated as required. If the user needs to access consecutive LUT locations the Address Register needs to be written to only at the beginning of the sequence. See table 2.

The 6-bit color data occupy the six least significant positions in the data bus. Bits D_6 and D_7 are ignored during write cycles and are set to 0 during read cycles. Bit D_0 is the least significant bit.

The Am81C176 uses one 8-bit ***Address Register*** to address the LUT as shown in Table 3. The Address Register resets to 0 after a blue read/write cycle to the LUT address 255. A user transparent modulo-3 counter (AR_b, AR_a) keeps track of the red, green and blue cycles and auto-increments at the end of each read/write access to the LUT. This counter is reset to zero after a write access to the Address Register, and is unchanged following a read access to the Address Register. Thus a write to the Address Register will abort any unfinished read or write sequence.

The Am81C176 uses one 8-bit ***Pixel Mask Register*** to modify the address of the LUT as provided by PIX_0 – PIX_7. The eight bits of this register are ANDed with PIX_0 – PIX_7, and the result used as the address to the LUT . This mechanism provides a quick way to alter the appearance of one or more colors on the display unit with just one MPU access, without the need for changing the bit-map memory or the LUT contents. The CPU addresses are not affected by this register.

Display Memory Interface

Pixel data PIX_0 – PIX_7 are latched on the rising edge of CLK and are used as address to the 256 locations of the LUT. The total pipeline delay from PIX_0 – PIX_7 and $\overline{BLANK}$ inputs, to R, G, B outputs is four clock cycles.

Video Generation

During each clock cycle, a 18-bit word from the LUT is presented to three DACs: 6 bits for red, 6 for green and 6 for blue. The three DACs convert the digital color memory output into RGB RS-170A analog format.

The $\overline{BLANK}$ input is latched on the rising edge of CLK. It is routed to the three DACs after a delay of four clock periods, identical to the delay incurred by the video stream.

$\overline{BLANK}$, when active, forces a zero to the input to the DACs, overriding the current LUT output.

The three analog outputs of the Am81C176 are each capable of driving a doubly terminated 75Ω coaxial cable.

Table 2. Read/Write Access to the Am81C176

$\overline{RD}$	$\overline{WR}$	RS_1	RS_0	AR_b	AR_a		Function
1	0	0	0	X	X	Write Address Register (LUT Write)	AR(7:0)←D(7:0); ARb:ARa←00.
1	0	0	1	0	0	Write Color Data Register(Red)	RREG(5:0)←D(5:0); ARb:ARa←01.
1	0	0	1	0	1	Write Color Data Register(Green)	GREG(5:0)←D(5:0); ARb:ARa←10;
1	0	0	1	1	0	WriteColor Data Register(Blue)	BREG(5:0)←D(5:0); ARb:ARa←00;
						Write Color Look-Up-Table	R(5:0)←RREG; G(5:0)←GREG; B(5:0)←BREG; INC. AR(7:0).
1	0	1	1	X	X	Write Address Register (LUT Read)	AR(7:0)←D(7:0); ARb:ARa←00;
						Read Color Look-Up Table	RREG←R(5:0); GREG←G(5:0); BREG←B(5:0); INC. AR(7:0).
0	1	0	1	0	0	Read Color Data Register (Red)	D(5:0)←RREG(5:0); D(7:6)←0; ARb:ARa←01.
0	1	0	1	0	1	Read Color Data Register (Green)	D(5:0)←GREG(5:0); D(7:6)←0; ARb:ARa←10.
0	1	0	1	1	0	Read Color Data Register (Blue)	D(5:0)←BREG(5:0); D(7:6)←0; ARb:ARa←00.
0	1	0	0	X	X	Read Address Register	D(7:0)←AR(7:0).
1	0	1	0	X	X	Write Pixel Mask Register	PMREG(7:0)←D(7:0).
0	1	1	0	X	X	Read Pixel Mask Register	D(7:0)←PMREG(7:0).

Note: Refer to timing diagrams for edge information on $\overline{RD}$ and $\overline{WR}$.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
Junction Temperature	+175°C
Supply Voltage to Ground Potential Continuous	−0.5 to 7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 to V_{CC} +0.5 V
DC Input Voltage	−0.5 to V_{CC} +0.5 V

Stresses above those listed under "Absolute Maximum Ratings" may cause device failure. Functionality at or above these limits is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC}) for 80 MHz devices	+4.75 to +5.25 V
for 35, 50, 66 MHz device	+4.50 to +5.50 V
I_{REF} Current	−7 to −9 mA
Output Load	37.5Ω

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (over operating range)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
Digital Inputs						
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{IL}	Input Low Voltage		GND-0.5		0.8	V
I_{IH}	Input High Current	V_{in}= V_{CC}			1	µA
I_{IL}	Input Low Current	V_{in}= GND			−1	µA
C_{IN}	Input Capacitance	f=1 MHz, V_{in}= 2.4 V			7	pF
Digital Outputs						
V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = +5 mA			.4	V
I_{OZ}	Three-State Current	GND <= V_{in} <= V_{CC}			50	µA
C_{out}	Output Capacitance				7	pF
Analog Outputs						
	Resolution (each DAC)		6	6	6	Bits
INL	Integral Linearity Error				±1/2	LSB
DNL	Differential Linearity Error				±1/2	LSB
	Full Scale Error				±5	%Gray
	Monotonicity			Guaranteed		
	Coding	Binary				Binary
	Output Voltage				1.5	V
	Output Current				21	mA
	DAC-to-DAC Matching				2	%
	Glitch Energy			120		pV-sec

SWITCHING CHARACTERISTICS

Parameter Number	Parameter Description	Min/Typ Max					Unit
	Clock Rate		80	66	50	35	MHz
1	$RS_0 - RS_1$ Setup Time	Min	10	10	10	15	ns
2	$RS_0 - RS_1$ Hold Time	Min	10	10	10	15	ns
3	$\overline{RD}$ Asserted to Data Bus Driven	Min	5	5	5	5	ns
4	$\overline{RD}$ Asserted to Data Valid	Max	40	40	40	40	ns
5	$\overline{RD}$ Negated to Data Bus 3-stated	Max	20	20	20	20	ns
6	Output Hold Time	Min	5	5	5	5	ns
7	$\overline{RD}$ Pulse Width Low	Min	50	50	50	50	ns
8	$\overline{WR}$ Pulse Width Low	Min	50	50	50	50	ns
9	Write Data Setup Time	Min	10	10	10	15	ns
10	Write Data Hold Time	Min	10	10	10	15	ns
11	Clock Cycle Time	Min	12.5	15.2	20	28	ns
12	Clock Pulse Width High Time	Min	4	5	6	7	ns
13	Clock Pulse Width Low Time	Min	4	5	6	9	ns
14	Pixel Setup Time	Min	3	3	3	4	ns
15	Pixel Hold Time	Min	3	3	3	4	ns
16	Analog Output Delay	Max	30	30	30	30	ns
17	Analog Output RiseTime (Note 1)	Max	3	6	8	8	ns
18	Analog Output Settling Time (Note 1)	Max	13	15.3	20	28	ns
19	Read after write address register (read mode)	Min	5* tCYC	5* tCYC	5* tCYC	5* tCYC	ns
20	Successive read interval	Min	4* tCYC	4* tCYC	4* tCYC	4* tCYC	ns
21	Read after color read	Min	5* tCYC	5* tCYC	5* tCYC	5* tCYC	ns
22	Write after color read	Min	5* tCYC	5* tCYC	5* tCYC	5* tCYC	ns
23	Successive write interval	Min	4* tCYC	4* tCYC	4* tCYC	4* tCYC	ns
24	Read after color write	Min	4* tCYC	4* tCYC	4* tCYC	4* tCYC	ns
25	Write after color write	Min	4* tCYC	4* tCYC	4* tCYC	4* tCYC	ns
26	Read followed by write interval	Min	4* tCYC	4* tCYC	4* tCYC	4* tCYC	ns
27	Write followed by read interval	Min	4* tCYC	4* tCYC	4* tCYC	4* tCYC	ns
	Analog Output Skew	Max	2	2	2	2	ns
	Pipeline Delay	Typ	4	4	4	4	clocks
	V_{CC} Supply Current (Note 3)	Typ	150	150	150	150	mA
	V_{CC} Supply Current (Note 3)	Max	180	180	180	180	mA

Notes:

1. Clock and data feedthrough are not included
2. Load = 37.5Ω + 30 pF with I_{REF} = −8.88 mA
3. Measured at maximum f_{CLK};
   I_{CC}(Max.): V_{CC} = 5.25 V, T_A = 0°C
   I_{CC}(Typ.): V_{CC} = 5.0 V, T_A = + 25°C

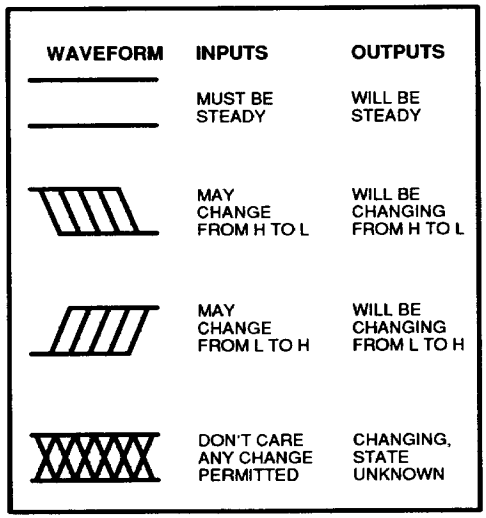
Test Conditions:

TTL Input Level: 0 to 3 V with t_R, t_F (10-90%) ≤ 3 ns

Analog Output Load ≤ 10 pF; $D_0 - D_7$ Output Load ≤ 50 pF

SWITCHING WAVEFORMS

Key To Switching Waveforms



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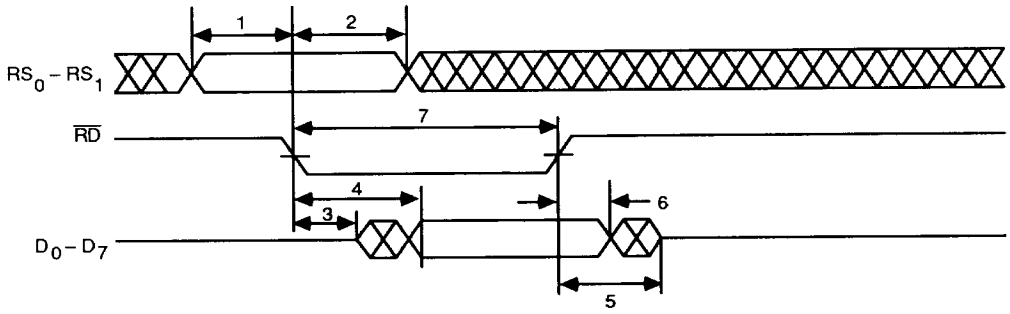
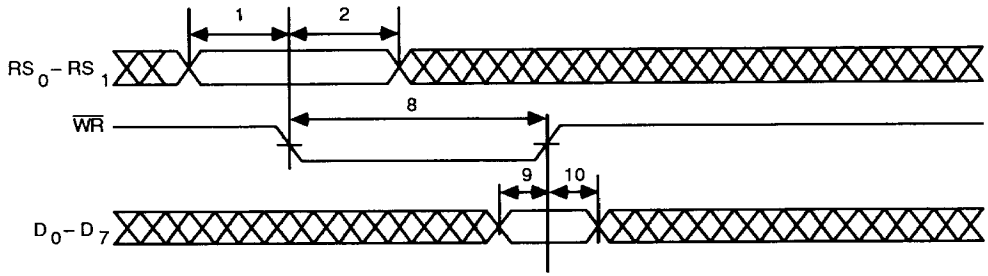
SWITCHING WAVEFORMS (continued)



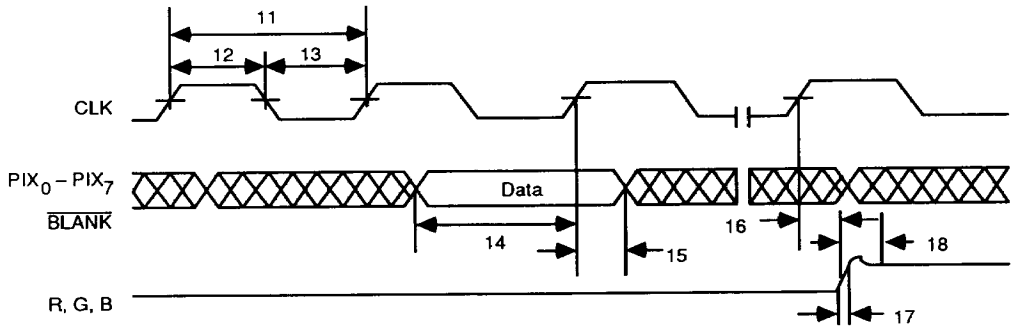
11912-005A

MPU Read Cycle



11912-006A

MPU Write Cycle



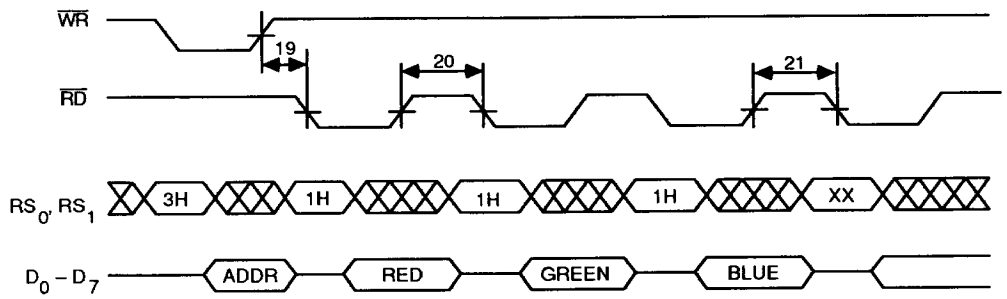
Note 1: Output delay measured from the 50% point of the rising edge of CLK to the 50 % point of the full scale transition.

Note 2: Settling time measured from the 50% point of the full scale transition to the output remaining within ± 1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

11912-007A

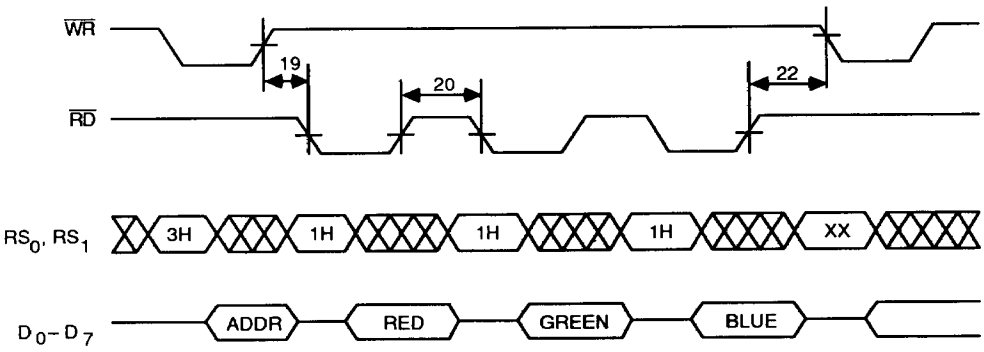
Video Input /Output



11912-008A

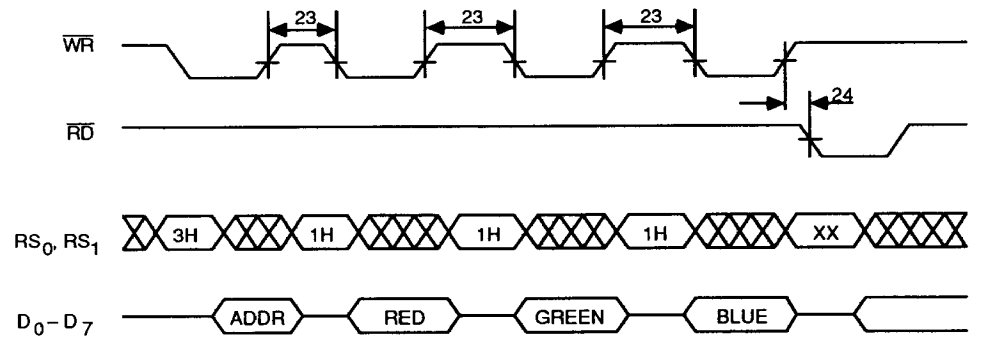
Color Value Read Followed by Any Read

SWITCHING WAVEFORMS (continued)



11912-009A

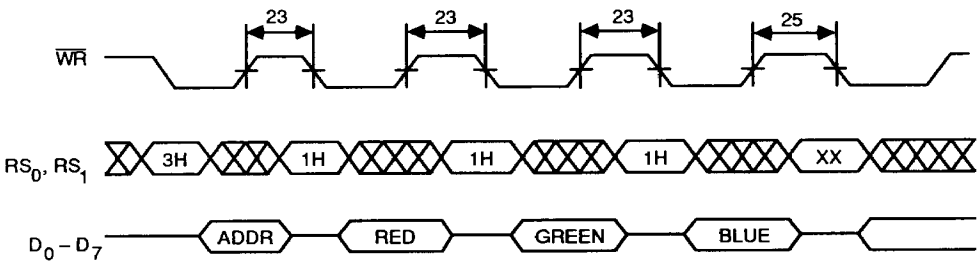
Color Value Read Followed by Any Write



11912-010A

Color Value Write Followed by Any Read

SWITCHING WAVEFORMS (continued)



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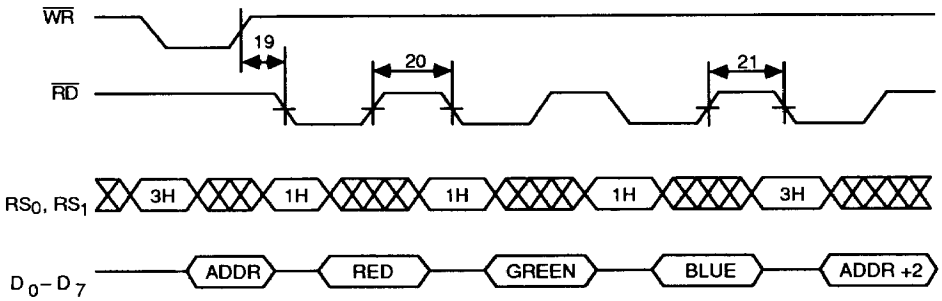
Color Value Write Followed by Any Write



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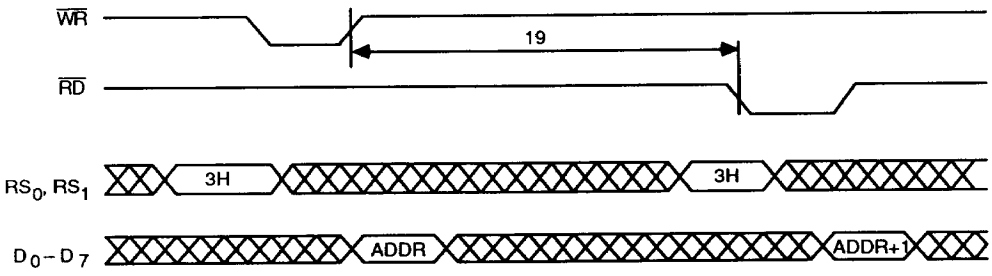
Read Color Value then Read the Address Register

SWITCHING WAVEFORMS (continued)



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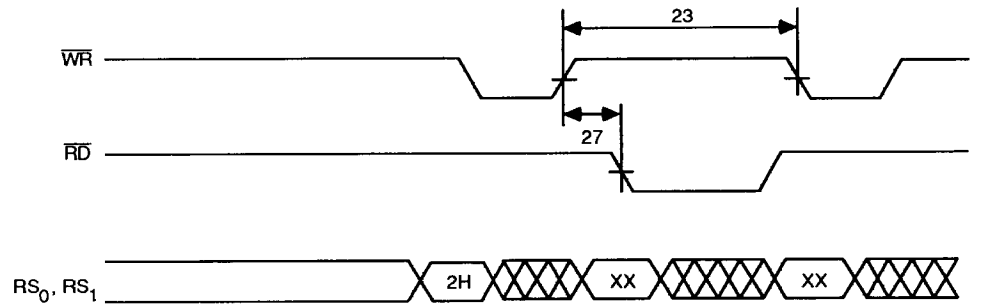
Write and then Read Back the Address Register



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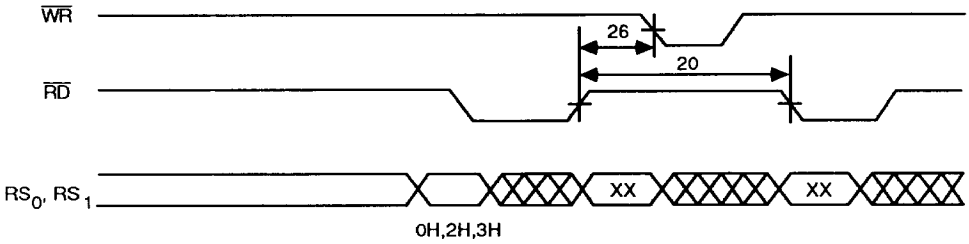
Write to Mask Register Followed by Read or Write

SWITCHING WAVEFORMS (continued)



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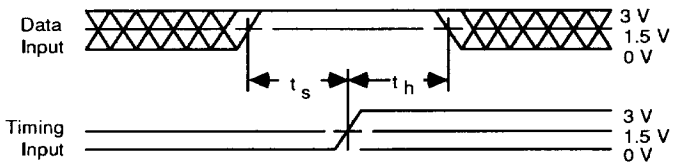
Read from Mask or Address Register Followed by Read or Write

SWITCHING TEST WAVEFORM



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross–hatched area is don't care condition.

11912-016A

APPENDIX A: APPLICATION NOTE FOR THE Am81C176

The design of a system using the Am81C176 should be based on the guidelines used for designing high precision mixed analog and digital circuits. Some of these rules are outlined here. Users may, of course, choose to design circuits considerably different from that shown here.

Separate power planes should be used for the analog and digital power pins to reduce the noise on the analog output due to the switching at the digital inputs. A high frequency capacitor of around 0.1 µf should be placed close to the package between V_{CC} and GND. A large tantalum capacitor of about 22 µF should also be placed in parallel to the 0.1 µF capacitor. This same arrangement should be used on the DIP package as well. An inductor used in series with the power supply acts as a low-pass filter and improves the Am81C176 supply even further. Care should be taken to see that the analog plane does not cross the digital plane. The pixel data lines should be kept as far from the digital lines accessible by the MPU interface.

Use of a current mirror such as the one shown in Figure A1 is recommended to ensure a constant current source for the DACs. The current sources may need to be temperature compensated externally using a diode bias. It may be necessary to add coupling capacitors (47 µF in parallel with 0.1 µF) between I_{REF} and V_{CC} to absorb power supply variations not absorbed by the current source. The two capacitors help track the variations in power supply at the low and the high frequency end.

The connection between the DACs and the monitor acts as a transmission lie The two ends of the line need to be terminated to provide proper impedance matching and thereby avoid any reflections that might result otherwise. Also, analog output protection is provided by the diode as shown in Figure A2. The diode basically acts to prevent excessive negative or positive voltage swings which could result from electrostatic discharges and things of that nature.

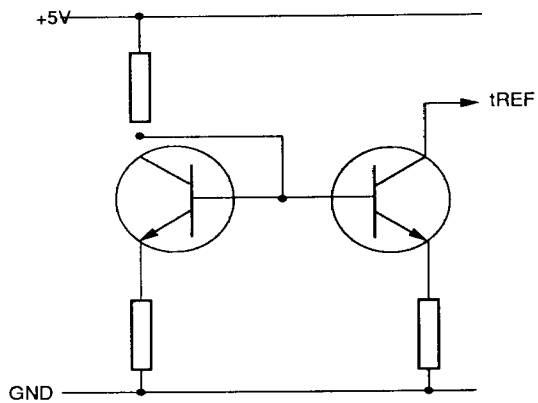


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Figure A1.

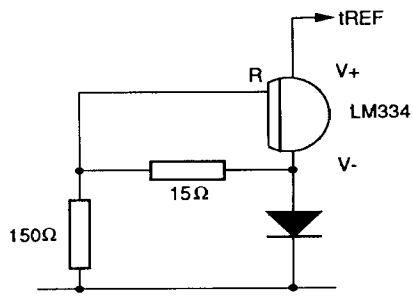

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Figure A2.

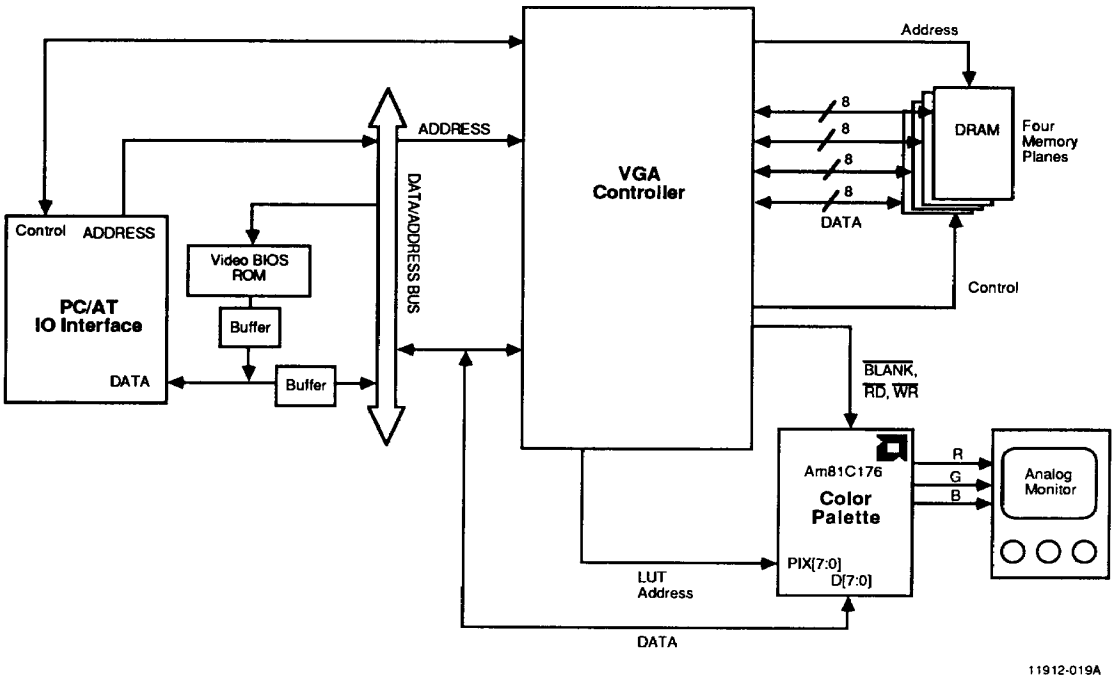
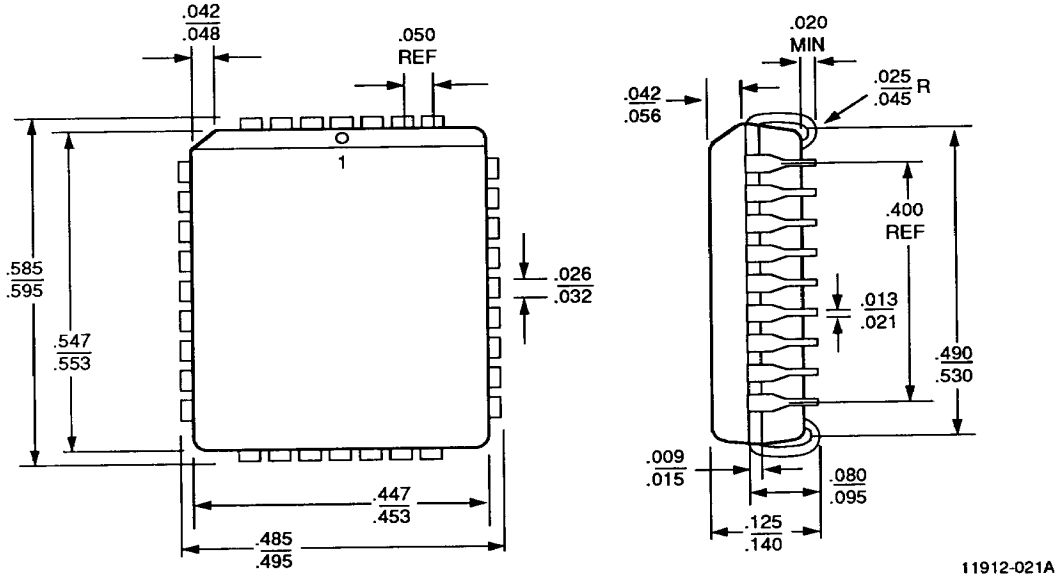


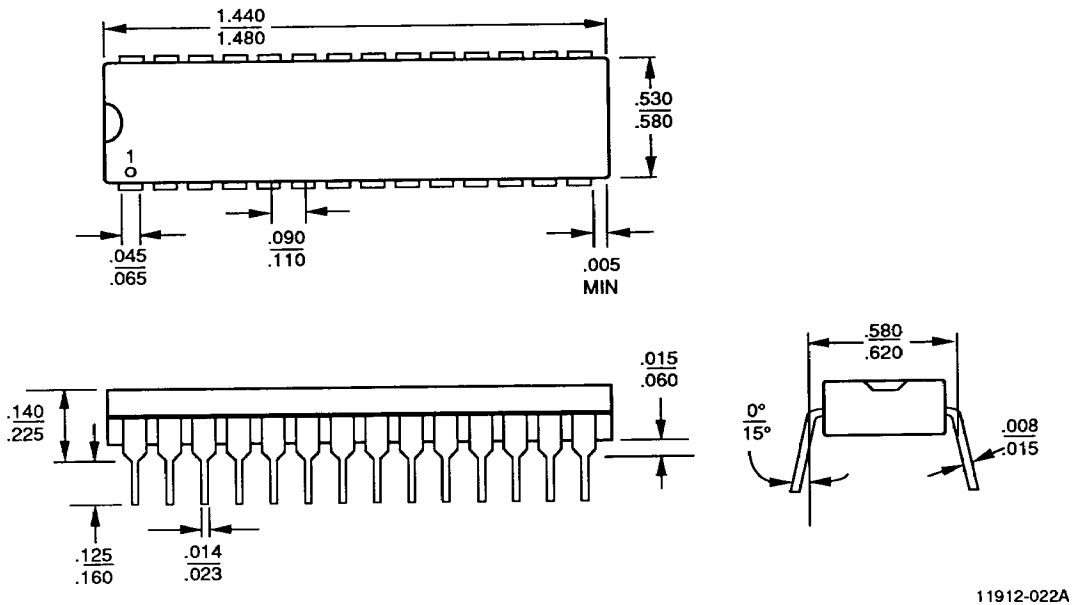
Figure A3. Application Example: VGA system using a VGA Controller and an Am81C176

PHYSICAL DIMENSIONS

PL 032



PD 028



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